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ADSP-2184x/ADSP-SC84x LPDDR4 Board Design Guidelines

Contributed by Shivakumar Puran and Manoj Chitneedi *Rev 1 – June 22, 2026*

Introduction

This EE note outlines the recommended board-level design guidelines for interfacing LPDDR4 memory in a point-to-point configuration to achieve the expected controller performance. Follow these guidelines in addition to standard board design best practices.

The ADSP-SC846 processor was used for the board design guidelines, but this EE note applies to all ADSP-2184x/ADSP-SC84x models.

PCB Stack-up

LPDDR4 operates at a higher data rate with tight timing and noise margins; therefore, a properly defined PCB stack-up is required to ensure adequate signal integrity and power integrity.

- Use a minimum 10-layer PCB stack-up. A 12-layer stack-up is recommended to provide improved fan-outs, routing flexibility, and overall design margin.
- Minimize the dielectric thickness between power and ground planes to reduce plane inductance and improve high-frequency decoupling.
- Avoid coupling between power planes and signal planes. Minimize power-to-power plane coupling to prevent noise coupling into sensitive LPDDR4 signals.
- Reference continuous planes, preferably ground, on both adjacent layers wherever possible for all LPDDR4 signal layers. Plane splits or discontinuities under LPDDR4 routing are not permitted.
- Figure 1 shows a representative 12-layer PCB stack-up example; this figure is for reference only. Because stack-up selection is design-specific, this example may not be applicable to all implementations.

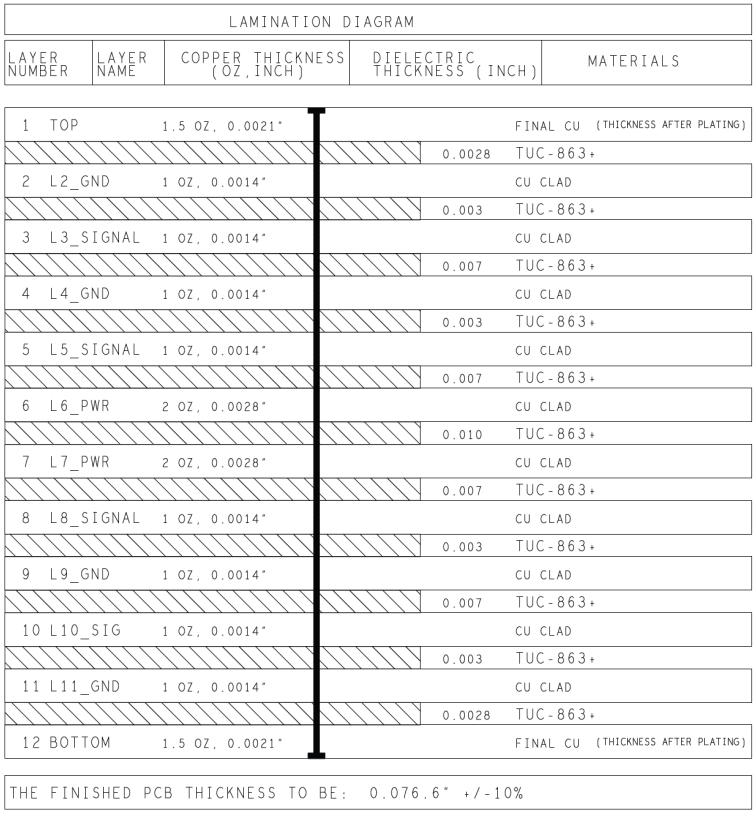

Figure 1. 12-Layer PCB Stack-up Example

Impedance Control

Impedance control is required to minimize signal reflections in high-speed designs. Proper matching of the transmission line impedance to the source and load impedance is essential for reliable signal integrity. The characteristic impedance of a PCB trace is determined by its geometry and its relationship to adjacent reference planes.

For differential pairs, trace width and trace spacing required to achieve a target impedance are dependent on the selected PCB stack-up. Since minimum trace width and spacing are constrained by the PCB manufacturing technology, the stack-up is defined such that all required impedances can be practically achieved.

Single-ended and differential impedances shall be treated independently and routed accordingly.

- LPDDR4 single-ended signal impedance: 40 Ω ±5%
- LPDDR4 differential pair impedance: 80 Ω ±5%
- All other high-speed single-ended signals: 50 Ω ±10%

LPDDR4 Signal Groups

Route all LPDDR4 signals as a group on each routing layer to prevent mismatches in trace impedance and propagation delay. Ensure that all signals within a group are routed on the same layer and contain the same number of vias and referenced to a common ground plane.

Changing the ground reference plane can change the trace impedance.

For LPDDR4 interfaces, delay skew should be controlled by matching the trace lengths within each defined signal group.

The following table outlines the recommended length-matching requirements for the LPDDR4 signal groups.

LPDDR4 Signals	Clock Reference	Group	Trace Impedance	Length Matching on PCB
CK_T_A/CK_C_A		Clock	80 Ω differential pair	
CK_T_B/CK_C_B				
DQS0_T_A/DQS0_C_A	CK_T_A/CK_C_A	Strobe		CK_T_A +/-2.5 mils
DQS1_T_A/DQS1_C_A				
DQS0_T_B/DQS0_C_B	CK_T_B/CK_C_B			CK_T_B +/-2.5 mils
DQS1_T_B/DQS1_C_B				
CA[5:0]_A	CK_T_A/CK_C_A	ADDR/CMD/CNTR	40 Ω single-ended	CK_T_A Trace +/-15mils
CS0_A				
CKE0_A				
CA[5:0]_B	CK_T_B/CK_C_B			CK_T_B Trace +/-15mils
CS0_B				
CKE0_B				
DMI0_A	DQS0_T_A/DQS0_C_A	Data Byte 0		DQS0_T_A Trace +/-15mils
DQ[7:0]_A				
DMI1_A	DQS1_T_A/DQS1_C_A	Data Byte 1		DQS1_T_A Trace +/-15mils
DQ[15:8]_A				
DMI0_B	DQS0_T_B/DQS0_C_B	Data Byte 2		DQS0_T_B Trace +/-15mils
DQ[7:0]_B				
DMI1_B	DQS1_T_B/DQS1_C_B	Data Byte 3		DQS1_T_B Trace +/-15mils
DQ[15:8]_B				
Differential Signals				Intra-pair Skew +/-1mils

Termination Requirements

- The ZQ of the digital signal processor must be connected to GND through a 120 Ω ±1%resistor. The total capacitance on the net connecting from the ZQ bump of the processor to the external calibration resistor must be limited to max 100 pF.
- Care should be taken to keep the resistance of the connection between the ZQ pins and the external calibration resistor low. A good guideline is for the pin-to-resistor total interconnect resistance to be less than 1% of the calibration resistor value.
- The ZQ pin at the DDR memory side must be connected to VDDQ through a 240 Ω ±1% resistor.
- For the RESET_N and CKE pins, a 60 Ω series resistor is recommended and must be placed close to the DRAM. The final resistor value may be adjusted based on signal integrity simulations; typically, it is chosen such that the sum of the series resistance and the driver's output impedance approximately matches the nominal board impedance.
- Some memory vendors recommend connecting the LPDDR4 RESET_N pin to GND through a pull-down resistor and the ODT_CA pin to VDD2 through a pull-up resistor. Refer to the respective memory vendor's data sheet for device-specific recommendations.

Placement and General Routing Guidelines

Use the following guidelines when designing PCB stack-up, trace routing, and component placement.

- Place the ADSP-SC846 SHARC+® processor and the memory as close as possible to each other, while minimizing routing length.
- To minimize crosstalk, the characteristic impedance of a trace must be determined predominantly by the distance to the reference plane and not the distance to the neighboring traces.
- The spacing between DDR traces within the same group must be 2× to 3× the distance to the nearest reference ground plane and above 3× the distance to the reference plane for signals of different groups. Longer routed parallel lengths must have wider spacing.
- If necessary, spacing between the same group can be cut to 1.5× to 2× the height to the nearest reference plane in stripline applications; wider spacing is always preferred.

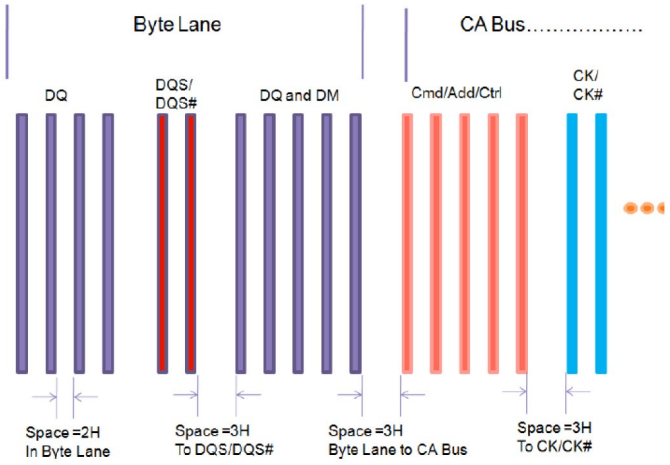

Figure 2. Spacing Between Different Signal Groups (Relative to Height from Reference Plane)

- The spacing between DDR signals to differential signals must be 3× the distance to the reference plane.
- It is recommended that the spacing between byte lanes and the spacing between the CA region be a minimum of 3× the height above the reference plane.
- Spacing to strobes and clocks must also be increased to ensure that crosstalk does not compromise the monotonicity of the system's strobes and clocks.
- If possible, it is recommended to use ground shield vias and ground guard trace around the clock and strobe traces. No floating guard traces or shielding lines should be there.
- For LPDDR4 applications that exceed 1866 Mbps, it is highly recommended that microstrip configurations be avoided.
- The trace length of LPDDR4 signals must be as short as possible.
- Spacing between parallel sections of the serpentine traces should be 3× to 4×, and parallel length should be kept as small as possible.
- All the high-speed signals must maintain solid reference planes. For DDR signals, maintain solid ground reference on both sides.
- Avoid routing over a split plane as the return current path cannot follow the signal trace.
- Use a ground plane as the primary reference or return paths for all signals. Whenever a power layer is used as the reference plane, it is important to ensure that the power layer is low-noise and there is proper stitching at the reference plane transitions to guarantee return path continuity.
- If the signals change layers and reference planes from one ground plane to another, add adjacent ground vias or capacitors close to the layer change vias to avoid return path discontinuities.
- Signal velocity varies between microstrip and stripline traces. Propagation delay difference between microstrip and stripline signals needs to be considered for meeting the required timing budgets.
- Minimize the number of vias and layer transition of LPDDR signal traces. Use the same number of vias on all data signals of the same group.

- Consider back-drilling to remove via stub and improve signal integrity.
- Avoid test points on the DDR signals, as they create stubs which can act as EMI sources. Instead, use vias for probing. It is also acceptable to use JEDEC-recommended methods that test vendors offer for diagnostics.
- Ensure that the power and ground planes are adjacent to each other to provide the shortest return path and better power integrity.
- Minimize the distance (keep as short as possible) between decoupling capacitor pins and BGA balls. Use wider trace or solid plane shape between decaps and BGA balls.
- Ideally, the trace length from the power via to the processor pad must not exceed 30 mils. The maximum trace length from each power via to its decoupling capacitor is 60 mils. The maximum trace length from each power via to its power ball pad is 35 mils.
- Use individual vias for each ground and power pads of decaps and BGA IC. Avoid via sharing between multiple pads.

DDR Supply Voltage Recommendations

- The VDDQ nominal voltage is 1.1 V for LPDDR4 (VDDQ minimum voltage is 1.06 V, and maximum voltage is 1.17 V).
- VDDQ power rail noise must be limited to within ±2.5% of its nominal value. Sufficient decoupling on the VDDQ and memory power rails is required to ensure signal integrity and avoid data corruption.
- Refer to the DDR memory data sheet or consult the vendor to identify the decoupling capacitor requirement for the DDR memory power rails.
- Place all decoupling capacitors very close to the VDDQ power rail and use solid power and ground planes.
- Isolate the DDR power planes from other supply planes. If this is not possible, separate them as much as possible and avoid overlapping them.
- Ensure that decoupling capacitors for the VDDQ power rail are placed as close as possible to the actual power pins. DDR signal slew rates are aggressive. Placing these capacitors close to the pin is **mandatory**. Wherever possible, provide dedicated power and ground vias for each decoupling capacitor pin.
- If the VAA_PLL supply is shared with other circuits on the PCB, it is recommended to include a ferrite filter circuit on the printed circuit board (PCB) as shown in Figure 3.

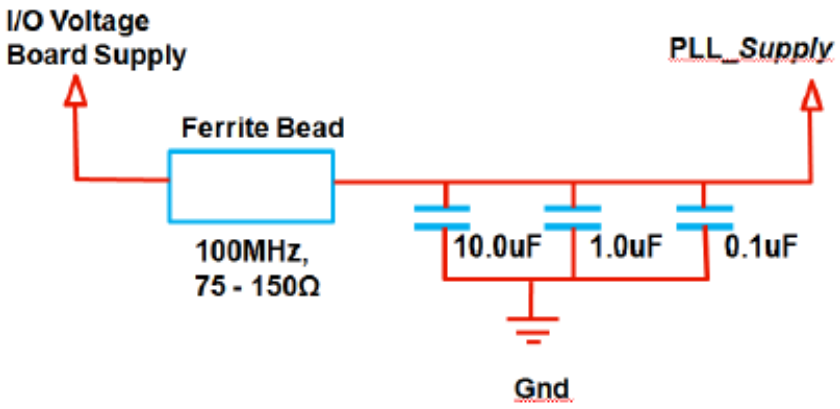

Figure 3. Example Filter Network for PLL Supply

References

[1] *ADSP-21844/ADSP-21846/ADSP-SC844/ADSP-SC846 High Performance SHARC-FX DSP Core With Arm-Based Connectivity/Security Preliminary Data Sheet. Rev PrD, April 2026. Analog Devices, Inc.*

[2] *ADSP-2159x/SC59x Board Design Guidelines for Dynamic Memory Controller (EE-434). Rev 4, June 2026. Analog Devices, Inc.*

Document History

Revision	Description
Rev 1 – June 22, 2026 *by Shivakumar Puran, Manoj Chitneedi*	Initial Release