AN-1441
APPLICATION NOTE

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A Pseudorandom Binary Sequence Calibration on the LVDS Interface of the AD9361

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INTRODUCTION

The AD9361 is a high performance, highly integrated, radio frequency (RF) Agile Transceiver™, designed for use in 3G and 4G applications. The programmability and wideband capability of the AD9361, especially its channel bandwidth ranging from less than 200 kHz to 56 MHz with low power consumption, make it ideal for a broad range of transceiver applications. The AD9361 is recommended for use in new designs for small cell applications where a wide bandwidth is necessary to support multicarrier applications where the carriers must be contiguous.

To support wide bandwidth, factors such as the transmitter (Tx) output linearity, local oscillator (LO) leakage, and the low voltage differential signaling (LVDS) interface must be considered. This application note mainly discusses the LVDS interface that is necessary to support a 56 MHz bandwidth. Figure 1 shows the connection between the AD9361 and the custom application specific integrated circuits (ASICs) and field programmable gate arrays (FPGAs) with an LVDS interface. The interface details are discussed in the AD9361 data sheet. This application note focuses on a pseudorandom binary sequence (PRBS) calibration method to make this interface more reliable over process and temperature variations.

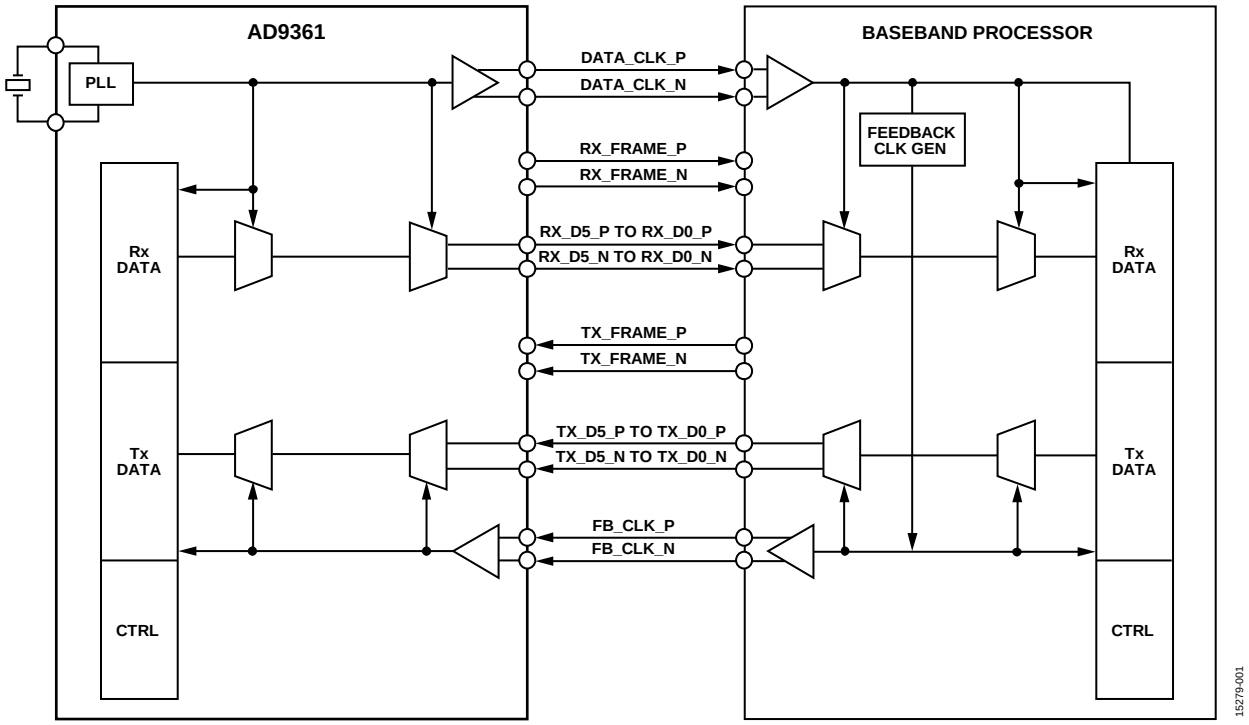

Figure 1. AD9361 Datapath in LVDS Mode

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REVISION HISTORY

4/2018—Revision 0: Initial Version

ISSUE DESCRIPTION

Note that for the purposes of this application note, all references to RX_Dx (x = 0 to 5), TX_Dx (x = 0 to 5), DATA_CLK, RX_FRAME, TX_FRAME, and FB_CLK are referring to signals, only. The RX_Dx signal is the signal on the RX_Dx_P and the RX_Dx_N pins. The TX_Dx signal is the differential signal on the TX_Dx_P pins and the TX_Dx_N pins. The DATA_CLK signal is the differential signal on the DATA_CLK_P pins and DATA_CLK_N pins. The RX_FRAME signal is the differential signal on the RX_FRAME_P pins and RX_FRAME_N pins. The TX_FRAME signal is the differential signal on the TX_FRAME_P pins and TX_FRAME_N pins, and FB_CLK is the differential signal on the FB_CLK_P and FB_CLK_N pins.

LVDS TIMING PARAMETERS

To support a 56 MHz bandwidth, the I/Q data rates on the AD9361 must be set to the maximum value of 61.44 MSPS. For 2T2R operation, the DATA_CLK signal must run at 4× the I/Q rates, 245.76 MHz. The timing constraints for the LVDS data buses at this rate are shown in Table 1.

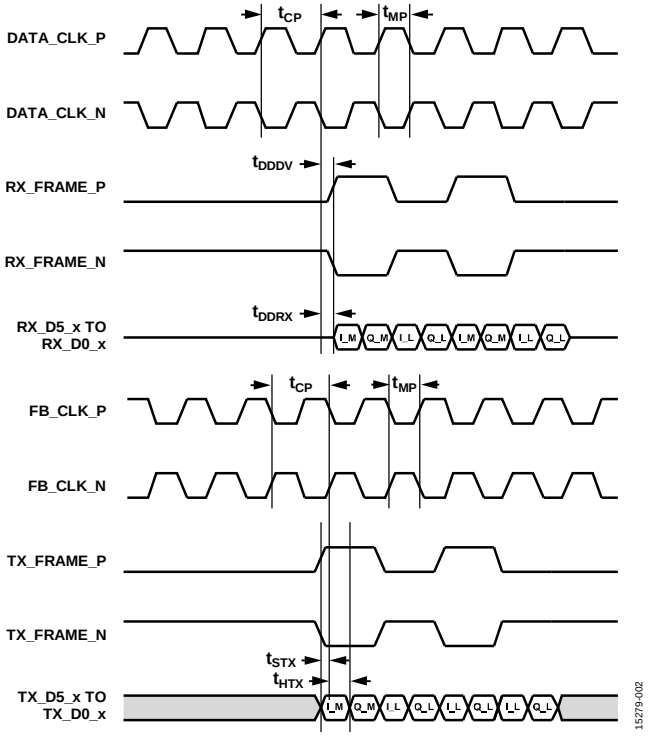

Figure 2. Data Port Timing Parameter Diagram—LVDS Bus Configuration (Where x Indicates the P and N Pins)

IMPACT TO THE CONNECTION WITH THE BASEBAND PROCESSOR

When the clock rate runs at 245.76 MHz, the cycle time of the DATA_CLK is 4.069 ns, and the minimum pulse width is 45% of the duty cycle, approximately 1.83 ns, according to Table 1. Compared with this pulse width, the delays (t_{DDRX} and t_{DDDV}) from the DATA_CLK signal to RX_D5 to RX_D0 signals, or the RX_FRAME signal are at a maximum of 1.25 ns.

Figure 2 illustrates the timing diagram in the AD9361.

Figure 3 illustrates the timing diagram in the baseband processor.

In Figure 3, t_{TDD} is the total delay difference that includes t_{DDRX} in the AD9361 (1.25 ns), the path delay difference that the data propagates through the printed circuit board (PCB) and the delay difference similar to t_{DDRX} in the baseband processor device. The value is larger than 1.25 ns for worst cases. For example, assuming is 1.5 ns, the time left for the data to set up (t_{ST}) and hold (t_{HT}) is only 0.33 ns, which is challenging (see Figure 3), because even if the timing is met on the bench at one temperature, it is difficult to maintain reliability over process and temperature variations.

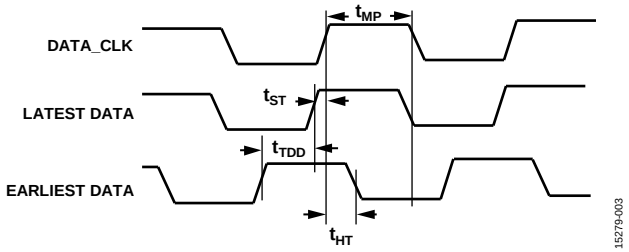

Figure 3. Timing Diagram in the Baseband Processor

To make this interface workable at 245.76 MHz, a calibration is recommended to correct the delay difference (t_{TDD}) between the AD9361 and the baseband processor.

Table 1. LVDS Timing Parameters Shown in Figure 2

Parameter	Min	Typ	Max	Unit	Description
t_{CP}	4.069			ns	DATA_CLK cycle time (clock period)
t_{MP}	45% of t_{CP}		55% of t_{CP}		DATA_CLK signal and FB_CLK signal high and/or low minimum pulse width (including effects of duty cycle distortion, period jitter, cycle to cycle jitter and half period jitter)
t_{STX}	1			ns	TX_D5 to TX_D0 and TX_FRAME signals setup time to FB_CLK signal falling edge at the AD9361 inputs
t_{HTX}	0			ns	TX_D5 to TX_D0 and TX_FRAME signals hold time from FB_CLK signal falling edge at the AD9361 inputs
t_{DDRX}	0.25		1.25	ns	Delay from DATA_CLK to RX_D5 to RX_D0 output signals
t_{DDDV}	0.25		1.25	ns	Delay from DATA_CLK signal to RX_FRAME signal

PRBS CALIBRATION DETAIL

DELAY VARIATION TEST RESULTS

Figure 4 shows the delay variation over the six RX_D0 to RX_D5 pairs and RX_FRAME from DATA_CLK on 300 devices. These digital signals have very different delay values from one another. The largest delay is close to 1.2 ns; however, the shortest delay is only 0.3 ns, and the difference can be 0.9 ns.

DELAY COMPENSATION IN THE BASEBAND PROCESSOR

Figure 4 demonstrates another phenomenon, where, for example, the largest delay mostly occurs on the RX_D4, which is close to 1.2 ns; however, on the RX_D1, the delay is only around 0.7 ns maximum. The difference between the RX_D4 and the RX_D1 is 0.5 ns; therefore, it is preferable to compensate 0.5 ns delay on the RX_D1, then the RX_D4 can be aligned with the RX_D1. This method can be extended to other RX_D5 to RX_D0 pairs and the RX_FRAME, as well as TX_D5 to TX_D0.

For example, if these compensations can be made in the baseband processor separately to each RX_D5 to RX_D0 with higher accuracy, according to Figure 4, which shows a delay correction of −500 ps made to RX_D5 and RX_D4, and a delay correction of −200 ps made to RX_D3, RX_D2 and RX_D0, the results as shown in Figure 5 are possible. The delays are more concentrated between 0.2 ns and 0.7 ns, and the performance is greatly improved.

The calibration can be adjusted on each device; therefore, it is more meaningful to investigate the delay difference between the RX_D5 to RX_D0 pairs and the DATA_CLK on a single AD9361 device. In Figure 6, the blue bars show the distribution of this kind of delay difference over 300 devices without any compensations. The delay difference on most devices is centralized at 0.5 ns, and 0.7 ns maximum. Adopting the same compensations described in the previous paragraph, the distribution moves to a lower delay difference, shown with green bars in Figure 6. The maximum delay difference is 0.3 ns, which is improved by 0.4 ns.

DELAY COMPENSATION IN THE AD9361

The baseband processor may not be able to correct the delay difference via the RX_D5 to RX_D0, or cannot make the delay compensation at all. A solution to this problem is to compensate in the AD9361 using Register 0x006 for Rx and Register 0x007 for Tx to tune the relative delay between RX_D5 to RX_D0 and the DATA_CLK signal (or TX_D5 to TX_D0 and the FB_CLK signal) with approximately 0.3 ns per least significant bit (LSB) accuracy. Note that this delay affects all data pairs with the same value. The AD9361 cannot tune the delay on the data pairs individually. However, this kind of compensation still makes the calibration workable. Figure 7 shows the results when a 300 ps delay is corrected in Register 0x006 of the AD9361. The results shown in Figure 7 show that the delay difference mainly distributes between 0.1 ns and 0.4 ns, and the largest delay is reduced to 0.4 ns, which gives the timing of t_{ST} + t_{HT} (in Figure 3) more margin in the baseband processor (around 1.4 ns), which guarantees the reliability over process and temperature variations.

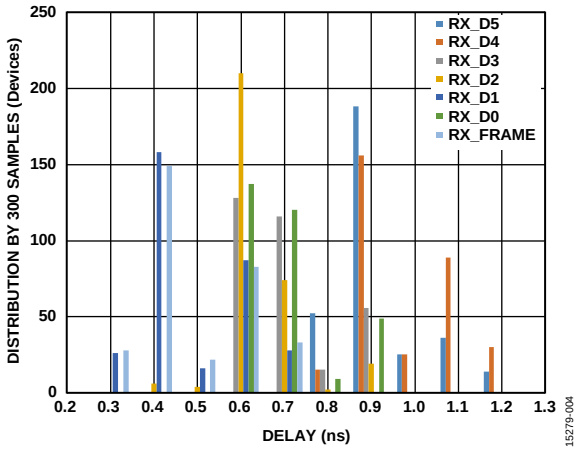

Figure 4. Delay Distribution on the RX_DATA Signal and the RX_FRAME Signal from the DATA_CLK Signal

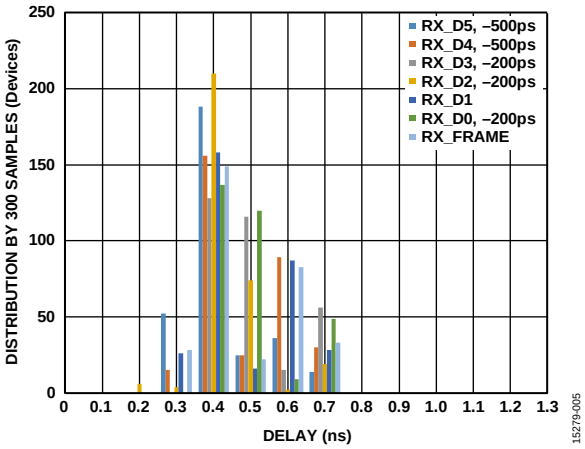

Figure 5. Delay Distribution after Correction

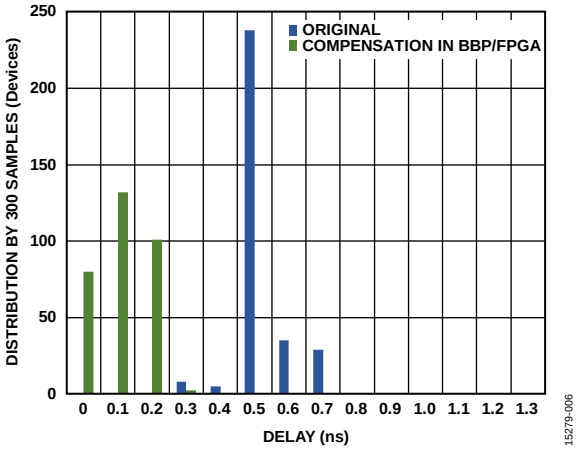

Figure 6. Distribution of Delay Difference on Single Device

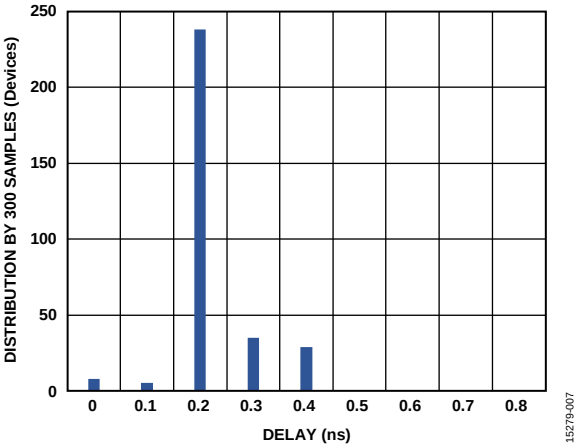

Figure 7. Distribution of Delay Difference with Delay Correction in the AD9361

PRBS CALIBRATION

A PRBS generator integrated in the AD9361 provides a method to decide how much delay compensation is required. This PRBS can be injected into the interface of the AD9361 and transmitted to the baseband processor. After the baseband processor receives this known sequence, a PRBS checker can be implemented to calculate the bit error rate (BER). If no errors occur on the received PRBS, the interface works correctly. Otherwise, tune the delay compensation blocks in the AD9361 or the baseband processor until the BER is reduced below the desired threshold.

The AD9361 has a 16-stage, 14-tap PRBS generator that uses the 16th-order polynomial shown in the following equation.

$$G(x) = x^{16} + x^{15} + x^{14} + x^{13} + x^{12} + x^{11} + x^{10} + x^{9} + x^{8} + x^{7} + x^{6} + x^{5} + x^{3} + x^{2} + 1$$

The detailed description of the PRBS generation and polynomial equation refers to the AD9361 register maps, Register 0x3F4.

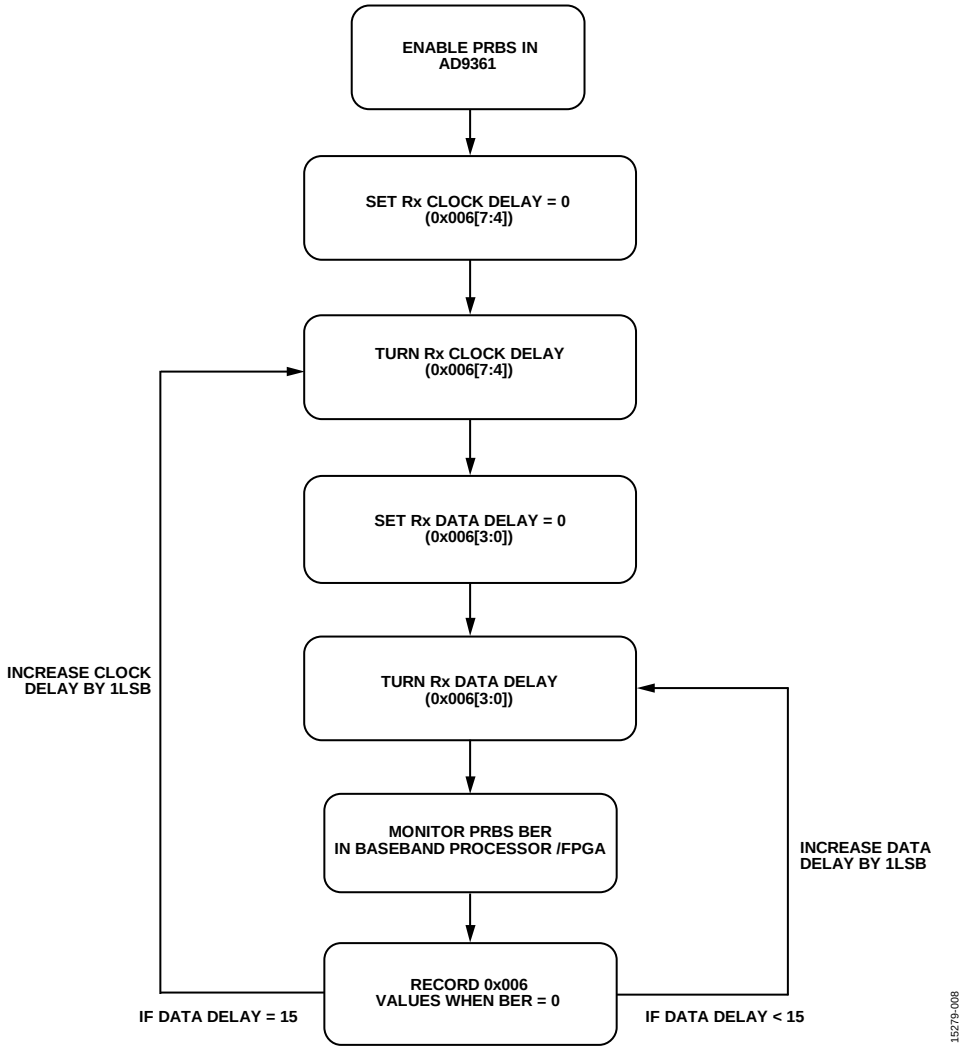

Figure 8. Calibration Sequence

Following the aforementioned calibration sequence shown in Figure 8, a matrix can be produced as shown in Table 2. In Table 2, P indicates that the PRBS test passes and F indicates a failure. In this example, the value of Register 0x006 can be 0x96, 0xA7, 0xB8, 0xC9, or 0xDA

After selecting the appropriate setting for receiver (Rx) delay on Register 0x006, the same method and sequence can be used to run the calibration routine on the Tx LVDS path. This time, when calibrating the Tx LVDS path, a pseudorandom binary sequence can be generated in the baseband processor and transmitted to the Tx interface of the AD9361. In the AD9361, an internal circuit can loop the TX_D5 to TX_D0 to the RX_D5 to RX_D0 path and then transmit the data back to the baseband processor, where a PRBS checker makes the comparison with its original sequence and determines how to tune the delay in Register 0x007 to achieve a similar matrix as shown in Table 2.

Table 2. Calibration Matrix—IQ Data Rates: 61.44 MSPS[1]

	Register 0x006[3:0] Bit Values															
Register 0x006[7:4] Bit Values	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**a**	**b**	**c**	**d**	**e**	**f**
0	P	F	F	F	F	F	F	F	F	F	P	P	P	F	F	F
1	P	F	F	F	F	F	F	F	F	F	F	F	F	F	P	P
2	P	P	F	F	F	F	F	F	F	F	F	F	F	F	F	P
3	P	P	P	F	F	F	F	F	F	F	F	F	F	F	F	F
4	P	P	P	P	F	F	F	F	F	F	F	F	F	F	F	F
5	F	P	P	P	P	F	F	F	F	F	F	F	F	F	F	F
6	F	P	P	P	P	P	F	F	F	F	F	F	F	F	F	F
7	F	F	P	P	P	P	P	F	F	F	F	F	F	F	F	F
8	F	F	F	F	P	P	P	P	F	F	F	F	F	F	F	F
9	F	F	F	F	P	P	P[2]	P	P	F	F	F	F	F	F	F
a	F	F	F	F	F	P	P	P[2]	P	P	F	F	F	F	F	F
b	F	F	F	F	F	F	P	P	P[2]	P	P	F	F	F	F	F
c	F	F	F	F	F	F	F	P	P	P[2]	P	P	F	F	F	F
d	F	F	F	F	F	F	F	F	P	P	P[2]	P	P	F	F	F
e	F	F	F	F	F	F	F	F	F	P	P	P	P	P	F	F
f	F	F	F	F	F	F	F	F	F	F	P	P	P	P	P	F

[1] P = PRBS test passes and F = PRBS test fails.
[2] Best value for the delay setting. These values have at least two LSBs (around 0.6 ns) of protection margin in both directions, which is typically enough margin for the process variation and temperature range variation

CONCLUSION

In this document, a PRBS calibration on the LVDS path delay is introduced to support a 245.76 MHz data clock (56 MHz band-width maximum). Consequently, when the calibration is implemented on the Rx data, the delay variation on the data pairs is dramatically improved down to 0.3 ns (compensation in the baseband processor) or 0.4 ns (compensation in the AD9361).

Both compen-sations make the high speed LVDS interface work with margins to overcome the temperature and process variations. This method is effective for Tx data delay calibration as well.

One example on the AD9361 is shown in this application note, which verifies that the calibration sequence is workable, and its implementation is used in mass production customer systems.

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