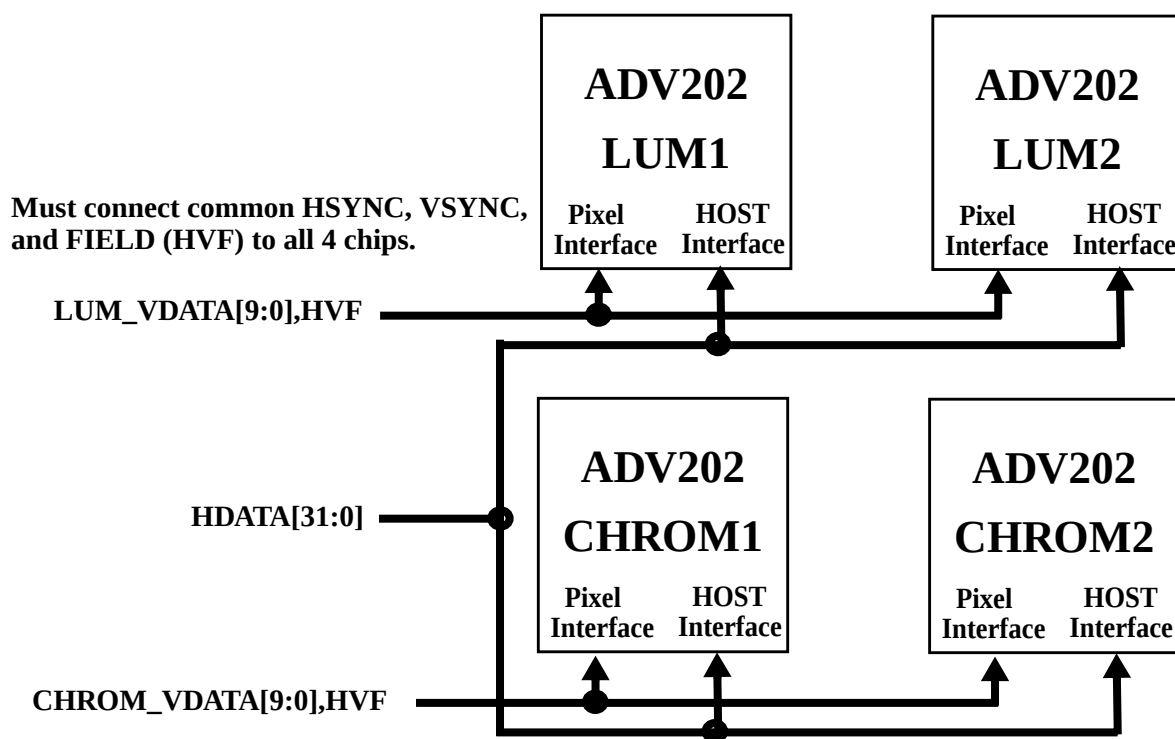


Recommended HD Architectures using 4 ADV202 Chips

OVERVIEW

This document provides a recommended architectures for implementing HD JPEG2000 Capture/Playback systems that require 4 ADV202 chips in order to achieve the highest possible level of performance. For each of these architectures, it is assumed that the Luminance and Chrominance pixel interfaces are separate 10-bit buses (or 8-bit buses), and each is sampled at 74.25 MHz. Thus, the chip configuration can be illustrated as such:

FIGURE 1. Diagram of 4-chip ADV202 Configuration

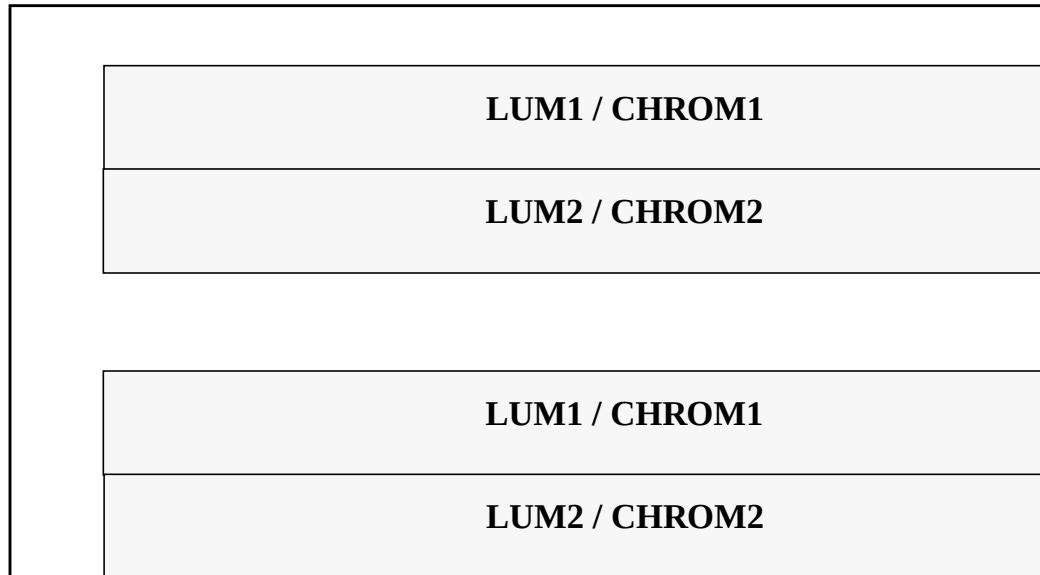


In this configuration, there are two possible methods for configuring the capture: (1) Multiple Tiles with Single Precinct per Image, or (2) Single Tile with Multiple Precincts per Image. Within these two main configuration methods, there are different recommended settings for Progressive vs. Interlaced Video. For simplicity, this document will describe these settings for each of these 4 possible combinations. For each of these configurations, the custom VFORMAT mode (0x04) should be used as described in the User Guide. When using this mode, the Pixel Interface (PI) registers must be written during the Initialization procedure. See the User Guide for details.

Multiple Tiles with Single Precinct per Image for 1080i

This mode should only be used for Lossless or near-Lossless (i.e. high bitrate) applications as tiling artifacts may occur for compression ratios larger than 15:1. The tiles for each field are 1920x270, and are assigned as follows:

FIGURE 2. Video Timing for Multiple Tiles with Single Precinct for 1080i video



The PI registers for all ADV202 chips should be written as follows (assuming 8-bit pixel samples):

TABLE 1. PI Settings for Multiple Tiles with Single Precinct for 1080i video

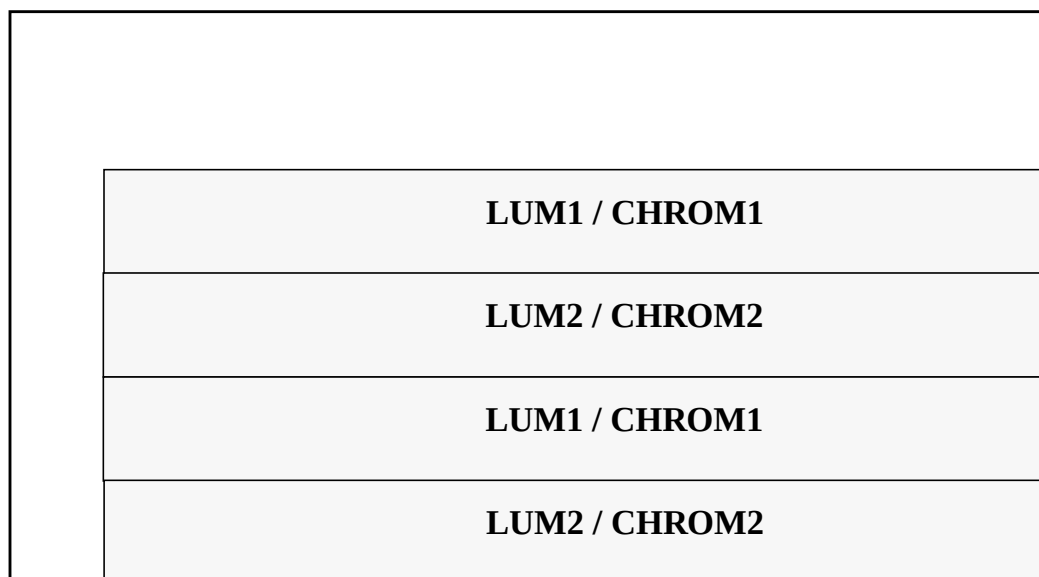
PI REGISTER	LUM1	LUM2	CHROM1	CHROM2
PMODE	0x0004	0x0004	0x0007	0x0007
XTOT	0x0898	0x0898	0x0898	0x0898
YTOT	0x0465	0x0465	0x0465	0x0465
FIELD0_START	0x0003	0x0003	0x0003	0x0003
FIELD1_START	0x0235	0x0235	0x0235	0x0235
FIELD0_VID_START	0x0017	0x0125	0x0017	0x0125
FIELD1_VID_START	0x024a	0x0358	0x024a	0x0358
FIELD0_VID_END	0x0124	0x0232	0x0124	0x0232
FIELD1_VID_END	0x0357	0x0465	0x0357	0x0465
PIXEL_START	0x0001	0x0001	0x0001	0x0001
PIXEL_END	0x0780	0x0780	0x0780	0x0780
PMODE2	0x0039	0x0039	0x0039	0x0039
VMODE (ENCODE)	0x0006	0x0006	0x0006	0x0006
VMODE DECODE)	0x0004**	0x0004	0x0004	0x0004

** The LUM1 chip could be setup as a Master for Decode by setting it's VMODE register to 0x0005, and thus can generate the HVF signals for the other 3 chips. Otherwise, the HVF signals must be generated externally.

Multiple Tiles with Single Precinct per Image for 1080p

This mode should only be used for Lossless or near-Lossless (i.e. high bitrate) applications as tiling artifacts may occur for compression ratios larger than 15:1. The tiles for each field are 1920x270, and are assigned as follows:

FIGURE 3. Video Timing for Multiple Tiles with Single Precinct for 1080p video



The PI registers for all ADV202 chips should be written as follows (assuming 8-bit pixel samples):

TABLE 2. PI Settings for Multiple Tiles with Single Precinct for 1080p video

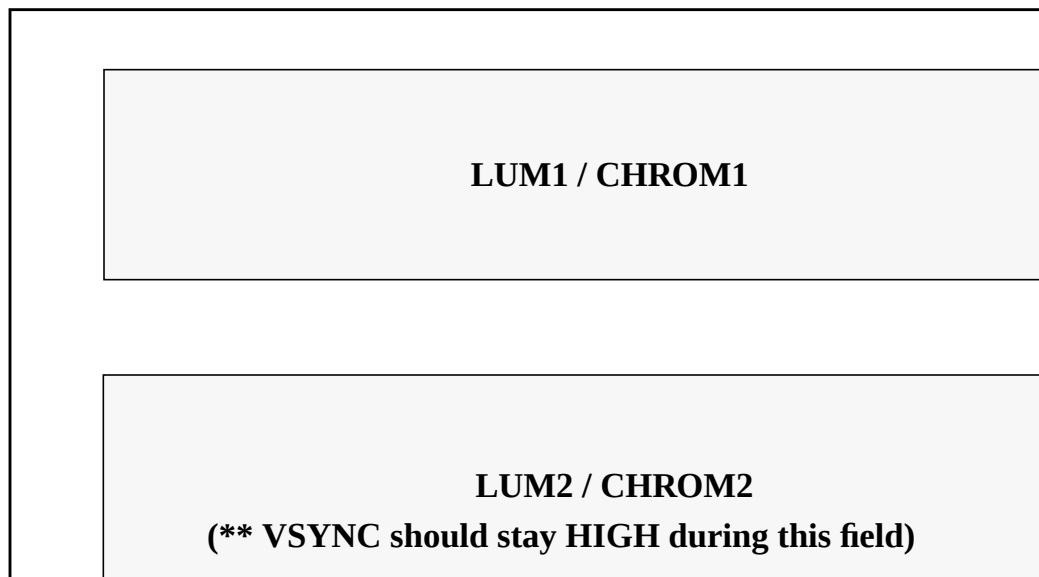
PI REGISTER	LUM1	LUM2	CHROM1	CHROM2
PMODE	0x0004	0x0004	0x0007	0x0007
XTOT	0x0898	0x0898	0x0898	0x0898
YTOT	0x0465	0x0465	0x0465	0x0465
FIELD0_START	0x0003	0x0003	0x0003	0x0003
FIELD1_START	0x0235	0x0235	0x0235	0x0235
FIELD0_VID_START	0x002e	0x013c	0x002e	0x013c
FIELD1_VID_START	0x024a	0x0358	0x024a	0x0358
FIELD0_VID_END	0x013b	0x0249	0x013b	0x0249
FIELD1_VID_END	0x0357	0x0465	0x0357	0x0465
PIXEL_START	0x0001	0x0001	0x0001	0x0001
PIXEL_END	0x0780	0x0780	0x0780	0x0780
PMODE2	0x0039	0x0039	0x0039	0x0039
VMODE (ENCODE)	0x0006	0x0006	0x0006	0x0006
VMODE DECODE)	0x0004**	0x0004	0x0004	0x0004

** The LUM1 chip could be setup as a Master for Decode by setting it's VMODE register to 0x0005, and thus can generate the HVF signals for the other 3 chips. Otherwise, the HVF signals must be generated externally.

Single Tile with Multiple Precincts per Image for 1080i

This mode should can be used for Lossless or Lossy applications, but relies on special firmware that is still being developed which will break the image into precincts. In this configuration, each chip only processes one field of the frame, and thus is setup as a progressive mode. Also note that VSYNC must be modified for this mode such that it does not pulse during the second field (i.e. must be suppressed during field 2):

FIGURE 4. Video Timing for Single Tile with Multiple Precincts for 1080i video



The PI registers for all ADV202 chips should be written as follows (assuming 8-bit pixel samples):

TABLE 3. PI Settings for Single Tile with Multiple Precincts for 1080i video

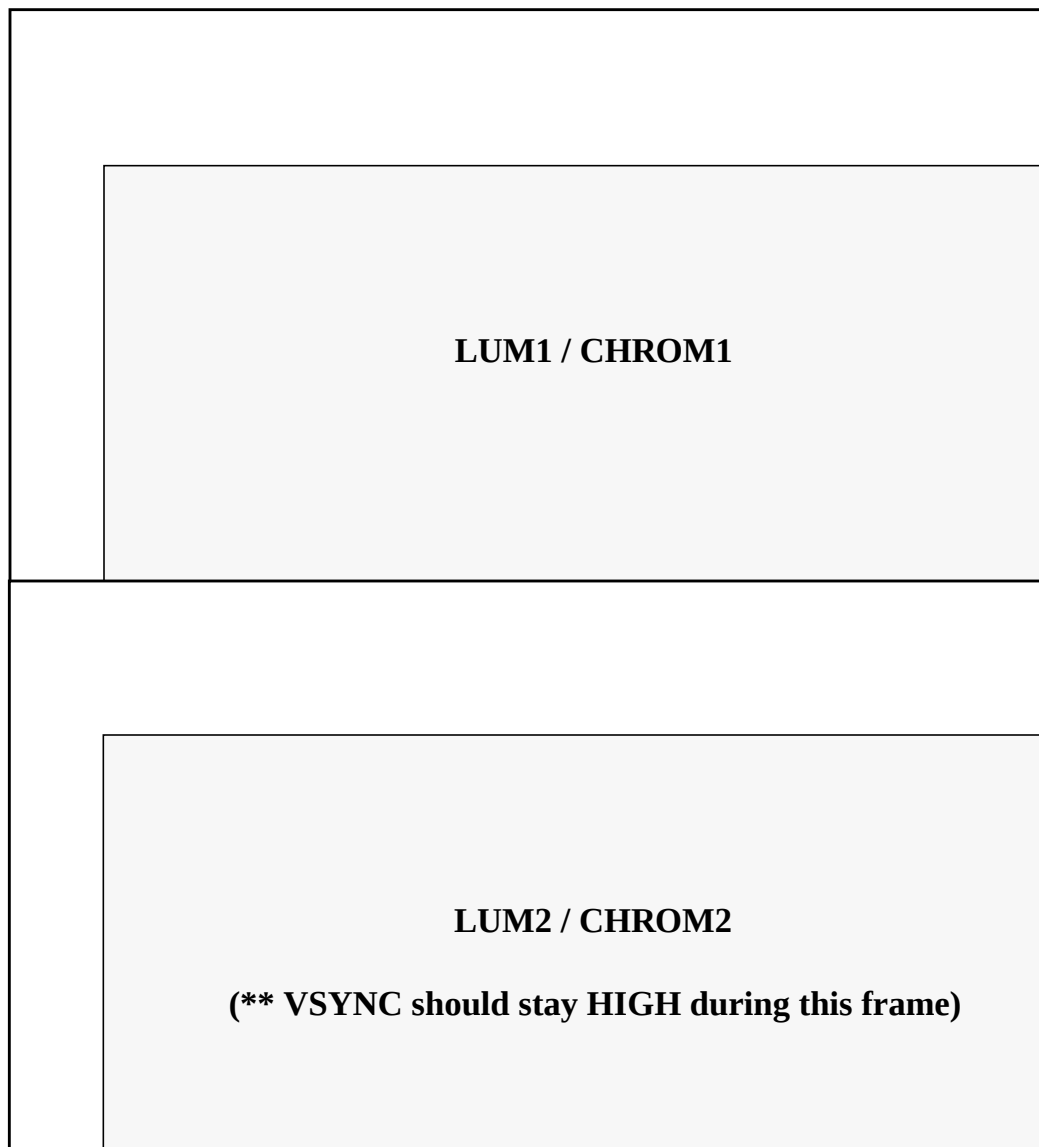
PI REGISTER	LUM1	LUM2	CHROM1	CHROM2
PMODE	0x0004	0x0004	0x0007	0x0007
XTOT	0x0898	0x0898	0x0898	0x0898
YTOT	0x0465	0x0465	0x0465	0x0465
FIELD0_START	0x0001	0x0001	0x0001	0x0001
FIELD1_START	0x0000	0x0000	0x0000	0x0000
FIELD0_VID_START	0x0017	0x024a	0x0017	0x024a
FIELD1_VID_START	0x0000	0x0000	0x0000	0x0000
FIELD0_VID_END	0x0232	0x0465	0x0232	0x0465
FIELD1_VID_END	0x0000	0x0000	0x0000	0x0000
PIXEL_START	0x0001	0x0001	0x0001	0x0001
PIXEL_END	0x0780	0x0780	0x0780	0x0780
PMODE2	0x0039	0x0039	0x0039	0x0039
VMODE (ENCODE)	0x0086	0x0086	0x0086	0x0086
VMODE DECODE)	0x0084**	0x0084	0x0084	0x0084

** The LUM1 chip could be setup as a Master for Decode by setting it's VMODE register to 0x0085, and thus can generate the HVF signals for the other 3 chips. Otherwise, the HVF signals must be generated externally.

Single Tile with Multiple Precincts per Image for 1080p

This mode should can be used for Lossless or Lossy applications, but relies on special firmware that is still being developed. In this configuration, each chip only processes one frame out of every two frames, and thus is setup as a progressive mode, but with YTOT being 2250 rather than 1125. Again, VSYNC must be modified such that it does not go LOW during the 2nd frame:

FIGURE 5. Video Timing for Single Tile with Multiple Precincts for 1080p video



The PI registers for all ADV202 chips should be written as follows (assuming 8-bit pixel samples):

TABLE 4. PI Settings for Single Tile with Multiple Precincts for 1080p video

PI REGISTER	LUM1	LUM2	CHROM1	CHROM2
PMODE	0x0004	0x0004	0x0007	0x0007
XTOT	0x0898	0x0898	0x0898	0x0898
YTOT	0x08ca	0x08ca	0x08ca	0x08ca
FIELD0_START	0x0001	0x0001	0x0001	0x0001
FIELD1_START	0x0000	0x0000	0x0000	0x0000
FIELD0_VID_START	0x002e	0x0493	0x002e	0x0493
FIELD1_VID_START	0x0000	0x0000	0x0000	0x0000
FIELD0_VID_END	0x0465	0x08ca	0x0465	0x08ca
FIELD1_VID_END	0x0000	0x0000	0x0000	0x0000
PIXEL_START	0x0001	0x0001	0x0001	0x0001
PIXEL_END	0x0780	0x0780	0x0780	0x0780
PMODE2	0x0039	0x0039	0x0039	0x0039
VMODE (ENCODE)	0x0086	0x0086	0x0086	0x0086
VMODE DECODE)	0x0084**	0x0084	0x0084	0x0084

** The LUM1 chip could be setup as a Master for Decode by setting it's VMODE register to 0x0085, and thus can generate the HVF signals for the other 3 chips. Otherwise, the HVF signals must be generated externally.

Multi-Chip Synchronization

This will work just as described in the Application Note "ADV202_multichip_application", but must be extended for 4 chips instead of 2. The SCOMM[5] pin of each ADV202 must be connected together such that they all are enabled simultaneously. The SWIRQ1 interrupt must be enabled in the EIRQIE register during initialization, and when all 4 chips assert this interrupt, the SCOMM[5] pins can all be set HIGH.