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## Technical Notes on using Analog Devices' DSP components and development tools

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### ***Booting the ADSP-21065L from an EPROM using VisualDSP 4.1***

March 23, 2000 (bk)

This document does not describe the basic boot procedure. Only 21065L specific issues will be discussed. For a more general description, please find the EE-Notes 56, 72 and 77.

#### **1) A23: Documentation Change**

The following sentence is mentioned by the Anomaly Sheet 08/99:

*"To ensure the proper number of wait states are inserted for DMAs with the SYSCON Bit BSO set, Bit A23 in the external DMA Index Register EIEPx must be set."*

The first booting DMA sequence enabled by the BSEL input pin is not affected by this documentation change: So, the first 256 instructions are loaded properly, but the boot loader must set Bit A23 for all further DMAs.

This will limit the maximal linear byte address space to 8 MByte (= 64 MBit), but shouldn't be a real restriction.

This documentation change does not require user intervention. It is completely handled by the VisualDSP 4.1 boot loader.

#### **2) Anomaly: Wait States during PROM Boot (Rev. 0.0 only)**

Revision 0.0 initializes the WAIT register to 0x200D.6B5A. This causes the processor to wait for the external ACKnowledge signal only and to disregard the internal wait-state generator.

In other words: If no external wait-state generator is used, revision 0.0 may be booted from a zero wait-state (!) device only.

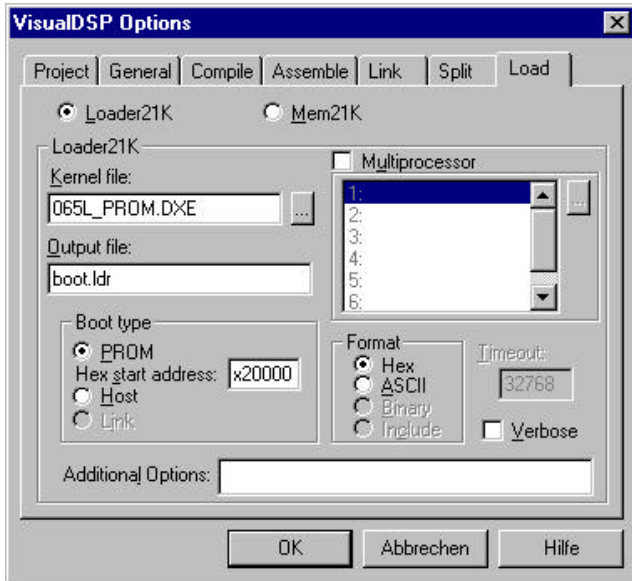
All newer revisions reset WAIT to 0x21AD.6B5A. Please note that the user's manual is still confusing there: Pages 5-55 and E-111 show the 0.0 reset value. Figures 5-16 and E-20 show the correct reset value for the revisions 0.1, 0.2 and 0.3.

#### **3) Differences between the Revisions: Offset of 0x20000**

Remember the ADSP-21060/62/61 devices: the external memory space starts from address 0x40.0000 there. Therefore after reset the external port DMA index register EI6 is set to 0x40.0000 for EPROM booting. Because of that the address bit A22 is always set and the maximal boot memory space is limited to 4 MByte (= 32 MBit).

The 21065L's external memory is mapped from 0x02.0000 on. Chip revisions 0.0 and 0.1 use the same technique as the other SHARCs and initialize the external port DMA index register EIEP0 to 0x02.0000. A17 is set and the boot memory space is limited to 128 kByte (= 1 MBit) max, which may be not enough for some applications.

If someone would try to connect a 2 MBit EPROM and VisualDSP would not care about, the 21065L would read the loader kernel (= 256 x 6 Bytes) from address 0x02.0000. The boot loader would continue to read bytes from 0x0600.



To provide a workaround the boot kernel of VisualDSP 4.1 sets the address line A17 in EIEP0 for all byte DMA reads<sup>1)</sup>. EPROMs greater than 1 MBit may be used, but then the entire boot image must start from 0x02.0000 on. Therefore an offset of 0x02.0000 has to be added when compiling the project. Just specify a “Hex Start Address” of 0x02.0000 in the VisualDSP “Load” Property Page.

In most of cases the output file will have the Intel Hex format. A normal data set is branded by the “00” type qualifier there. It features 16 address bits only.

```
# bytes  address  type      data
: 20   0020   00      00043E0600..
```

Therefore additional address information is required. Beside other enhancements the Intel Hex format features the “04” command, which specifies

additional address bits A31..A16 valid for all the following data sets. The first line of the generated loader file looks like:

```
          type      address  checksum
: 02  0000   04      0002    F8
```

Unfortunately not all of the EPROM programmers and HEX-to-Binary Converter utilities do support this format enhancements, but they will feature other (manual) techniques to specify the required offset of 0x02.0000.

Chip revisions 0.2 and 0.3 work different to avoid the need of workarounds. There, the EPROM is mapped to byte address zero and EIEP0 is cleared after reset.

The boot loader must not set Bit A17 when it runs on chips with revision 0.2 or greater. It determinates the chip revision at run-time by the MODE2 register to avoid the need of different loader versions.

The 21065L’s EZ-LAB comes with a 2 MBit EPROM. To support all of the chip revisions the whole boot image is stored twice in this EPROM: at address 0x00.0000 and at 0x02.0000. A 1 MBit EPROM would not be a bad choice, of course.

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<sup>1)</sup> *Setting the Bit A17 is not the right way to solve that problem. A real addition by 0x02.0000 would be more decent. In fact this little bug of the VisualDSP 4.1 boot loader may cause errors in huge dual-processor designs.*

#### **4) Simulating the Boot Sequence**

The VisualDSP 4.1 Simulator features the possibility to simulate the entire boot sequence by the menu “Settings->Load Sim Loader->Boot from

PROM”. After selecting a loader file the “Debug->Reset” command starts the boot.

Another menu command is very helpful here: “File->Load Symbols->065L\_prom.dxe”.

Unfortunately the several workarounds required for the real 21065Ls make the simulator fail.

Before you are going to let the simulator run, please set a breakpoint on all instructions that write to the memory-mapped register EIEP0 (= DM 0x45).

There are two such instructions in the original boot loader at address 0x805E and 0x8067.

When the simulator halts on that breakpoints, please clear bit 23 and bit 31 (but not bit 17) manually in the registers USTAT1/R3 before they are copied into EIEP0.

### **5) SDRAM Controller Initialization**

Normally, there is no need to modify the original boot loader. SDRAM Controller Initialization is the famous exception.

Whenever SDRAM is connected to the ADSP-21065L and the data/code placed in the SDRAM has to be initialized/zeroed by the boot loader, the SDRAM controller has to be set up before the DSP may access the SDRAM.

The loader’s source code can be found in the VisualDSP subdirectory “ldr”. To change the loader a new project has to be created, that includes the files “065L\_ldr.ldf” and “065L\_prom.asm”. Project type is “DSP Executable file”.

The original source code has already prepared a piece of code that initializes the SDRAM controller for the SDRAM type featured by the EZ-LAB.

These view instructions are inactivated by a preprocessor statement (#if 0 ... #endif).

Just remove these preprocessor parentheses to activate the instruction between them, but please note that other SDRAM types need different initialization sequences.