



ADSP-2156x Board Design Guidelines for Dynamic Memory Controller

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Introduction

This EE-note provides board design guidelines for interfacing an ADSP-2156x processor to DDR memory and achieving expected performance from its DDR controller. These guidelines should be used in addition to standard board-level design practices.

Placement and General Routing Guidelines

Use the following guidelines when designing PCB stack up, trace routing and component placement:

- Place the ADSP-2156x device and the memory as close as possible to each other while reducing routing length.
 - The ADSP-2156x DMC interface supports only point-to-point design and does not support fly-by topology.
 - Plan the PCB stack-up such that all the DMC signals (address, command and control) have continuous reference planes (ground planes) on an immediately adjacent layer. Ensure that these signals do not travel across splits in the power/ground planes. It is better to increase the distance between the signal and its relevant planes than to implement the “cross split” routing.
 - For better signal integrity, avoid power-plane-to-signal-plane and power-plane-to-power-plane coupling. Strive to minimize this coupling.
- The PCB trace characteristic impedance must be 50 Ω for single-ended signals and 100 Ω for differential signals, with a 5% tolerance.
 - Route all DDR signals as a group in every layer to avoid a mismatch in trace impedance and propagation delay. Keep all grouped signals on the same layer. For example, the DMC_DQ00-07, DMC_LDQS, and DMC_LDQM signals should be routed as a group, in the same layer and having the same ground reference. Changing the ground reference plane can change the trace impedance.
 - To avoid crosstalk, ensure that all DDR signals have center-to-center spacing of at least 3W between DDR signals and 4W to other signals, where W is the trace width.
 - Maintain perpendicularity between DMC signals routing for different DMC signals routed in adjacent layers. This configuration reduces crosstalk, as signals on adjacent layers will not be parallel to each other.
 - Avoid test points on the DDR signals, as they create stubs which can act as EMI sources. Instead, use vias for probing. It is also acceptable to use JEDEC-recommended methods that test vendors offer for diagnostics.

Trace Length-Matching Criteria

The routing of all the DDR interface signals must be length-matched to avoid set-up and hold time violations due to propagation delay.

The length-matching criteria are as follows:

- Match the trace length of all address (DMC_A [nn], DMC_BA[n]) and command (DMC_CKE, DMC_CS[n], DMC_ODT, DMC_RAS, DMC_RESET, DMC_WE) signals within +/- 40 mils relative to the DMC_CK signal.
- Match the trace length of all data (DMC_DQ [nn]) and data mask (DMC_UDM, DMC_LDM) signals within +/- 40 mils relative to their corresponding DQS signal. For example, match the trace length of the lower order data byte (DMC_DQ00 - DMC_DQ07) and the corresponding data mask (DMC_LDM) signals with the lower order strobe (DMC_LDQS) signal.
- Match the trace length of differential signals such as clock (DMC_CK and /DMC_CK) and DQS pairs (DMC_LDQS and /DMC_LDQS, DMC_UDQS and /DMC_UDQS) within +/- 10 mils. For example, match the trace length of the DMC_CK and /DMC_CK signals within +/- 10 mils relative to each other.
- The maximum allowed trace length for DDR signals is 2 inches.

Interface Termination

All of the DDR interface signals without ODT require external termination for improved signal integrity. The DDR3/DDR3L data group signals do not require external termination because they have ODT.

The termination guidelines are as follows:

- Install external series termination resistors on all address and control signals and place them as close as possible to the processor.
- The recommended value of the series termination resistors is 100 Ω . This value can vary based on board routing.
- Select appropriate series termination resistor values, as well as ODT values, based on simulation results of the board.

VTT Termination

Use the following guidelines for VTT termination. These guidelines can differ from vendor to vendor.

- For DDR3/3L, VTT termination is recommended by JEDEC, as this mitigates signal reflection. The primary purpose of a VTT island is to prevent reflections at the memory device. Removing the VTT termination results in signal reflections. The removal can lead to higher than nominal voltages at the memory address or command input pins. It can damage or reduce the lifetime of the memory. Check with the appropriate memory vendor for device-specific information.
- Implement VTT termination for the DMC_CK and /DMC_CK as shown in [Figure 1](#), where RN7 is a resistor pack.

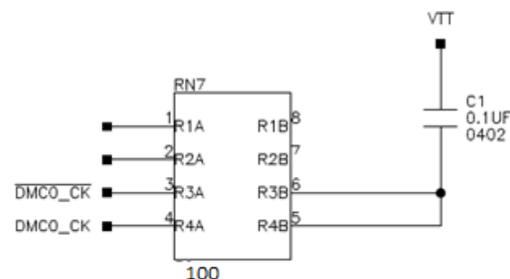


Figure 1: VTT Termination for DMC_CLK

- Place individual power and ground vias from every power and ground pin of the ADSP-2156x processor and the memory device to its associated plane.
- Place decoupling capacitors for the VDD_DMC power rail as close as possible to the actual power pins. This is very important because DDR signal slew rates are aggressive. Placing these capacitors close to the pin is mandatory. Provide dedicated power and ground vias for each decoupling capacitor pin, wherever possible.
- Ideally, the trace length from the power via to the processor pad should not exceed 30 mils. The maximum trace length from each power via to its decoupling capacitor is 60 mils. The maximum trace length from each power via to its power ball pad is 35 mils.
- Placement of the mid-bulk bypass capacitors (~10 μ F) is not critical. They can be placed to accommodate other circuitry with more constrained placement and routing requirements.

DMC_VREF Voltage Supply

DMC_VREF acts as a voltage reference for DDR3/DDR3L data signals and compares the difference between a steady reference voltage (DMC_VREF) and the signal received for identifying the logic. Hence, it is recommended to minimize noise on DMC_VREF.

- Route the DMC_VREF trace at least 40 mil away from high-speed signals and noisy power supply traces.
- Guard traces can be provided around the DMC_VREF trace, if required. Ensure that the

guard traces have sufficient ground vias stitched to the main ground plane.

- Provide adequate decoupling near the DMC_VREF pins of the ADSP-2156x processor, as well as at the memory device.
- Keep the DMC_VREF trace as short as possible, with a width of at least 20 mils.

Recommended ADSP-2156x DMC_VREF Filtering Scheme

Figure 3 shows the RCR filtering scheme on DMC_VREF that is recommended for ADSP-2156x processors. As shown, DMC_VREF0 and DMC_VREF1 can be shorted together.

PCB Placement and Routing Guidelines for the DMC_VREF Filter Network

Use the following guidelines for the DMC_VREF filter network placement:

- Place the recommended RCR network between the DMC_VREF supply paths from the memory to the processor.
- Place the C (100 pF)-R (2 k Ω) portion of the RCR network as close as possible to the ADSP-2156x DMC_VREF pin.
- Use a small package, preferably the 0402 size, for the 100pF capacitor to guarantee a high self-resonant frequency.
- Route the entire RCR network on one layer with no vias in the traces.

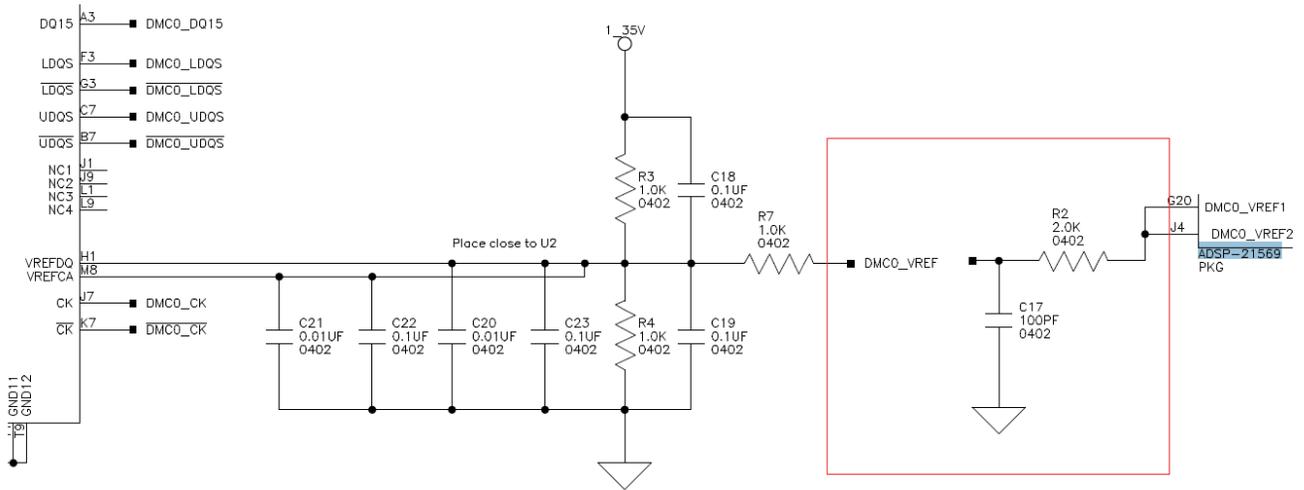


Figure 3: DMC_VREF Filtering Network

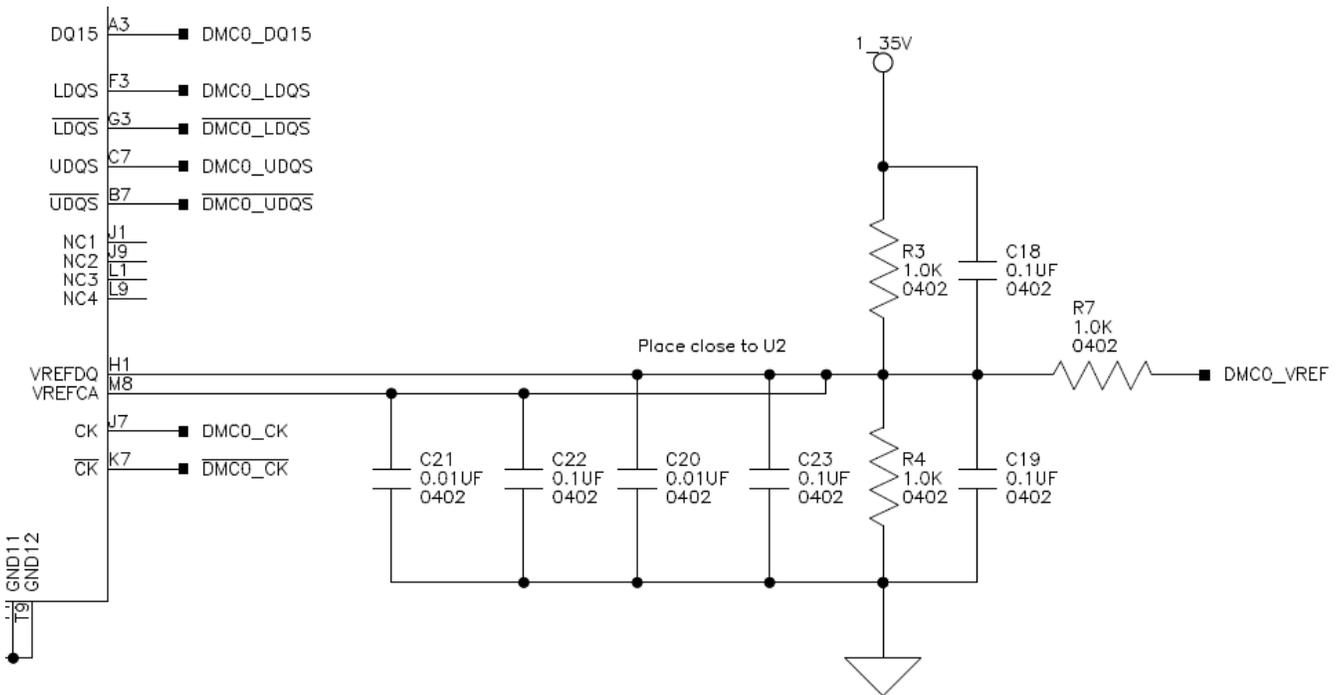


Figure 4: Recommended VREF Supply Circuit

Memory-Side Recommendations for VREF Supply

Use the following guidelines for DMC_VREF supply placement on the memory side. The requirements apply to both DDR3 and DDR3L.

- DDR3 memory has two VREF pins: VREFCA and VREFDQ. VREFCA serves as the reference for clock, address, command, and control signals. VREFDQ serves as the reference for strobe, data, and data mask signals
- VREFCA and VREFDQ can have a common supply source, but should be “STAR” routed and decoupled at the dedicated DRAM pins.

- Place two decoupling capacitors, 0.1 μ F and 0.01 μ F, for each VREF pin (VREFCA and VREFDQ).
- Place the 0.01 μ F capacitor closer to the DRAM pin, followed by the 0.1 μ F capacitor.
- Keep the length from the decoupling capacitor to the DRAM supply pin as short as possible. Maintain the trace width based on the peak current requirement of the DDR. [Figure 4](#) shows the recommended VREF supply circuit for a DDR3 memory device.

References

- [1] *Interfacing DDR3/DDR2/LPDDR Memory to ADSP-SC5xx/215xx Processors (EE-387)*. Rev. 3, April 2018. Analog Devices, Inc.
- [2] *ADZS-21569 EZ-Kit® Schematic*, Rev B, Sep 2017. Analog Devices, Inc.

Document History

Revision	Description
Rev 1 – January 15, 2020 by Sachin-V Kumar	Initial Release