



Processor Comparison Guide (ADSP-BF60x/BF70x vs ADSP-SC58x/2158x)

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Introduction

Beginning with the ADSP-BF60x family of Blackfin® processors, the processor portfolio offered by Analog Devices shares common peripherals and infrastructure blocks. This EE-Note provides a high-level summary of the technology that is common between the ADSP-BF60x and ADSP-BF70x Blackfin processors and the latest ADSP-SC58x/ADSP-2158x SHARC® processors. The intent of this document is to identify where portions of the technology are common and identify any differences in terms of supported features.



For complete information describing use and programming of the architectural blocks and peripherals described herein, please refer to the respective product *Hardware Reference Manuals*^{[1][3][5]} and *Processor Datasheets*^{[2][4][6]}. This document should not be considered as a replacement to this literature.

Infrastructure Blocks

Beginning with the ADSP-BF60x processors, the architecture fabric was modified to accommodate ARM technology as well as Blackfin and SHARC cores, and many of these architectural blocks are identical among all the processors released since the ADSP-BF60x, including the ADSP-BF70x Blackfin processors and the ADSP-SC58x/2158x SHARC processors, as follows:

- Clock Generation Unit (CGU)
- Reset Control Unit (RCU)
- System Event Controller (SEC)
- Fault Management Unit (FMU)
- Trigger Routing Unit (TRU)

While the above architectural blocks are common and unchanged between the processors addressed in this EE-Note, other blocks are common with minor differences or not present on all processors for various reasons, which is covered in the following sections.

Clock Distribution Unit (CDU)

Due to providing support for multiple Phase-Locked Loops (PLLs) in the ADSP-SC58x/2158x processors, the Clock Distribution Unit (CDU) architecture block was introduced to provide fine control to the user as to how clocks are configured and where to route the clocks inside the device. As there is only one PLL in the Blackfin devices, this unit is not available on those products.

System Protection Unit (SPU) and System Memory Protection Unit (SMPU)

The System Protection Unit (SPU) was introduced in the ADSP-BF60x processors, providing the capability to lock down areas of system memory to prevent software from accessing MMR space unexpectedly. The block was carried forward to the ADSP-BF70x processors, but new features were added to support protection associated with the security state of the processor. This implementation was then carried forward to the ADSP-SC58x/2158x processors.

With the security features that were added to the SPU, the System Memory Protection Unit (SMPU) was added to the ADSP-BF70x Blackfin processor to provide the same protection over the memory blocks (protection based on security state). This block was then carried forward to the ADSP-SC58x/2158x processors as well.

Dynamic Power Management (DPM) Block

The Dynamic Power Management (DPM) block introduced in the ADSP-BF60x processors provides the ability to transition to lower-power states and dynamically control whether or not clocks are routed to peripherals (thus saving dynamic power for peripherals that are not being used). The lower-power states are common across the Blackfin processors, so the block was carried forward to the ADSP-BF70x processors; however, the ADSP-SC58x/2158x processors do not support these lower-power states. Therefore, the DPM is only used for enabling/disabling clocks to used/unused peripherals.

System Watchpoint Unit (SWU)

The System Watchpoint Unit (SWU) introduced in the ADSP-BF60x processors provides the ability to monitor transactions across the fabric coming from the various system crossbars (e.g., accesses to a specific MMR). Two modes of operation are supported:

- Watchpoint Mode – looks for an exact match and takes action after a specific number of matches are recognized
- Bandwidth Mode – counts the number of exact match transactions for a defined window of time

This implementation is common between the ADSP-BF60x and ADSP-BF70x Blackfin processors.

With the ADSP-SC58x/2158x SHARC processors, the SWU capabilities were expanded to also look at data rather than just addresses. In addition to the read and write address channels, the read and write data channels' ID, VALID, and READY signals are also monitored, which means looking for a specific data pattern in the transaction is also supported.

Further, scaling was added to the Bandwidth Mode, which allows the SWU to count more transactions by scaling the number of transactions and the number of clock cycles in the bandwidth window (using the CNTn register) by 10,000 or 1000.

System Debug Unit (SDU) and System Debug and Trace Unit (DBG)

On the ADSP-BF60x Blackfin processors, the System Debug Unit (SDU) provides debug access to the connected system. It provides debug host interface support through a JTAG (IEEE-1149.1) interface. In addition to traditional JTAG features, the SDU provides direct access to the processor's system resources to allow highly flexible and non-intrusive debug support.

Starting with the ADSP-BF70x processors (and carrying forward to the ADSP-SC58x/2158x SHARC processors), this architecture block was replaced by the System Debug and Trace Unit (DBG). The DBG is

based on ARM CoreSight™ technology, which is a set of architecture specifications defining debug and trace architecture. The processor featuring the DBG block use CoreSight infrastructure to provide industry-standard debug and trace capabilities.

Architecture Block Feature Summary

[Table 1](#) provides a summary of the architectural blocks described in the previous sections, identifying those common to all and citing feature differences where applicable.

Infrastructure Block Name	ADSP-BF60x	ADSP-BF70x	ADSP-SC58x/ADSP-2158x
CGU	Yes	Yes	Yes
CDU	No	No	Yes
RCU	Yes	Yes	Yes
SPU	Yes	Adds security-based system protection	Same as ADSP-BF70x
SMPU	No	Yes	Yes
DPM	Yes	Yes	No low-power modes
SEC	Yes	Yes	Yes
FMU	Yes	Yes	Yes
TRU	Yes	Yes	Yes
SWU	Yes	Yes	Adds data monitoring capabilities and scaling to Bandwidth Mode
SDU/DBG	SDU	DBG	DBG

Table 1. Summary of Infrastructure Block Features

Peripherals

As was the case with the architecture blocks described above, there are several peripherals that are shared and identical across the products covered by this EE-note:

- UART
- TWI
- CAN
- Counter

[Table 2](#) provides a summary of the peripherals between the ADSP-BF60x/ADSP-BF70x Blackfin processors and the ADSP-SC58x/ADSP-2158x SHARC processors. A “Yes” in the column represents the standard feature set, a “No” means it isn’t applicable, and any other text describes points of differentiation.

Peripheral	ADSP-BF60x	ADSP-BF70x	ADSP-SC58x/ADSP-2158x
DMC	DDR2/LPDDR	DDR2/LPDDR	DDR2/DDR3/LPDDR
L2CTL	Yes	Adds hardware support for L2 SRAM initialization, automatic refresh/scrub, and low-power modes	No write protection support
SMC	Yes	No burst read support	No burst read support
SPORT	Yes	Yes	Yes (Part of DAI0 and DAI1)
SPI	Yes	SPI2 adds support for memory-mapped mode and execute-in-place (XIP) Adds SPI Host Port (HP) support	SPI2 adds support for memory-mapped mode and execute-in-place (XIP)
ACM	4 external triggers	No	1 external trigger
10/100 EMAC	Yes	No	No PTP Support
GEMAC (10/100/1000)	No	No	Yes
USB OTG	Yes	Yes	Dual-USB (one OTG and one device/host) with shared USB_CLKIN and separate PHY
RSI/MSI	MMC version 4.3	Integrated DMA support FIFO SIZE increased to 1024 MMC version 4.41	Same as ADSP-BF70x
Link ports	83 MHz Maximum	No	150 MHz Maximum
ePPI	Up to 24-bit data	Up to 18-bit data	Up to 24-bit data
Timers	Yes	Adds trigger toggle mode	Yes
WDT	Yes	Yes	Yes
HPPWM	Yes	No	PWM dead time individually controlled for each channel
HADC	No	4 channels	8 channels
Crypto Engine	No	32-bit PKTE post-processing	16-bit PKTE post-processing
GP Ports	Yes	Adds TRU Trigger Toggle	Yes

Table 2. Peripheral Summary

Table 3 provides a summary of peripherals/features which are not common between the processors.

Feature	ADSP-BF60x	ADSP-BF70x	ADSP-SC58x/ADSP-2158x
HAE	No	No	Yes
SINC	No	No	Yes
PCG	No	No	Yes
ASRC	No	No	Yes
SPDIF Transceiver	No	No	Yes
FFT Accelerator	No	No	Yes
FIR Accelerator	No	No	Yes
IIR Accelerator	No	No	Yes
MLB	No	No	Yes
PCIe	No	No	Yes
RTC	No	No	Yes
DTCP	No	No	Yes
PVP	Yes	No	No
PIXC	Yes	No	No
Oscillator WDOG	No	No	Yes
TrustZone	No	No	Yes
OTP	No	Yes	Yes

Table 3. Summary of Peripherals/Features Specific to ADSP-SC58x/ADSP-BF60x

Boot ROM

The boot ROM is a small piece of code that executes out of reset to initialize the processor, resolve the application code/data, and commence execution. It is defined by expected system requirements, boot ROM size, and available peripherals. Of the processors discussed in this EE-Note, the ADSP-BF60x processor is the baseline, providing boot support for all of the following peripherals:

- RSI Master
- SPI Master
- SPI Slave
- Link Port Slave
- UART Slave

As the ADSP-BF70x processor does not feature link ports, the Link Port Slave boot mode doesn't exist for these devices. The RSI Master boot mode was also removed, but all the other modes listed above are supported identically. However, the secure boot features were added to all the supported boot modes beginning with the ADSP-BF70x processor.

The ADSP-SC58x/2158x SHARC processors also removed the RSI Master boot mode and added the same security features. However, unlike the ADSP-BF70x Blackfin processors, these processors do feature link ports, so the Link Port Slave boot mode (with the secure boot features) is also supported.

[Table 4](#) provides a summary of the boot modes supported across the processors.

Boot Mode	ADSP-BF60x	ADSP-BF70x	ADSP-SC58x/ADSP-2158x
SPI Master	Yes	Yes†	Yes†
SPI Slave	Yes	Yes†	Yes†
UART Slave	Yes	Yes†	Yes†
Link Port Slave	Yes	No	Yes†
RSI Master	Yes	No	No

† Secure boot mode is also supported for this peripheral

Table 4. Boot Mode Summary

References

- [1] *ADSP-BF60x Blackfin Processor Hardware Reference*. Rev. 0.5, February 2013. Analog Devices, Inc.
- [2] *ADSP-BF606/ADSP-BF607/ADSP-BF608/ADSP-BF609 Blackfin Dual Core Embedded Processor Data Sheet*. Rev. A, February 2014. Analog Devices, Inc.
- [3] *ADSP-BF70x Blackfin Processor Hardware Reference*. Rev. 0.2, May 2014. Analog Devices, Inc.
- [4] *ADSP-BF700/701/702/703/704/705/706/707 Blackfin+ Core Embedded Processor Data Sheet*. Rev. PrD, November 2014. Analog Devices, Inc.
- [5] *ADSP-SC58x Processor Hardware Reference*. Preliminary Revision 0.2, June 2015. Analog Devices, Inc.
- [6] *SHARC+ Core Dual Processor with ARM Cortex-A5 Data Sheet*. Rev PrC, May 2015. Analog Devices, Inc.

Document History

Revision	Description
Rev 1 – June 15 th 2015 by Jeyanthi J and Gurudath V	Initial Revision