



Estimating Power for the ADSP-21362 SHARC® Processors

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Introduction

This EE-Note discusses power consumption of the ADSP-21362, ADSP-21363, ADSP-21364, ADSP-21365, and ADSP-21366 SHARC® processors, hereafter representatively referred to as ADSP-21362 processors.

Power estimates are based on characterization data measured over power supply voltage, core frequency ($CCLK$), and junction temperature (T_J). The intent of this document is to assist board designers in estimating their power budget for power supply design and thermal relief designs using ADSP-21362 processors.

ADSP-21362 processors are members of the SIMD SHARC family of processors, featuring Analog Devices Super Harvard Architecture. Like other SHARC processors, the ADSP-21362 is a 32-bit processor optimized for high-precision signal processing applications.

In the commercial and industrial temperature ranges, the processor operates at core clock frequencies of 100-333 MHz with the core operating at 1.2 V (V_{DDINT}) and the I/O operating at 3.3 V (V_{DDEXT}). In the extended industrial temperature range, the processor operates at core clock frequencies of 100-200 MHz with the core operating at 1.0 V (V_{DDINT}) and the I/O operating at 3.3 V (V_{DDEXT}).

The total power consumption of the ADSP-21362 processor is the sum of the power consumed for each of the power supply domains (V_{DDINT} , V_{DDEXT} , and AV_{DD}). The total power

consumption has two components: one due to internal circuitry (i.e., the core and the PLL), and the other due to the switching of external output drivers (i.e., the I/O). The following sections detail how to derive both of these components for estimating total power consumption based on different dynamic activity levels, I/O activity, power supply settings, core frequencies, and environmental conditions.

Estimating Internal Power Consumption

The total power consumption due to internal circuitry (on the V_{DDINT} supply) is the sum of the static power component and dynamic power component of the processor's core logic. The dynamic portion of the internal power is dependent on the instruction execution sequence, the data operands involved, and the instruction rate. The static portion of the internal power is a function of temperature and voltage; it is not related to processor activity.

Analog Devices provides current consumption figures and scaling factors for discrete dynamic activity levels. System application code can be mapped to these discrete numbers to estimate the dynamic portion of the internal power consumption for an ADSP-21362 processor in a given application.

Internal Power Vector Definitions and Activity Levels

The following power vector definitions define the dynamic activity levels that apply to the internal power vectors shown in [Table 2](#).

- **$I_{DD-IDLE}$** V_{DDINT} supply current for idle activity. Idle activity is the core executing the `IDLE` instruction only, with no core memory accesses, no DMA, and no interrupts.
- **$I_{DD-INLOW}$** V_{DDINT} supply current for low activity. Low activity is the core executing a single-function instruction fetched from internal memory, with no core memory accesses, no DMA, and no Parallel Port (PP) activity.
- **$I_{DD-INMED}$** V_{DDINT} supply current for medium activity. Medium activity is the core executing a multi-function instruction fetched from internal memory and a `NOP`, with 8 core memory accesses per `CLKIN` cycle (DMx64), DMA through three SPORTs running at 3.47 MHz and no Parallel Port (PP) activity. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random.
- **$I_{DD-INHIGH}$** V_{DDINT} supply current for high activity. High activity is the core executing a multi-function instruction fetched from internal memory, with 16 core memory accesses per `CLKIN` cycle (DMx64) and DMA through three SPORTs running at 3.47 MHz, and Parallel Port (PP) running with 5 wait-states. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random.
- **$I_{DD-INPEAK}$** V_{DDINT} supply current for peak activity. Peak activity is the core executing a multi-function instruction fetched from internal memory and/or cache, with 16 core memory accesses per `CLKIN` cycle (DMx64, PMx64), DMA through six SPORTs running

at 41.67 MHz, and Parallel Port (PP) running at 27.75 MHz. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random.



The test code used to measure $I_{DD-INPEAK}$ represents worst-case processor operation. This activity level is not sustainable under normal application conditions.

[Table 1](#) summarizes the low, medium, high, and peak dynamic activity levels corresponding to the internal power vectors listed above and in [Table 2](#).

Operation	Low	Medium	High	Peak
Instruction Type	Single-function	Multi-function	Multi-function	Multi-function
Instruction Fetch	Internal Memory	Internal Memory, NOP	Internal Memory	Internal Memory, Cache
Core Memory Access ¹	None	8 per t _{CK} cycle ²	16 per t _{CK} cycle ³	16 per t _{CK} cycle
DMA Transmit Int to Ext				
SPORTs	N/A	3 @ 1/96*CCK	3 @ 1/96*CCK	6 @ 1/8*CCK
Parallel Port	N/A	N/A	5 ws	0 ws
Data Bit Pattern for Core Memory Access and DMA	N/A	Random	Random	Random

Table 1. Dynamic Activity Level Definitions

¹ t_{CK} = CLKIN; Core clock ratio 16:1

² DMx64 accesses

³ DMx64, PMx64 accesses

Estimating I_{DDINT} Dynamic Current, I_{DD-DYN}

There are two steps involved in estimating the dynamic power consumption due to the internal circuitry (i.e., on the V_{DDINT} supply). The first step is to determine the dynamic baseline current, and the second step is to determine the percentage of activity for each discrete power vector with respect to the entire application.

I_{DD} Baseline Dynamic Current, I_{DD-BASELINE-DYN}

The ADSP-21362 I_{DD-BASELINE-DYN} current graph in Figure 1 (Appendix A contains a larger image of this graph). Note that the I_{DD-BASELINE-DYN} current is derived using the I_{DD-INHIGH} dynamic activity level vs. core frequency. Each curve in the graph represents a baseline I_{DDINT} dynamic current for a specified power supply setting. Using the curve specific to the application, the baseline dynamic current (I_{DD-BASELINE-DYN}) for the V_{DDINT} power supply domain can be estimated at the operating frequency of the processor in the application. For example, with the core operating at 1.2 V (V_{DDINT}) and a frequency of 333 MHz, the corresponding baseline dynamic current (I_{DD-BASELINE-DYN}) for the V_{DDINT} power supply domain would be approximately 0.75 A.

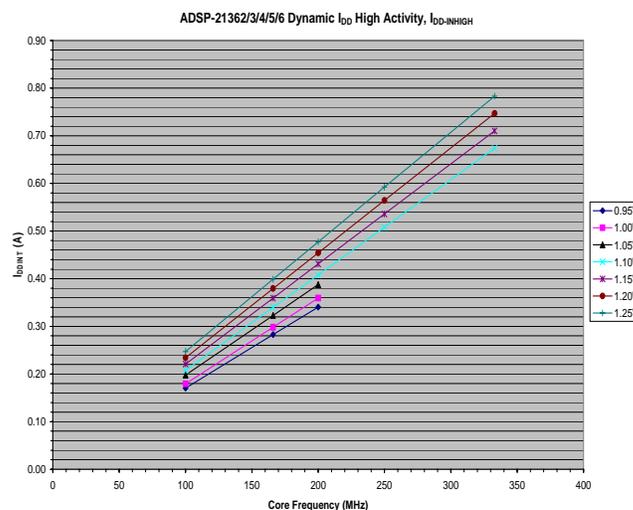


Figure 1. Baseline I_{DDINT} Dynamic Current

I_{DD} Dynamic Current Running Your Application

Table 1 lists the scaling factors for each activity level, which are used to estimate the dynamic current for each specific application. With knowledge of the program flow and an estimate of the percentage of time spent at each activity level, the system developer can use the baseline dynamic current (I_{DD-BASELINE-DYN}) shown in Figure 1 and the corresponding activity scaling factors from Table 2 to determine the dynamic

portion of the internal current (I_{DD-DYN}) for each ADSP-21362 processor in a system.

Power Vector	Activity Scaling Factor (ASF)
$I_{DD-IDLE}$	0.21
$I_{DD-INLOW}$	0.40
$I_{DD-INMED}$	0.85
$I_{DD-INHIGH}$	1.00
$I_{DD-INPEAK}$	1.13

Table 2. Internal Power Vectors and Dynamic Scaling Factors

The dynamic current consumption for an ADSP-21362 in a specific application is calculated according to the following formula, where “%” is the percentage of the overall time that the application spends in that state:

$$\begin{aligned}
 & (\% \text{ Peak activity level } \times I_{DD-INPEAK} \text{ ASF } \times I_{DD-BASELINE_DYN}) \\
 & (\% \text{ High activity level } \times I_{DD-INHIGH} \text{ ASF } \times I_{DD-BASELINE_DYN}) \\
 & (\% \text{ High activity level } \times I_{DD-INMED} \text{ ASF } \times I_{DD-BASELINE_DYN}) \\
 & (\% \text{ Low activity level } \times I_{DD-INLOW} \text{ ASF } \times I_{DD-BASELINE_DYN}) \\
 & + (\% \text{ Idle activity level } \times I_{DD-IDLE} \text{ ASF } \times I_{DD-BASELINE_DYN}) \\
 & = \text{Total Dynamic Current for } V_{DDINT} \text{ (} I_{DD-DYN} \text{)}
 \end{aligned}$$

Equation 1. Internal Dynamic Current (I_{DD-DYN})

For example, after profiling the application code for a particular system, activity is determined to be proportioned as follows.

$$\begin{aligned}
 & (10\% \text{ Peak Activity Level}) \\
 & (30\% \text{ High Activity Level}) \\
 & (50\% \text{ Med. Activity Level}) \\
 & (10\% \text{ Low Activity Level}) \\
 & (0\% \text{ Idle Activity Level})
 \end{aligned}$$

Figure 2. Internal System Activity Levels

Using the activity scaling factors (ASF) provided for each activity level in Table 2 (and with the core operating at 1.2 V (V_{DDINT}) and 333 MHz), a value for the dynamic portion of the internal current consumption of a single processor can be estimated as follows.

$$\begin{aligned}
 & (10\% \times 1.13 \times 0.75) \\
 & (30\% \times 1.00 \times 0.75) \\
 & (50\% \times 0.85 \times 0.75) \\
 & (10\% \times 0.40 \times 0.75) \\
 & + (0\% \times 0.20 \times 0.75) \\
 & \hline
 & I_{DD-DYN} = 0.66A
 \end{aligned}$$

Figure 3. Internal Dynamic Current Estimation

Therefore, the total estimated dynamic current on the V_{DDINT} power supply in this example is 0.66 A.

Estimating I_{DDINT} Static Current, $I_{DD-STATIC}$

The ADSP-21362 $I_{DD-STATIC}$ current graph is shown in Figure 4 (Appendix C contains a larger image of this graph). The static current on the V_{DDINT} power supply domain is function of temperature and voltage but is *not* a function of frequency or activity level. Therefore, unlike the dynamic portion of the internal current, the static current does not need to be calculated for each discrete activity level or power vector. Using the static current curve corresponding to the application (i.e., at the specific V_{DDINT}), the baseline static current ($I_{DD-STATIC}$) can be estimated vs. junction temperature (T_J) of the ADSP-21362 processor.

For example, in an application with the core operating at 1.2 V (V_{DDINT}) and the ADSP-21362 at a junction temperature (T_J) of +100°C (see Appendix A for estimating T_J), the corresponding baseline static current ($I_{DD-STATIC}$) for the V_{DDINT} power supply domain would be approximately 0.55 A.

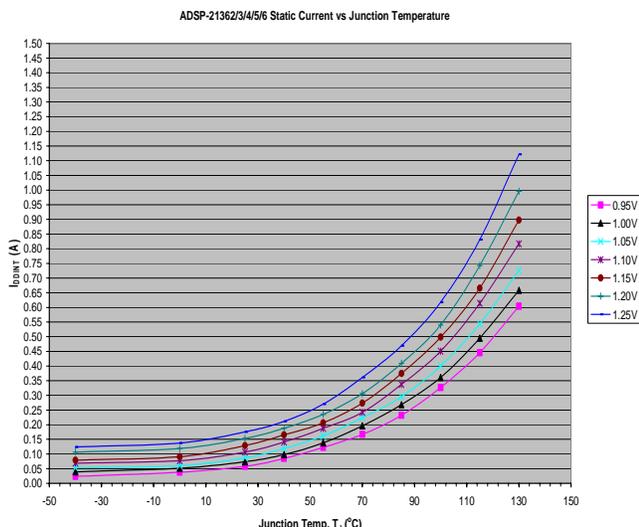


Figure 4. Baseline I_{DDINT} Static Current

The static power of the ADSP-21362 is constant for a given voltage and temperature. Therefore, it is simply added to the total estimated dynamic current when calculating the total power consumption due to the internal circuitry of the ADSP-21362. Note that the $I_{DD-STATIC}$ current shown in Figure 4 represents the worst-case static current as measured across the wafer fabrication process for the ADSP-21362 device.

Estimating Total I_{DDINT} Current

The total current consumption due to the internal core circuitry (I_{DDINT}) is the sum of the dynamic current component and the static current component as shown in Equation 2.

$$I_{DDINT} = I_{DD-DYN} + I_{DD-STATIC}$$

Equation 2. Internal Core Current (I_{DDINT}) Calculation

Continuing with the example (the processor operating at 1.2 V and 333 MHz, and with the code as profiled) assume that the resulting junction temperature (T_J) is estimated to be +100°C. The total internal current consumed by the processor core under these conditions would be:

$$I_{DDINT} = 0.66 + 0.55 = 1.21A$$

Equation 3. Total Internal Core Current Estimation

Each ADSP-21362 processor includes an analog phase-lock loop (PLL) and related internal circuitry to provide clock signals to the core and peripheral logic. This circuitry receives power through the AV_{DD} power supply pin of the processor. Compared to the processor core, this circuitry consumes little power. However, since it is always active, it should be considered when calculating the overall power consumed by the internal circuitry of each ADSP-21362 processor.

The ADSP-21362 data sheet indicates that the maximum expected A_{IDD} per processor is 10 mA; therefore, the total expected internal current consumed by the processor core and the PLL logic under the conditions described in the example would be:

$$I_{DDINT} = 0.66 + 0.55 + 0.01 = 1.22A$$

Equation 4. Total Internal Current Estimation

Total Estimated Internal Power, P_{DDINT}

The resulting internal power consumption (P_{DDINT}) is given by Equation 5.

$$P_{DDINT} = V_{DDINT} \times I_{DDINT}$$

Equation 5. Internal Power (P_{DDINT}) Calculation

Using Equation 5, the total estimated internal power consumed by the processor in the application described in this example would be:

$$P_{DDINT} = 1.20V \times 1.22A = 1.46W$$

Equation 6. Total Internal Power (P_{DDINT}) Estimation

Estimating External Power Consumption

The external power consumption (on the V_{DDEXT} supply) is dependent on the switching of the output pins. The magnitude of the external power depends on:

- The number of output pins that switch during each cycle, O
- The maximum frequency at which the output pins can switch, f
- The voltage swing of the output pins, V_{DDEXT}
- The load capacitance of the output pins, C_L

In addition to the input capacitance of each device connected to an output, the total load capacitance should include the capacitance (C_{OUT}) of the processor pin itself, which is driving the load. The maximum data transfer rate for the parallel port address/data pins (AD15-0) is one-twelfth (1/12) the processor core clock rate. This corresponds to a maximum switching frequency of 27.75 MHz for AD15-0 and a maximum switching frequency of 27.75 MHz for WR at a core clock rate of 333 MHz. In addition, the serial ports can operate up to one-eighth (1/8) the processor core clock rate. This corresponds to a maximum switching frequency of 20.8 MHz for SDATA and a maximum switching frequency of 41.6 MHz for SCLK at a core clock rate of 333 MHz.

Equation 7 shows how to calculate the average external current (I_{DDEXT}) using the above parameters :

$$I_{DDEXT} = O \times f \times V_{DDEXT} \times C_L$$

Equation 7. External Current (I_{DDEXT}) Calculation

The estimated average external power consumption (P_{DDEXT}) can be calculated as follows.

$$P_{DDEXT} = V_{DDEXT} \times I_{DDEXT}$$

Equation 8. External Power (P_{DDEXT}) Calculation

Using the sample configuration (Figure 5), we can estimate the external current and thereby the external power consumption with the following assumptions:

- Processor core running at 333 MHz (CCLK)

- 64K x 16 bit external memory, $C_L = 10\text{pF}$ (trace capacitance ignored)
- 16 bit external latch (used to hold the address when accessing external memory), $C_L = 10\text{pF}$ (trace capacitance ignored)
- During external memory writes, 50% of the AD15-0 pins are switching
- Transfer of data (writes) to external memory takes two cycles (32-bit transfer to 16-bit external memory):
 - 1st cycle is an ALE cycle where the processor drives the external address on the AD15-0 pins
 - 2nd cycle is a WRITE cycle where the processor drives the data to be written on the AD15-0 pins
- DAI configured to transmit and receive 32-bit words at $1/8 * \text{CCLK}$, $C_L = 10 \text{ pF}$ (trace capacitance ignored)
- Output capacitance of processor pin, $C_{OUT} = 4.7 \text{ pF}$

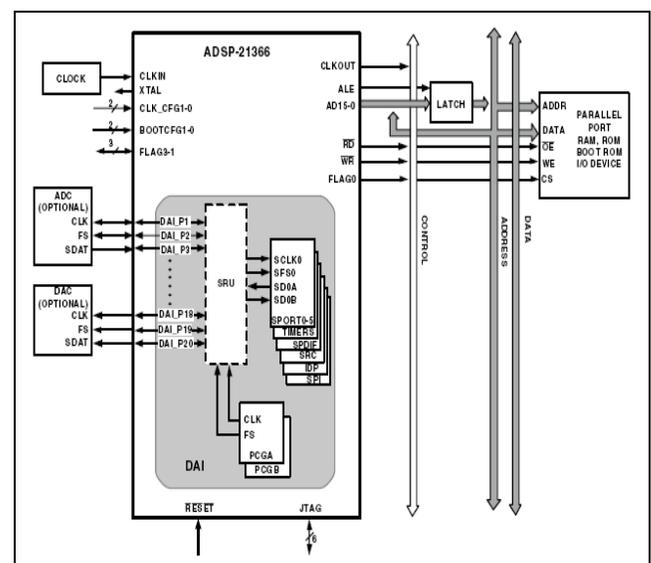


Figure 5. ADSP-21362 System Sample Configuration

The external current (I_{DDEXT}) (Equation 7) can be calculated for each class of pins that can drive as shown in Table 3.

Pin Type	No. of Pins	% Switching	x f	x V _{DDEXT}	x C	I _{DDEXT}
AD15-0	16	50	27.75 MHz	3.3V	4.7pF + (2 x 10pF)	0.01811
$\overline{\text{RD}}$	1	0	n/a	3.3V	4.7pF + (1 x 10pF)	0.00000
$\overline{\text{WR}}$	1	100	27.75 MHz	3.3V	4.7pF + (1 x 10pF)	0.00135
ALE	1	100	27.75 MHz	3.3V	4.7pF + (1 x 10pF)	0.00135
FLAG0	1	0	n/a	3.3V	4.7pF + (1 x 10pF)	0.00000
DAI_P1 (SCLK)	1	100	41.67 MHz	3.3V	4.7pF + (1 x 10pF)	0.00404
DAI_P2 (FS)	1	100	1.3 MHz	3.3V	4.7pF + (1 x 10pF)	0.00013
DAI_P3 (SDATA)	1	0	n/a	3.3V	4.7pF + (1 x 10pF)	0.00000
DAI_P18 (SCLK)	1	100	41.67 MHz	3.3V	4.7pF + (1 x 10pF)	0.00404
DAI_P19 (FS)	1	100	1.3 MHz	3.3V	4.7pF + (1 x 10pF)	0.00013
DAI_P20 (SDATA)	1	100	20.83 MHz	3.3V	4.7pF + (1 x 10pF)	0.00101

Table 3. External Current (I_{DDEXT}) Summary for Figure 3.

Summing the individual currents from above, the total external current (I_{DDEXT}) for the sample configuration shown in Figure 5 would be 0.030 A. Using this current, the estimated average external power is calculated as:

$$P_{DDEXT} = 3.3V \times 0.030A = 0.099W$$

Figure 6. External Power (P_{DDEXT}) Calculation for Sample Configuration Shown in Figure 5

Total Power Consumption

For a particular system, the total power consumption becomes the sum of its individual components, the power consumed by the internal circuitry, and the power consumed due to the switching of the I/O pins, as follows:

$$P_{TOTAL} = P_{DDINT} + P_{DDEXT}$$

Equation 9. Total Power (P_{TOTAL}) Calculation

Where :

P_{DDINT} = Internal power consumption as defined by Equation 5

P_{DDEXT} = External power consumption as defined by Equation 8

For example, if we assume that the processor in Figure 5 is operating under the conditions detailed in the example (the processor operating at 1.2 V, 333 MHz, and code as profiled in Figure 2) and we also assume the resulting junction temperature (T_j) has been estimated to be +100°C (see Appendix A for estimating T_j), the total estimated power consumed would be:

$$P_{TOTAL} = 1.46W + 0.099W = 1.56W$$

Figure 7. Total Power (P_{TOTAL}) Calculation for Sample Configuration Shown in Figure 3 While Running Code Described in Example 1

Appendix A

For the ADSP-21362 the total power budget is limited by the maximum allowed junction temperature (T_J) of the device, +125°C. The ABSOLUTE MAXIMUM RATINGS table in the ADSP-21362 data sheet states that exposure to junction temperatures greater than +125°C for extended periods of time may affect device reliability. Therefore, to avoid causing permanent damage to the device, care should be taken to ensure that T_J does not exceed +125°C.



The ABSOLUTE MAXIMUM RATINGS table in the ADSP-21362 datasheet states that exposure to junction temperatures greater than +125°C for extended periods of time may affect device reliability.

To determine the junction temperature of the device while on the application printed circuit board (PCB), use the following equation:

$$T_J = T_T + (P_{TOTAL} \times \psi_{JT})$$

Equation 10. Junction Temperature (T_J) Calculation

Where:

T_T = Package temperature (°C) measured at the top center of the package

P_{TOTAL} = Total power consumption (W) as defined in [Equation 9](#)

ψ_{JT} = Junction-to-top (of package) characterization parameter (°C /W)

Under natural convection, ψ_{JT} for a thin plastic package is relatively low. This means that under natural convection conditions, the junction temperature (T_J) is typically just a little higher than the temperature at the top-center of the package (T_T). The die is physically separated from the surface of the package by only a thin region of plastic mold compound. Unless the top of the package is forcibly cooled by significant airflow, there will be very little difference between T_T and T_J . However, note that ψ_{JT} is affected by airflow and values for ψ_{JT} under various airflow conditions, and PCB design configurations are listed in the THERMAL CHARACTERISTICS section of ADSP-21362 data sheet for both the 136-ball mini-BGA and the 144-LQFP packages.

The THERMAL CHARACTERISTICS section of the data sheet also provides thermal resistance (θ_{JA}) values for both the 136-ball mini-BGA and the 144-LQFP packages. Data sheet values for θ_{JA} are provided for package comparison and PCB design considerations only and are not recommended for verifying T_J on an actual application PCB.

Industrial applications of the mini-BGA package require thermal vias to an embedded ground plane on the PCB. Refer to JEDEC standard JESD51-9 for printed circuit board thermal ball land and thermal via design information.

Likewise, industrial applications using the LQFP package require thermal trace squares and thermal vias to an embedded ground plane on the PCB. The bottom side thermal slug must be soldered to the thermal trace squares. Refer to JEDEC standard JESD51-5 for more information.

Appendix B

The ADSP-21362 $I_{DD_BASELINE_DYN}$ current graph is shown in Figure 8 (also in Figure 1). The $I_{DD_BASELINE_DYN}$ current is derived using the I_{DD_INHIGH} dynamic activity level vs. core frequency. Each curve in the graph represents a baseline I_{DD_INT} dynamic current for a specified power supply setting.

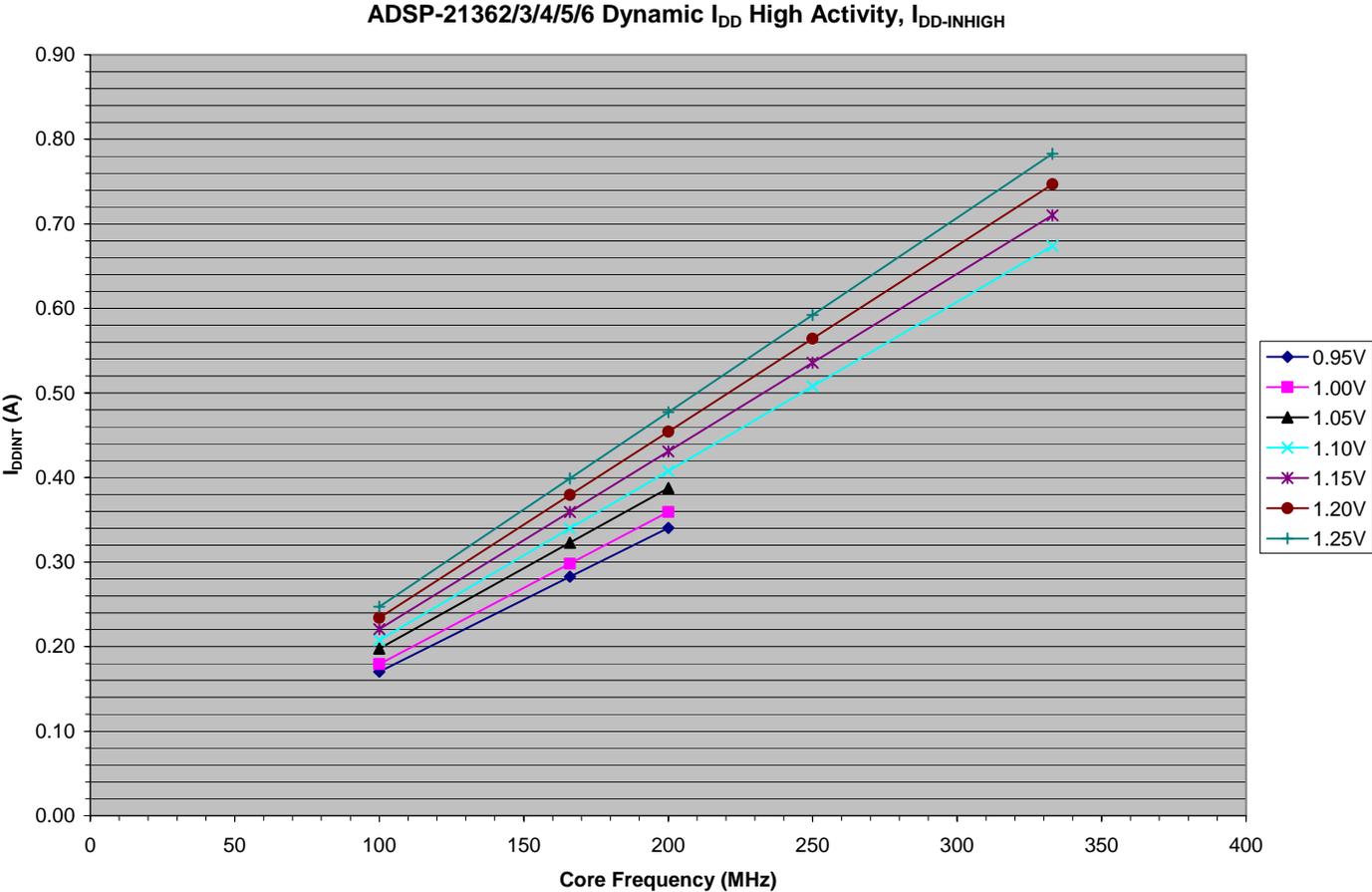


Figure 8. $I_{DD_BASELINE_DYN}$ Graph

Appendix C

The ADSP-21362 $I_{DD-STATIC}$ current graph is shown in Figure 9 (also in Figure 2). The static current on the V_{DDINT} power supply domain is a function of temperature and voltage and is *not* a function of frequency or activity level. Each curve in the graph represents a baseline I_{DDINT} static current for a specified power supply measured at various junction temperatures (T_J). The $I_{DD-STATIC}$ current graph (Figure 9) represents the worse-case static currents as measured across the wafer fabrication process for the ADSP-21362 processor.

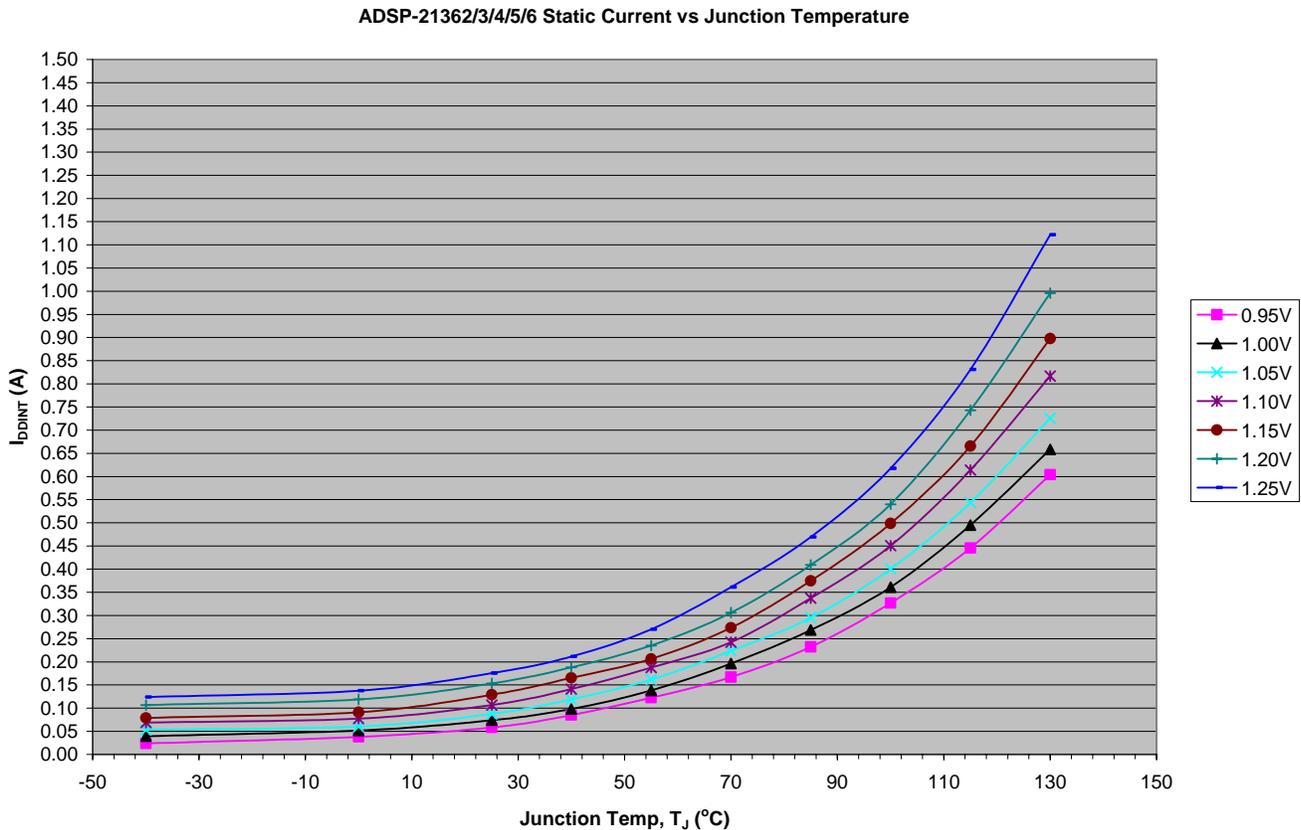


Figure 9. $I_{DD-STATIC}$ Graph

References

- [1] *ADSP-21362 SHARC Processor Data Sheet*. Rev 0, October 2005. Analog Devices, Inc.
- [2] *ADSP-21363 SHARC Processor Data Sheet*. Rev 0, October 2005. Analog Devices, Inc.
- [3] *ADSP-21364 SHARC Processor Data Sheet*. Rev 0, October 2005. Analog Devices, Inc.
- [4] *ADSP-21365 SHARC Processor Data Sheet*. Rev 0, October 2005. Analog Devices, Inc.
- [5] *ADSP-21366 SHARC Processor Data Sheet*. Rev 0, October 2005. Analog Devices, Inc.

Document History

Revision	Description
<i>Rev 1 – January 31, 2006 by Chris Coughlin</i>	Initial Release.