Estimating Power Dissipation for ADSP-21262S SHARC® DSPs

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Introduction

This EE-Note discusses power consumption of the ADSP-21262S SHARC® DSPs based on characterization data measured over power supply voltage, core frequency (CCLK) and ambient operating temperature (T_A). The intent of this document is to assist board designers in estimating their power budget for power supply design and thermal relief designs using the ADSP-21262S DSP.

The ADSP-21262S DSP is a member of the SIMD SHARC family of DSPs featuring Analog Devices’ Super Harvard Architecture. Like other SHARC DSPs, the ADSP-21262S is a 32-bit processor optimized for high-precision signal processing applications. The DSP operates at core clock frequencies up to 200MHz with the core operating at 1.2V (V_DDINT) and the I/O operating at 3.3V (V_DDEXT).

Total power consumption has two components: internal circuitry (i.e. the core and PLL) and switching of external output drivers (i.e. the I/O). The following sections detail how to derive both of these components for estimating total power consumption.

Estimating Internal Power Consumption

The internal power consumption (on the V_DDINT supply) is dependent on the instruction execution sequence and the data operands involved. The data sheet[2] provides current consumption figures for discrete activity levels. Mapping system application code to specified values provides a means of estimating internal power consumption for an ADSP-21262S DSP in a given application.

Internal Power Vector Definitions and Activity Levels

The following power vector definitions define the levels of activity that apply to the internal power vectors shown in Table 1:

- **IDD-IDLE** V_DDINT supply current for Idle activity. Idle activity is the core executing the IDLE instruction only, without core memory accesses, DMA, or interrupts.
- **IDD-INLOW** V_DDINT supply current for Low activity. Low activity is the core executing a single-function instruction fetched from internal memory with no core memory accesses and no DMA.
- **IDD-INHIGH** V_DDINT supply current for High activity. High activity is the core executing a multifunction instruction fetched from internal memory, with 4 core memory accesses per CLKIN cycle (DMx64) and DMA through 3 SPORTs running @ 50MHz. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access and DMA is random.
- **IDD-INTP** Same code as High activity, however, operating under nominal power...
Table 1 lists the maximum internal current consumption for the DSP at different levels of activity. These figures represent the worst case $I_{DD\text{INT}}$ as measured across process, voltage, temperature, and frequency (PVTF). From these internal activity levels (and from an understanding of the program flow using profiling or some other method), you can calculate a worst-case weighted-average of power consumption for each ADSP-21262S DSP in a system.

- **$I_{DD\text{-INPEAK}}$**: $V_{DD\text{INT}}$ supply current for Peak activity. Peak activity is the core executing a multifunction instruction fetched from internal memory and/or cache, with 8 core memory accesses per CLKin cycle (DMx64, PMx64) and DMA through 6 SPORTs running @ 50MHz. The DMA is chained to itself (running continuously) and does not use interrupts. The bit pattern for each core memory access is random, and the DMA bit pattern is worst case.

<table>
<thead>
<tr>
<th>Vector</th>
<th>Test Conditions (worst case except where noted)</th>
<th>$I_{DD\text{INT}}$ (A)</th>
<th>$I_{DD\text{INT}}$ (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{DD\text{-IDLE}}$</td>
<td>$T_A = +70, ^\circ\text{C}, V_{DD\text{INT}} = \text{Max}, \text{CCLK} = \text{Max}$</td>
<td>0.70</td>
<td>0.70</td>
</tr>
<tr>
<td>$I_{DD\text{-INLOW}}$</td>
<td>$T_A = +70, ^\circ\text{C}, V_{DD\text{INT}} = \text{Max}, \text{CCLK} = \text{Max}$</td>
<td>0.85</td>
<td>0.85</td>
</tr>
<tr>
<td>$I_{DD\text{-INHIGH}}$</td>
<td>$T_A = +70, ^\circ\text{C}, V_{DD\text{INT}} = \text{Max}, \text{CCLK} = \text{Max}$</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>$I_{DD\text{-INTYP}}$</td>
<td>$T_A = +25, ^\circ\text{C}, V_{DD\text{INT}} = 1.2, \text{V}, \text{CCLK} = 200, \text{MHz}$</td>
<td>0.50</td>
<td>0.50</td>
</tr>
<tr>
<td>$I_{DD\text{-INPEAK}}$</td>
<td>$T_A = +70, ^\circ\text{C}, V_{DD\text{INT}} = \text{Max}, \text{CCLK} = \text{Max}$</td>
<td>1.26</td>
<td>1.06</td>
</tr>
</tbody>
</table>

**Table 1: Maximum Internal Current Consumption per Vector Type**

1. Worst-case conditions: $T_J < +125\, ^\circ\text{C}, V_{DD\text{EXT}} = 3.47\, \text{V}, V_{DD\text{INT}} = 1.26\, \text{V}, \text{CCLK} = 200\, \text{MHz}$; does not apply to $I_{DD\text{-INTYP}}$

2. Worst case across process, voltage, temperature and frequency (PVTF) for 136-ball mBGA package option. See “Estimating Total Power Consumption and Power Budget” for more information pertaining to the power budget and the mBGA package option.

3. Worst case across process, voltage, temperature and frequency (PVTF) for 144-lead LQFP package option. See “Estimating Total Power Consumption and Power Budget” for more information pertaining to the power budget and the LQFP package option.

<table>
<thead>
<tr>
<th>Operation</th>
<th>Low Activity</th>
<th>High Activity</th>
<th>Peak Activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction Type</td>
<td>Single Function</td>
<td>Multifunction</td>
<td>Multifunction</td>
</tr>
<tr>
<td>Instruction Fetch</td>
<td>Internal Memory</td>
<td>Internal Memory</td>
<td>Internal Memory, Cache</td>
</tr>
<tr>
<td>Core Memory Access &lt;sup&gt;4&lt;/sup&gt;</td>
<td>None</td>
<td>4 per $t_{CK}$ cycle (DMx64)</td>
<td>8 per $t_{CK}$ cycle (DMx64, PMx64)</td>
</tr>
<tr>
<td>DMA Transmit Int to Ext</td>
<td>N/A</td>
<td>3 SPORTs running @ 50 MHz</td>
<td>6 SPORTs running @ 50MHz</td>
</tr>
<tr>
<td>Data Bit Pattern for core Memory Access and DMA</td>
<td>N/A</td>
<td>Random</td>
<td>Worst case</td>
</tr>
</tbody>
</table>

**Table 2: Activity Level Definitions**

<sup>4</sup> $t_{CK} = \text{CLKIN}$; Core clock ratio 8:1
Table 2 summarizes low, high and peak activity levels corresponding to the vectors listed in Table 1.

The average current consumption for an ADSP-21262S device in a specific application is calculated according to the following formula, where “%” is the percentage of the time that the application spends in that state.

\[
\text{Total Current for } V_{DDINT} (I_{DDINT}) = \% \text{ Peak Activity Level} \times I_{DD-INPEAK} + \% \text{ High Activity Level} \times I_{DD-INHIGH} + \% \text{ Low Activity Level} \times I_{DD-INLOW} + \% \text{ Idle Activity Level} \times I_{DD-IDLE}
\]

\[
\begin{align*}
30\% & \times 1.26 \\
30\% & \times 1.00 \\
20\% & \times 0.85 \\
20\% & \times 0.70 \\
\hline
I_{DDINT} & = 0.988 \text{ A}
\end{align*}
\]

**Example 2: Internal Current Estimation Example**

Therefore, an estimate of the average internal power for the processor can be calculated from Example 2 as follows:

\[
P_{DDINT} = V_{DDINT} \times I_{DDINT} = 1.20 \text{ V} \times 0.988 \text{ A} = 1.1856 \text{ W}
\]

**Example 3: Internal Power Estimation**

**Estimating External Power Consumption**

The external power consumption (on the \(V_{DDEXT}\) supply) is dependent on the switching of the output pins. The magnitude of the external power depends on:

- The number of output pins \((O)\) that switch during each cycle
- The maximum frequency \((f)\) at which the output pins can switch
- The voltage swing of the output pins \((V_{DDEXT})\)
- The load capacitance of the output pins \((C_L)\)

In addition to the input capacitance of each device connected to an output, the total load capacitance includes the capacitance \((C_{OUT})\) of the DSP pin itself which is driving the load. The parallel port address/data pins (AD15-0) can transfer data at 1/3 the DSP core clock rate. This corresponds to a maximum switching frequency of 33MHz for AD15-0 and 66MHz for /WR at a core clock rate of 200MHz. In addition, the serial ports can operate up to 1/8 the DSP core clock rate. This corresponds to a maximum switching frequency of 12.5MHz for SDATA and a
maximum switching frequency of 25MHz for SCLK at a core clock rate of 200MHz.

Equation 3 shows how to calculate the average external current (I_{DDEXT}) using the above parameters:

\[ I_{DDEXT} = O \times f \times V_{DDEXT} \times C_L \]

*Equation 3: External Current (I_{DDEXT}) Calculation*

Estimated average external power consumption (P_{DDEXT}) can then be calculated as:

\[ P_{DDEXT} = V_{DDEXT} \times I_{DDEXT} \]

*Equation 4: External Power (P_{DDEXT}) Calculation*

Using the sample configuration shown in Figure 1, we can estimate the external current and thereby the external power consumption with the following assumptions:

- DSP core running at 200MHz (CCLK)
- 64K x 16-bit external memory, C_L = 10pF
- 16-bit external latch (used to hold the address when accessing external memory), C_L = 10pF
- AD15-0 can transfer data at a rate of 1/3 * CCLK, with 50% of the pins switching
- External memory write cycles can occur at a rate of 1/6 * CCLK (32-bit transfer to 16-bit external memory)
- DAI configured to transmit and receive 32-bit words at 1/8 * CCLK, C_L = 10pF
- Output capacitance of DSP pin, C_{OUT} = 4.7pF

Using Equation 3, I_{DDEXT} can then be calculated for each class of pins that can drive as shown in Table 3.

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9 Trace capacitance is ignored

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*Figure 1: ADSP-2126x System Sample Configuration*
Table 3: External Current (I_{DEXT}) Summary for Figure 1.

Summing the individual currents from Table 3, the total external current (I_{DEXT}) for the example configuration shown in Figure 1 is 0.0527 A. Using this current, the estimated average external power can then be calculated as:

\[
P_{DDEXT} = 3.3 \, V \times 0.0527 \, A = 0.1739 \, W
\]

Example 4: External Power (P_{DEXT}) Calculation

At T_A = +70°C, the P_TOTAl for any ADSP-2126x should not exceed 1.95W in the mBGA or 1.69W in the LQFP package for proper DSP operation. Power consumption greater than these limits (1.95W or 1.69W) could result in permanent damage to the DSP.

\[
T_J = P_{TOTAL} \times \theta_{JA} + T_A
\]

Equation 5: Junction Temperature (T_J) Calculation

Table 4 contains examples of power supply currents that satisfy the total power budget for an ADSP-2126x DSP in an mBGA package operating at T_A = +70°C. Power is calculated using V_{DDMAX} for each power supply:

<table>
<thead>
<tr>
<th>I_{DDINT} (A)</th>
<th>I_{DEXT} (A)</th>
<th>A_{DD} (A)</th>
<th>P_{DDINT} (W)</th>
<th>P_{DEXT} (W)</th>
<th>P_{PLL} (W)</th>
<th>P_{TOTAL} (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.9</td>
<td>0.231</td>
<td>0.01</td>
<td>1.134</td>
<td>0.8016</td>
<td>0.0126</td>
<td>1.95</td>
</tr>
<tr>
<td>1.0</td>
<td>0.195</td>
<td>0.01</td>
<td>1.260</td>
<td>0.6774</td>
<td>0.0126</td>
<td>1.95</td>
</tr>
<tr>
<td>1.1</td>
<td>0.159</td>
<td>0.01</td>
<td>1.386</td>
<td>0.5514</td>
<td>0.0126</td>
<td>1.95</td>
</tr>
<tr>
<td>1.2</td>
<td>0.123</td>
<td>0.01</td>
<td>1.512</td>
<td>0.4254</td>
<td>0.0126</td>
<td>1.95</td>
</tr>
</tbody>
</table>

Table 4: Power Supply Currents and Total Power Budget

** Note: the total power budget (P_{TOTAL}) can be increased by reducing the ambient operating temperature (T_A). However, the user must insure that the maximum junction temperature (T_J), as defined by Equation 6, does not exceed +125°C.

For additional information regarding the power budget and its relationship to the thermal characteristics of the ADSP-2126x DSP, see the Thermal Characteristics section of ADSP-2126x data sheet.
## Estimating Total Power Consumption and Power Budget

For a particular system, the total power budget is equal to the sum of the individual components:

\[
PTOTAL = P_{DDINT} + P_{DDEXT} + P_{PLL}
\]

*Equation 6: Total Power (PTOTAL) Calculation*

where:

- \(P_{DDINT}\): Average internal power consumption as defined by Equation 2
- \(P_{DDEXT}\): Average external power consumption as defined by Equation 4
- \(P_{PLL}\): Power consumption due to the PLL as defined by \((A_{DD} \times AV_{DD})\) where the max value for \(A_{DD}\) and \(AV_{DD}\) is listed in the data sheet

For ADSP-2126x DSPs, the total power budget is limited to 1.95W (mBGA package) and 1.69W (LQFP package). The power budget is determined by the package thermal resistance \((\theta_{JA})\), 28.2°C/W for the mBGA and 32.5°C/W for the LQFP, a maximum operating temperature \((T_A)\) of +70°C and a maximum junction temperature \((T_J)\) of +125°C. Equation 5 shows the relationship between these three parameters and power:

\[
IDDINT \text{ versus Voltage, Frequency and Operating Temperature}
\]

The following section contains graphs of \(IDDINT\) for various activity levels versus the specified ranges of processor core voltage \((V_{DDINT})\), operating frequency \((CCLK)\) and ambient operating temperature \((T_A)\). Each of these curves represent the mean value for \(IDDINT\) across process, voltage, temperature and frequency \((PVTF)\). These graphs provide the system designer with data showing the effect of core voltage, processor operating frequency and ambient operating temperature on internal power consumption \((P_{DDINT})\). With this information, a system can be designed to meet the power budget requirements of an ADSP-2126x DSP as discussed in the previous section of this EE-Note.
$I_{D\text{D-INLOW}}$ versus Voltage, Frequency and Operating Temperature

$I_{D\text{D-INLOW}}$ vs $V_{\text{DDINT}}$

$V_{\text{DDINT}} (V)$

$TA = 0^\circ C$

$TA = 25^\circ C$

$TA = 70^\circ C$

$I_{D\text{D-INLOW}}$ vs Clock Frequency

$CCLK (MHz)$

$I_{D\text{D-INLOW}}$ vs Ambiant Operating Temp ($TA$)

$TA (^\circ C)$
**IDD-INHIGH versus Voltage, Frequency and Operating Temperature**

*IDD-INHIGH vs VDDINT*

(CCLK = 200MHz, VDDEXT = 3.3V)

*IDD-INPEAK vs VDDINT*

(CCLK = 200MHz, VDDEXT = 3.3V)

**IDD-INHIGH vs CCLK FREQ**

(TA = +70°C and VDDEXT = 3.3V)

**IDD-INPEAK vs CCLK FREQ**

(TA = +70°C and VDDEXT = 3.3V)
References


Document History

<table>
<thead>
<tr>
<th>Version</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>December 02, 2003 by R. Murphy</td>
<td>Initial Release</td>
</tr>
</tbody>
</table>