



## Considering the ADSP-21262 SHARC® DSP

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### Introduction

The ADSP-21262 DSP is the latest member of the SHARC® family delivering new levels of speed, power performance and peripheral integration while maintaining code compatibility with the existing SHARC portfolio of products. This document is focused on helping existing SHARC designers who need information on evaluating whether upgrading systems to the new ADSP-21262 is right for them. This note will highlight the new features that the ADSP-21262 has to offer and detail the list of traditional SHARC peripherals that do not exist in this product. The ADSP-21161 will be used as the example for the traditional SHARC processor. For a more in depth analysis of each of the peripherals available on the ADSP-21262 the ADSP-2126x SHARC Hardware Reference Manual is an excellent resource.

### Commonalities

The ADSP-21262 has a lot in common with the previous members of the SHARC family in terms of memory and core functionality. The serial interfaces and JTAG port are also largely the same as in the ADSP-21161 and other SHARC products.

The ADSP-21262 uses the SHARC SIMD core and runs at 200MHz, twice the speed of the ADSP-21161. Because the ADSP-21262 uses the traditional 2<sup>nd</sup> generation SIMD SHARC core, existing code written for the core is 100% compatible to the ADSP-21262. The ADSP-

21262 also provides 2Mbits of on chip dual ported SRAM, twice what is available on the ADSP-21161. The efficient model for accessing data from memory using the core or IO processor also remains the same between both parts. In addition there is a 4Mbit secure ROM that can be programmed with your personal code at an additional fee.

While you will find that some of the peripheral options have been significantly changed, the serial interface protocols are similar to those that exist in the ADSP-21161. There are 6 serial ports available on the ADSP-21262 and they support normal mode, I2S and TDM as well as a left justified sample pair mode that is common to some older CODEC components. The SPORTs are connected to the pins on the DSP through a signal routing unit (SRU) which is part of the Digital Applications Interface (DAI) that will be discussed in more detail later in this document. The SPORTs will continue to run at half the core processor speed translating to 100Mbits/s on the ADSP-21262. Additionally, precision clock generators (PCG) now enable the DSP to generate a low jitter clock for use by external devices as well as the DSPs own serial ports.

In addition to serial ports, the ADSP-21262 supports the SPI protocol in a separate port. While the internal design of the SPI port is not identical to the ADSP-21161, the functionality is mainly the same. The major difference between the 2 ports is that ADSP-21262 now supports DMA chaining on the SPI DMA channel. The

transmit and receive DMA channels are shared on this part so DMA transfers are not full duplex, although they can be if the core is used or is used in conjunction with DMA. A hardware option for SPI master booting allows the DSP to boot from serial EPROM and FLASH in addition to the traditional SPI slave boot mode that allows an SPI host to control the booting process on the DSP.

The boundary scan and ICE/debug functionality provided is the same as in the previous SHARC family processor, save two functionality improvements: user defined hardware breakpoints and background telemetry channels (BTC). The user defined hardware breakpoints allow users to program hardware breakpoints from within their application code instead of manually through the emulator software. The BTC is an enhanced trace capability that allows the emulator to modify some buffers through JTAG without interrupting the core.

## Important Differences

One of the goals for the ADSP-21262 is to provide a flexible and powerful SHARC in a smaller package that uses less power and real estate for a more attractive price. A number of major changes have been made to facilitate this philosophy.

One of the ways to meet this goal was to introduce a new way to effectively access a number of the peripherals through what we've termed a Digital Applications Interface (DAI). The DAI contains a signal routing unit (SRU) that allows 20 I/O pins to be configured for use by any of the peripherals in the DAI as well as used as general purpose I/O. The SRU also allows peripherals to be connected to each other internally without having to drive the signal out onto the pads of the DSP. A macro is provided that makes it quite simple to connect signals through the SRU, simplifying the underlying hardware. In addition to the serial ports and the PCG which are mentioned earlier in this

document, there is also an Input Data Port that can capture data from 8 serial channels and bring it into the internal memory via DMA. 3 I/O interval timers can be routed through the SRU as well. These timers are in addition to the programmable timer provided in the core. They support PWM, even capture and can handle watchdog timing. Each pin also has a status bit associated with it so all the pins can be polled. Inputs on these signals can also generate interrupts on the DAI port itself through a dedicated DAI interrupt controller that maps DAI interrupts to the core interrupt handler. The DAI also contains the Parallel Data Acquisition Port (PDAP) for bringing in synchronous parallel data. This configurable 20 pin synchronous port is only capable of data acquisition and cannot write data out of the DAI pins.

Another way to bring the pin count down is to reduce the external port width. Instead of a traditional external/host port, the ADSP-21262 employs a Parallel Port (PP). The PP is a configurable 8 or 16 bit wide port that makes use of a total of 19 pins for data and addressing. The port allows you to access external SRAM via DMA and also allows for booting from an EPROM or FLASH. Because of the limited size of the external port and the associated time constraints that go with accessing packed instructions or data there is no support for external execution. The expanded internal memory space, possibility of using ROM code and the use of overlays from external memory will provide all of the memory requirements for instructions and data. There is also no support for multiprocessing as there was in previous SHARC families as this requires extensive use of a large external bus. The PP and the PDAP are the only ways for the DSP to acquire parallel data. The ADSP-21262 does not support the link port protocol that is supported in a number of previous SHARCs.

## Additional Improvements and Changes

The ADSP-21262 is designed with a new stable PLL. In addition to supporting CLKIN to CORE rates of 3:1, 8:1 and 16:1 on powerup the PLL can be configured dynamically to achieve greater power savings by slowing down the core clock or disengaging the clock from unused peripherals. Multipliers of 1-32 and divisors of 2,4,8 and 16 are supported.

The ADSP-21262 is not a pin compatible option for upgrading from any of the previous SHARC products. The core voltage has also changed to 1.2V due to changes in the process and a push for lower power consumption. There are also some new system design considerations. For customers using the ADSP-2126x with a crystal on the CLKIN pins, in a departure from the 06x & 16x, there is no internal shunt resistor, so the designer would need to add one (we spec 1M-ohm in the datasheet.) Also, the requirement for properly terminating the JTAG signals when the emulator is not in use has become more important in this product. When designing with this part, please consult the updated System

Design Chapter in the Hardware Reference to better understand constraints for designing with this product.

## Conclusion

With twice the speed, more memory, lower power and expanded serial interface options upgrading to the ADSP-21262 can be a wise choice for certain ADSP-21161 designs. This document is intended to provide a general overview of what is new and what is not in the ADSP-21262 and the ADSP-21161. More in-depth analysis of the ADSP-21262 is available in the ADSP-21262 Datasheet and the ADSP-2126x Hardware Reference Manual. Another important reference is the section entitled “Differences from Previous SHARC DSPs” in chapter 1 of the Hardware Reference Manual.

The chart in the appendix summarizes the major differences of the ADSP-21262 and the ADSP-21161 SHARC DSPs.

## Appendix

Features	ADSP-21161	ADSP-21262
<b>Core</b>		
max instruction rate	100MHz	200MHz
Core to CLKIN PLL ratios	2::1, 3::1, 4::1 /CLKDBL will double ratios to 4::1, 6::1 and 8::1	SW Programmable (M/N); 3 ratios pin-selectable: 3::1, 8::1, 16::1; Divisors of 2,4,8 or 16; Multipliers of 1-32
<b>Memory</b>		
On Chip, Dual Port SRAM	1Mbits	2Mbits
On Chip, Custom bootable ROM with security features	N/A	4Mbits
<b>Peripherals</b>		
<b>DMA controller</b>	14 DMA channels	22 DMA channels
<b>SPI</b>	1 port accessible through DMA and core; full duplex with dedicated TX and RX DMA channels	1 port accessible through DMA and core including chaining support; full duplex through the core and half duplex with a shared DMA channel for TX and RX
<b>Digital Applications Interface (DAI)</b>	N/A	Consists of a Signal Routing Unit (SRU), Precision Clock Generator (PCG), Input Data Port (IDP), Parallel Data Acquisition Port (PDAP) and Serial Ports
<b>Serial Port (SPORT)</b>	4 @ max 1/2 core speed (normal mode, I2S, TDM)	6 @ max 1/2 core speed; routed through the SRU, (normal mode, I2S, Left Justified Sample Pair, TDM)
<b>Input Data Port (IDP)</b>	N/A	Captures receive sport data through 8 DMA channels
<b>Precision Clock Generator (PCG)</b>	N/A	Generates up to 4 low jitter clock or frame sync signals
<b>Parallel Data Acquisition Port (PDAP)</b>	N/A	Captures up to 20 bits of parallel synchronous data
<b>General Purpose I/O flags</b>	4 core flags; 8 IOP flags	Multiplexed with other pins; 20 possible routed through the SRU/4 dedicated flags through the PP
<b>Parallel Port (PP)</b>	N/A (see External Port)	
Speed	N/A	66MB/sec typical ; 132MB/sec max
Width	N/A	8 bit data mode (24 bit address space); 16 bit data mode (16 bit address space)
Features	N/A	supports overlays
<b>External Port</b>		see (Parallel Port)

Speed	CLKIN or 2xCLKIN	N/A
Width	24 bit address bus (32 bit data bus expandable to 48 bits)	N/A
Features	Multiprocessor Support, External Execution, Overlays	N/A
<b>Link Ports</b>	2 (nibble or byte wide)	N/A (see PDAP or PP for parallel data acquisition)
<b>JTAG Support</b>	Boundary Scan and basic emulation support	Boundary Scan and Enhanced emulation support including Background Telemetry and Software defined breakpoints
<b>Temperature Grades</b>	K (0 to 85 C) : C (-40 to 105 C)	K (0 to 85 C) : C (-40 to 105 C)
<b>Voltage Requirement</b>	1.8V core/ 3.3V IO	1.2V core/ 3.3V IO
<b>Package</b>	225 BGA	135 ball BGA; 144 pin LQFP
<b>Approximate Pricing in 10K volume</b>	\$21.67	\$14.95 for BGA; \$16.45 for LQFP

Appendix 1. Comparison of the ADSP-21161 and the ADSP-21262

## References

- [1] ADSP-21161 SHARC® DSP Microcomputer Data Sheet. First Rev A, Analog Devices, Inc.
- [2] ADSP-21262 SHARC® High Performance Floating-Point Processor Preliminary Data Sheet. Rev. PrB, Analog Devices, Inc.

## Document History

Version	Description
September 25, 2003	Title change
September 3, 2003 by G. Linden	Initial Release