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Power Supply Sequencing
by Martin Murnane and Chris Augusta

POWER-UP CONSIDERATIONS

Powering up a circuit on a printed circuit board is too often taken for granted and can cause damage and both destructive and nondestructive latch-up conditions. These problems may not be prominent until volume production begins when the tolerances of devices and designs are put to the test. This is dangerously late in the process and extremely expensive, with respect to time and the delivery of projects and products. Errors found at this stage result in numerous modifications, including PCB layout changes, design alterations, and extra anomalies.

With the advent of incorporating many functional blocks into one integrated circuit (IC), this has resulted in supplying these blocks with multiple, sometimes equal, or in many instances, differing voltage supplies. As more and more of these system-on-a-chip (SoC) ICs proliferate the marketplace, the need for particular power supply sequencing and power management issues arises.

There is usually enough information in data sheets from Analog Devices, Inc., to guide a designer to a correct power-up sequence for an individual IC. However, some ICs specifically require a well-defined power-up sequence. This is true in the case of many of ICs from Analog Devices and is quite common in ones using multiple supplies such as converters (consisting of both analog-to-digital converters (ADCs) and digital-to-analog converters (DACs)), digital signal processors (DSPs), audio/video, radio frequency, and many other mixed signal ICs. Essentially, any IC containing some analog input/output with a digital engine falls into this category, where particular power sequencing may be required. On these ICs, there could be separate analog and digital supplies and some may even have a digital input/output supply, as detailed in specific examples discussed in the following sections.

This application note looks at some of the more subtle power supply issues that a designer must consider in new designs, especially when there are several different power supplies required for an IC. Some of the more common supplies presently are: +1.8 V, +2.0 V, +2.5 V, +3.3 V, +5 V, −5 V, +12 V, and −12 V.

With over 10,000 different products worldwide from Analog Devices, the scope of this application note looks only at a few ADCs. However, these supply sequencing considerations can be applied to practically any mixed signal IC from Analog Devices.

PULSAR ADC EXAMPLES—ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings (AMR) section is available in all Analog Devices data sheets. It states what maximum voltages, currents, or temperatures can be applied to the pins or case of a device to avoid causing damage.

The AD7654 PulSAR 16-bit ADCs are quite good examples of mixed signal ADCs with three (or more) separate supplies. These ADCs require a digital supply (DVDD), an analog supply (AVDD), and a digital input/output supply (OVDD). Because these are ADCs, they convert analog signals to digital codes and therefore require an analog core to handle the incoming analog input. The digital core powers the bit-decision process and the control logic. The I/O core is used to set the level of the digital outputs to interface with the host logic (level shift). Specifications for the ADC's supplies are found in the Absolute Maximum Ratings section for each respective data sheet. Table 1 shows an excerpt from the Absolute Maximum Ratings section of the AD7654 (Rev. B) data sheet.

Table 1. Absolute Maximum Ratings for the AD7654 (Rev. B)

Parameter	Values
Analog Inputs	
INAx, INBx, REFx, INxN, REFGND	AVDD + 0.3 V to AGND − 0.3 V
Ground Voltage Differences	
AGND, DGND, OGND	±0.3 V
Supply Voltages	
AVDD, DVDD, OVDD	−0.3 V to +7 V
AVDD to DVDD, AVDD to OVDD	±7 V
DVDD to OVDD	−0.3 V to +7 V
Digital Inputs	−0.3 V to DVDD + 0.3 V

Note that all three supplies in Table 1 can range between −0.3 V and +7 V. AVDD can vary between +7 V and −7 V with respect to DVDD and OVDD. This confirms there is no restriction whether AVDD is powered up first or DVDD. There is also no restriction on whether AVDD is powered up first or OVDD. However, a restriction arises between DVDD and OVDD. Because the specification states that OVDD can be only a maximum of 0.3 V greater then DVDD, DVDD must be powered up before or at the same time as OVDD. If OVDD was powered up first (say to 5 V), DVDD would be less than OVDD by 5 V at power-up and would therefore not comply with the Absolute Maximum Ratings and possibly damage the device.

The analog inputs, INAx, INBx, REFx, INxN, REFGND, have a restriction in that these inputs cannot exceed AVDD + 0.3 V or AGND − 0.3 V. This states that if an analog signal or reference source is present before AVDD, the analog core powers up in a highly probable latched-up state. This is typically a nondestructive condition, but the current through AVDD can easily escalate to 10× the normal current and cause the ADC to become quite hot. In this condition, internal electrostatic discharge (ESD) diodes become forward biased and in turn power up the analog supply. To correct this, power sequence the ADC with the inputs and/or reference source in an unpowered or disconnected state.

In a similar fashion, the digital inputs can be −0.3 V to DVDD + 0.3 V. This states they must be less than DVDD + 0.3 V. This indicates that at power−up, DVDD must be powered up before or at the same time as the microprocessor/logic interface circuitry. Similar to the analog core scenario previously detailed, ESD diodes on these pins can also become forward-biased and power up the digital core in an unknown state.

The faster PulSAR ADCs such as the AD7621, AD7622, AD7623, AD7641, and AD7643 are newer devices in the family using lower voltage supplies of 2.5 V (as opposed to 5 V for the AD7654). For the AD7621 and AD7623, these devices have a clearly specified power-up sequence. Table 2 shows an excerpt from the Absolute Maximum Ratings section of the AD7621 (Rev. 0) data sheet.

Table 2. Absolute Maximum Ratings for the AD7621 (Rev. 0)

Parameter	Rating
Analog Inputs/Outputs	
IN+, IN−, REF, REFBUFIN, TEMP, INGND, REFGND to AGND	AVDD + 0.3 V to AGND − 0.3 V
Ground Voltage Differences	
AGND, DGND, OGND	±0.3 V
Supply Voltages	
AVDD, DVDD	−0.3 V to +2.7 V
OVDD	−0.3 V to +3.8 V
AVDD to DVDD	±2.8 V
AVDD to OVDD	+2.8 V to −3.8 V
OVDD to DVDD	≤ +0.3 V if DVDD < 2.3 V
Digital Inputs	−0.3 V to +5.5 V

Again, there is a restriction with OVDD in respect to DVDD. The Absolute Maximum Ratings state that OVDD must be less than or equal to 0.3 V above DVDD, while DVDD is less than 2.3 V. Once DVDD reaches 2.3 V during power-up, the restriction no longer applies. If this restriction is not observed, damage to the AD7621 (and AD7623) is likely (see Figure 1).

So, a possible general power-up sequence is as follows: AVDD, DVDD, OVDD, V_{REF}. But each application is different and requires analysis. Note that powering down a device is also just as important as powering up a device. Do not forget that the same specifications apply. A classic power-up/power-down sequence for the AD7621 is shown in Figure 1.
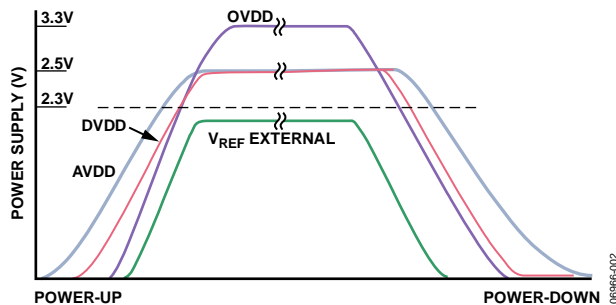

Figure 1. Possible Power-Up/Power-Down Sequence—AD7621 (Rev. 0)

The same case for the analog inputs and reference are true for these ADCs as previously described. Applying voltage to any analog input pin can cause the ESD diodes to become forward-biased, thus powering up the analog core in an unknown state.

The digital inputs and outputs for these ADCs are slightly different as these devices should accommodate 5 V digital inputs. These are a faster migration of the AD7654, both the digital inputs and outputs are related to the OVDD supply, because this can accommodate the higher 3.3 V. Note that the digital input restriction is limited to 5.5 V as opposed to DVDD + 0.3 V as in the AD7654.

SIGMA-DELTA ADC EXAMPLE

The AD7794 sigma-delta (Σ-Δ) 24-bit ADC is another good example. Table 3 shows an excerpt from the Absolute Maximum Ratings section of the AD7794 (Rev. D) data sheet.

Table 3. Absolute Maximum Ratings for the AD7794 (Rev. D)

Parameter	Rating
AV_{DD} to GND	−0.3 V to +7 V
DV_{DD} to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to DV_{DD} + 0.3 V

The issue that arises here is with respect to the reference voltage. It must be less than AV_{DD} + 0.3 V. Therefore, AV_{DD} must be powered up before or at the same time as the reference voltage.

POWER SUPPLY SEQUENCERS

Analog Devices offers a larger range of devices for correct sequencing of power supplies. Generally, they operate when the output voltage of the first regulator reaches a preset threshold and a time delay occurs before enabling subsequent regulators to power up. A similar procedure occurs during power down. They can also be used to sequence logic signals such as power good signals, which may apply a reset to a device or micro-processor or simply indicate that all power supplies are valid. Power sequencers from Analog Devices can be found at http://www.analog.com/sequence.

RECOMMENDATIONS

Most circuits nowadays with high speed and low power require-ments need multiple power supplies on a PCB such as +1.8 V, +2.0 V, +2.5 V, +3.3 V, +5 V, −5 V, +12 V, and −12 V. Powering these supplies on the PCB is not a task to be taken lightly. A correct and reliable power-up and power-down sequence is required and must be analyzed thoroughly. Doing this discretely is becoming more and more difficult. A power sequencing IC is the solution for power supply sequencing, where a code change can change the order of the sequence rather than a layout change on the PCB.

NOTES

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