

## Interfacing the ADSP-BF533/ADSP-BF561 Blackfin® Processors to High Speed Parallel ADCs

by Jeritt Kent and Jeff Sondermeyer

### INTRODUCTION

This application note describes how to interface the [ADSP-BF533/ADSP-BF561](#) Blackfin processors parallel peripheral interface (PPI) to a high speed analog-to-digital converter (ADC). The document focuses on the [AD6652](#) from Analog Devices, which is a 12-bit, 65 mega samples per second (MSPS) intermediate frequency (IF) to baseband diversity receiver. This interface, however, relates to many other applications. The AD6652, though most often indicated as a communications receiver, is also suitable for imaging, medical ultrasound, instrumentation, and test equipment.

In this document, specific references to processors in the ADSP-BF531/ADSP-BF532/ADSP-BF533 Blackfin family are identified as ADSP-BF533 processors. In generic references, Blackfin processors include the ADSP-BF534/ADSP-BF536/ ADSP-BF537 family as well as ADSP-BF561 dual-core processors.

### ABOUT BLACKFIN PROCESSORS

In addition to providing a simple, low cost connection to a wide set of communication receivers, the Blackfin processor 16-bit PPI port provides a glueless connection to devices that are compliant with Standard 656 of the International Telecommunications Union (ITU). The ITU-R 656 standard specifies the interface to interlaced standard-definition TV systems with an aspect ratio of 4:3. Luminance (Y) and multiplexed chrominance (CbCr) information is sampled at a rate of 13.5 MHz, and the resulting output streams are multiplexed into a single 8-bit or 10-bit data stream at a clock rate of 27 MHz. The PPI is linked to an ITUR 656-compliant device by connecting the data lines and a clock. In this interface, all control codes are embedded in the data stream.

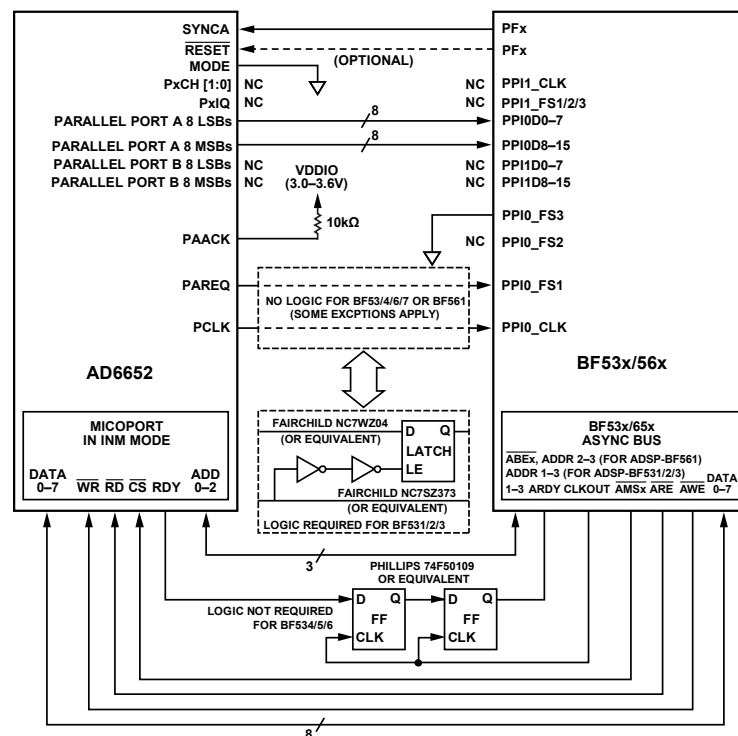


Figure 1.

The PPI can also use external frame syncs in place of embedded control signals to frame data being sent to a liquid crystal display (LCD) or data taken from a CMOS sensor. This data mode can also be used to connect to a wide range of ADCs and digital-to-analog converters (DACs). For this application, the Blackfin processor's PPI is used with some added external logic to accept 16-bit ADC data at rates as high as 28 Mwords/s.

Direct memory access (DMA) is a critical component that dictates the maximum data throughput of a processor. Blackfin processors incorporate a sophisticated DMA controller capable of moving data into and out of memory without consuming any core processing cycles. Blackfin processors employ an advanced DMA feature called two-dimensional DMA that enables data to be sorted into different data buffers on the fly.

The AD6652 has four independent data channels. Because each of these channels generates in-phase (I) and quadrature (Q) data, a typical algorithm processes each channel and I/Q data separately. Blackfin processors uniquely handle this sorting without core involvement. Because of other system-related considerations, this document provides a thorough analysis to determine the maximum data throughput for this application.

## CONFIGURING THE AD6652 VIA THE MICROPORT

The AD6652 uses a microport to configure the address and control register settings via an indirect addressing scheme. The external memory map (composed of external registers) is used to access the internal memory maps, that comprise a channel memory map and an output port memory map. The 4-channel memory pages are decoded using A[9:8], given in External Memory Register 7 of the AD6652 access control register (ACR).

When interfacing to Blackfin processors, set the microport to Intel® nonmultiplexed mode (INM), as shown in Figure 1. To configure the Blackfin processor asynchronous memory bus, use the  $\overline{\text{CS}}$ ,  $\overline{\text{RD}}$ , and  $\overline{\text{WR}}$  inputs on the AD6652. The AD6652 RDY signal, produced by the microport, signals the Blackfin processor via its ARDY pin that an access has been completed. RDY goes low at the start of the access and is released when the internal cycle is complete. Refer to Figure 31 and Figure 32 in the AD6652 (Rev. 0) data sheet. A quick analysis of AD6652 microport timing,  $t_{\text{SC}}$  and  $t_{\text{HC}}$ , implies that the  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  inputs have a setup and hold time relative to the rising edge of  $\text{CLK}_{\text{AD6652}}$ . However, if  $t_{\text{SC}}$  is not met,  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  are sampled on a subsequent rising edge of  $\text{CLK}_{\text{AD6652}}$ . For all practical purposes,  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  may be considered asynchronous inputs.

Assertion and deassertion of the Blackfin processor ARDY pin must meet the data sheet setup and hold times ( $t_{\text{SARDY}}$  and  $t_{\text{HARDY}}$ ). Note that ARDY setup before  $\text{CLKOUT}$  ( $t_{\text{SARDY}}$ ) is 4 ns, per the ADSP-BF531/ADSP-BF532/ADSP-BF533 (Rev. B) data sheet. Failure to meet these synchronous specifications can result in metastable behavior internally on the Blackfin processor. Use the  $\text{CLKOUT}$  signal to ensure synchronous

transitions of ARDY. Therefore, per Figure 1, a dual flip-flop is added to synchronize the two devices and to meet the setup time ( $t_{\text{SARDY}}$ ). Philips Semiconductors has designed such a device in the 74F50109. Setup time violations can cause a single flip-flop to exhibit metastability and an invalid output at Q. For this reason, a dual flip-flop approach is used here. One result to this approach is the addition of two Blackfin processor wait states to account for the two-clock delay. Any choice of flip-flop suffices, as propagation delays are hidden by the dual clocking. Assuming worst-case timing of the AD6652 (no maximum  $t_{\text{DRDY}}$  given), the wait states are calculated per Equation 4. Note that, per the ADSP-BF533 Blackfin Processor Hardware Reference (Rev. 3.1), BxRDYPOL must be set to 1 (transition completes if ARDY is sampled high). Blackfin processors support a maximum of 15 wait states; thus, the maximum ratio of  $\text{SCLK}$  to  $\text{CLK}_{\text{AD6652}}$  is 13.

The  $\text{CLK}_{\text{AD6652}}$  performs a dual function on the AD6652, acting not only as the ADC sampling clock for the front end receiver, but also as the clock for the digital filtering section. To take advantage of over-sampling,  $\text{CLK}_{\text{AD6652}}$  should be close to the 65 MSPS maximum, resulting in processing gain and optimized filter characteristics resulting from a high number of taps. The AD6652 incorporates two interpolators (a resampling cascaded integrator comb, rCIC2, and an interpolating half-band), and three decimators (an rCIC2, a fifth-order cascaded integrator comb, CIC5, and a RAM coefficient filter, RCF), which are used to set the output data rate as a function of  $\text{CLK}_{\text{AD6652}}$ . The interpolating half-band filters interpolate by a factor of two or are bypassed.

## NARROW-BAND APPLICATION EXAMPLE

Output data rate = 270.833 kSPS

PCLK = 15.36 MHz

$\text{CLK}_{\text{AD6652}}$  = 61.44 MHz

SCLK = 133 MHz

Number of wait states =  $(133/15.36)_{\text{ceil}} + 2 = 11$

If other peripherals on the Blackfin processor asynchronous memory bus require ARDY, a logic OR is required. Note that a wire-OR also suffices, but this requires open-collector RDY outputs from all devices. The external memory-mapped microport is the only way to gain access to the 4-channel address register pages and the output port control register page. With the exception of Channel Address 0xA9 (see the Channel Address Memory Map table in the AD6652 data sheet), this section specifically discusses configuration of the output port control registers (see the Memory Map for Output Port Control Registers table in the AD6652 data sheet).

First, the ACR is initialized so that all chips and all channels have access. To access the registers of Output Port A and Port B, Bit 5 of External Address 3 (the sleep register) must be set high. When this bit is written as 0, the channel memory map is selected. Referring to the External Memory Map table in the

AD6652 data sheet, set the Microport Address Bus A[2:0] to 0b011 and the Bidirectional Microport Data Bus D[7:0] to 0x20 (see Listing 1).

The AD6652 incorporates two independent, 16-bit parallel ports for output data transfer. To minimize package ball count, the 8 least significant bits (LSBs) of each 16-bit port are shared with their respective parallel port data bits. This means that an output port can transmit 16-bit parallel data or 8-bit link port data, but not both. This application note focuses on 16-bit parallel data; it does not discuss the link ports typically allocated for use with ADSP-TS10x *TigerSHARC*® processors, another family in processors from Analog Devices. Applications with ADSP-BF533 Blackfin processors use only one of the parallel ports—in this case, Port A. ADSP-BF561 Blackfin processors, which have two (2) PPI ports, can interface to both of the 16-bit-wide AD6652 parallel ports, if required.

To interface the AD6652 to the Blackfin processor PPI port, configure the AD6652 for master mode parallel port clock (PCLK) and configure the parallel port channel mode for 16-bit I and Q interleaved. Tie the AD6652 PCLK to the Blackfin processor PPI\_CLK, as shown in Figure 1. As a result, the signals are used interchangeably, depending upon the part being discussed.

The AD6652 channel address register (CAR) located at External Address 6 is first written by setting A[2:0] to 0b110. Port clock master/slave mode is configured using the port clock control register at Address 0x1E—D[7:0] is 0x1E. Bit 0 of this address determines whether PCLK is supplied externally (slave mode) or derived internally (master mode). For this application, the AD6652 is the master, enabled by setting Bit 0 of Address 0x1E high. This is done by setting A[2:0] to 0b010 (DR2) and D[7:0] to 0x00. Subsequently, A[2:0] is set to 0b001 (DR1) and D[7:0] is set to 0x00. In master mode, PCLK is an output frequency equal to the AD6652 clock frequency ( $CLK_{AD6652}$ ) divided by the PCLK divisor. As values for the PCLK divisor [2:1] can range from 0 to 3, integer divisors of 1, 2, 4, or 8, respectively, can be obtained. The highest PCLK rate in master mode is 65 MHz (PCLK divisor is 1). Finally, A[2:0] is set to 0b000 (DR0), and Bit 0 of D[7:0] is set high. Bits [2:1] set the PCLK divisor. When External Address DR0 is written, an internal access is triggered to the AD6652, based on the addresses indicated in the ACR and the CAR. This is why External Address 0 must always be written last (see Listing 1).

### Listing 1

```
/* Address/Data Configuration for AD6652 -
Master Mode, 16b Interleaved I and Q
Script Syntax :
micro_write(binary A[2:0], hex D[7:0]); */

/* Turn off Auto-Increment, Broadcast in ACR*/
micro_write(7,0x00);

/* Sleep Reg - Bit 5 high */
micro_write(3,0x2F); /* all channels asleep */

/*Port Clock Control - PCLK divisor is 1*/
micro_write(6, 0x1E); micro_write(2, 0x00);
micro_write(1, 0x00); micro_write(0, 0x01);

/* Link Port Control A- bit 7 low to disable */
micro_write(6, 0x1B); micro_write(0, 0x00);

/*Parallel Port Control A - 16b interleaved I/Q
channel mode*/
micro_write(6, 0x1A); micro_write(0, 0x00);

/*Output Control Register - Bit 5 is high to
set 16b format*/

micro_write(6, 0xA9); micro_write(0, 0x40);
```

Parallel port configuration is specified by accessing port control register Address 0x1B and Address 0x1D for Parallel Port A and Port B, respectively. This programming procedure is similar to that discussed previously. When Bit 7 of Address 0x1B is low, Link Port A is disabled, and Parallel Port A is enabled. Similarly, Parallel Port B is enabled when Bit 7 of Address 0x1D is low.

Set Bit 5 and Bit 0 of Address 0x1A low to enable 16-bit interleaved I and Q channel mode on Parallel Port A. Likewise, setting Bit 5 and Bit 0 of Address 0x1C low enables the same mode on Parallel Port B. In channel mode, I and Q words from each channel are directed to the parallel port, bypassing automatic gain control (AGC). For this ADSP-BF533 Blackfin processor application, only Parallel Port A is used.

The 16-bit interleaved format provides I and Q data for each output sample on back-to-back PCLK cycles. Both I and Q words consist of the full port width of 16 bits. Data output is triggered on the rising edge of PCLK when both PAREQ and P<sub>A</sub>ACK are asserted (the A in these signal names substitutes for x in Figure 2, designating the A output port). To set this 16-bit format, program the CAR for Internal Address 0xA9. This output control register is 10 bits wide, and Bit 5 in DR0 must be set high. In Figure 1, a Blackfin processor GPIO pin (PFx) drives the RESET pin of the AD6652, ensuring proper host setup before the microport is accessed. The AD6652 (Rev. 0) data sheet has additional information on the microport in the section entitled “Microport Control.” Designers are also encouraged to read the “Design Guidelines” section.

## SYNCHRONIZATION OPTIONS FOR MULTICHANNEL APPLICATIONS

Flexible channel multiplexing in the DDC stage allows one to four channels to be interleaved onto one parallel output port. Bit 0 low and Bit 1 to Bit 4 of Port Control Register Address 0x1A and Address 0x1C determine which combination of the four processing channels is output. Data should be read from the output port when it is available, otherwise the sample is overwritten when the next new data sample arrives. This occurs on a per-channel basis; that is, a Channel 0 sample is only overwritten by a new Channel 0 sample. The order of data output depends on when data arrives at the port, which is a function of the total decimation rate and start hold-off values (see Equation 3). Priority order, when data arrives simultaneously, is, from highest to lowest, Channel 0, Channel 1, Channel 2, then Channel 3. There are two types of synchronization methods: *Soft\_Sync* and *Pin\_Sync*. The first method is initiated over the microport using a software routine. There is more information regarding this in the “Channel/Chip Synchronization” section of the [AD6652](#) (Rev. 0) data sheet. The second method, a hardware method, relies on an external stimulus that is attached to one of the four synchronization input pins (*SYNC A*, *SYNC B*, *SYNC C*, and *SYNC D*). In both cases, a logic high triggers the synchronization process. Both methods can be used simultaneously by setting the appropriate qualifiers.

A majority of applications, including those for a single communications standard, configure identical filters for all four channels of the AD6652. The only difference is the numerically controlled oscillator (NCO) frequency that places the filter in the frequency spectrum. For this reason, the internal registers of the AD6652 are programmed such that all four registers are hardware-synchronized to a single pin, *SYNCA*, connected to a Blackfin processor GPIO Pin *PFx* (see Figure 1). This simplifies the output data to format under a singular frame-sync envelope. For this case, the default priority order (0, 1, 2, and then 3) provides the data in a burst-like mode as four sequential I and Q pairs (eight 16-bit words). Data continues to be processed in this manner with dead time between multichannel bursts directly proportional to the filter latencies. If the channel filters are different, then the start hold-off registers at Channel Address 0x83 can be used via Equation 3 to force simultaneity, thus priority order, or another preferred sequence. Lower speed applications (less than 1 MHz) can use an alternate synchronization method. The *PACH*[1:0] and *PBCH*[1:0] pins form a 2-bit binary number, identifying the source channel of the current data-word. With the channel order known, either the LSB or MSB of the *PACH* or *PBCH* bus can drive another Blackfin processor GPIO pin (*PFx*) as a fast hardware interrupt to identify the start of a burst sequence.

## CONFIGURING THE BLACKFIN PROCESSOR AND AD6652 INTERFACE

By default, the polarity clock bit (*POLC*) is low, and the Blackfin processor references frame sync delay timing with respect to the falling edge of *PPI\_CLK*. Because the AD6652 frame sync (*PAREQ*) is an active-high output synchronous to *PCLK* on its rising edge, set this bit high to *POLC* = 1 (see Listing 2). This prepares the slave Blackfin processor for a frame sync delayed off the rising edge of *PCLK*.

Conversely, data is sampled on the rising edge of *PCLK*, by default. With *POLC* high, data is sampled at the *PPI* on the falling edge corresponding to the timing presented by the AD6652 master shown in Figure 3.

A logic high on *PAACK* when *PAREQ* is high causes the parallel port to shift out data according to the programmed data mode—16-bit I and Q interleaved. This application does not require a handshake, so *PAACK* is tied high with an external pull-up resistor (see Figure 1). When the data becomes available, it is shifted out one *PCLK* cycle after the assertion of *PAREQ* (see Figure 2).

Because data is delayed for one *PCLK* cycle (see Figure 32 in the [AD6652](#) Rev. 0 data sheet), set *PPI\_DELAY* = 1 in the Blackfin processor software. This is shown in Listing 2. Though this delay is required for the AD6652, it may not be needed for converters with different frame sync to data timing.

*PAREQ* timing is internally fixed relative to *PCLK* and cannot be adjusted. Although *PAREQ* from the AD6652 is synchronous with the rising edge of *PCLK*, the maximum delay ( $t_{DPREQ}$ ), between these edges is only 1 ns (see Figure 2). The Blackfin processor requires more delay; its timing requirements are examined next.

## EXTERNAL LOGIC REQUIREMENTS FOR ADSP-BF533 BLACKFIN PROCESSORS

The remaining portion of this document focuses on the external logic required for ADSP-BF533 Blackfin processors to meet the delay and hold time requirements shown in Figure 3. For many Blackfin processors, including the ADSP-BF561 and ADSP-BF534/ADSP-BF536/ADSP-BF537, no external logic is necessary (some exceptions apply, as described in the appropriate processor anomaly list). These devices incorporate the external logic shown in Figure 1 along with other enhancements (refer to the timing information in the respective data sheet).

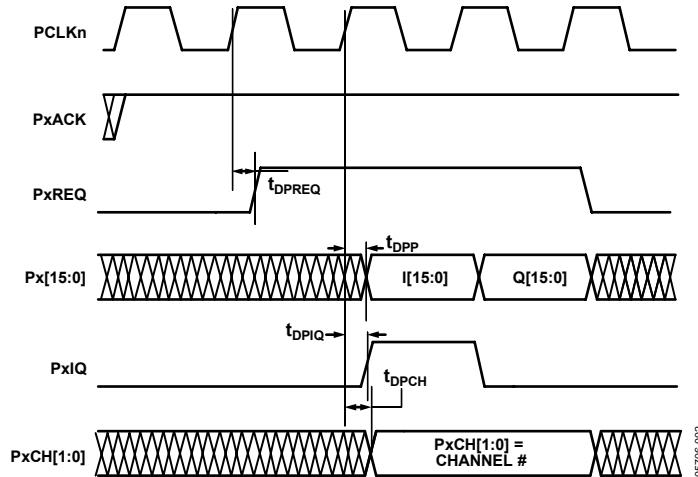


Figure 2. AD6652 Parallel Input Mode 16-Bit Interleaved Data Timing Diagram

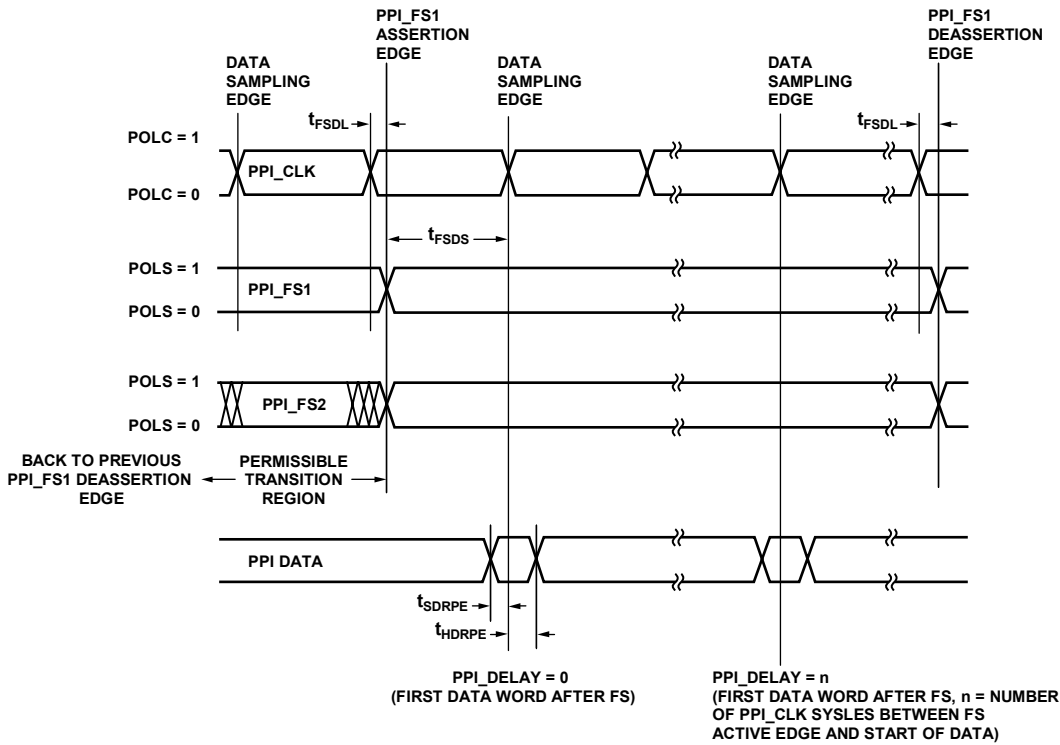


Figure 3. ADSP-BF531/BF532/BF533 PPI Timing in GP Input Mode with External Frame Sync

The ADSP-BF533 Blackfin processors require that the frame sync assertion edge occur a minimum of 5.5 ns ( $t_{FSDS}$ ) before the next data sampling edge of PPI\_CLK (see Figure 3). It is imperative that PAREQ transition only when PCLK is completely stable. In addition, if the PAREQ transition edge is insufficiently delayed after the corresponding edge (that is, the rising-to-rising or falling-to-falling) of PCLK ( $t_{FSDL}$ ), data is never latched into the PPI. Possible contributors to this issue

include clock jitter, propagation delay tolerances, temperature, fanout as a result of reuse of PCLK for other signaling, non-symmetric board layout, and edge slewing. The design task, then, for this application, is to extend the delay of the PAREQ (PPI\_FS1) signal after the rising edge of PCLK and to ensure that both  $t_{FSDL}$  and  $t_{FSDS}$  are met. There are two ways to accomplish this.

The first (preferred and fail-safe) method is to use a level-sensitive latch triggered from a delayed version of PCLK (see Figure 1) as two inverter delays. This solution covers the previously mentioned problems that may cause PCLK to lag the frame sync signal. The latch passes the D input when a delayed PCLK reaches the  $V_{inh}$  level of the latch enable (LE). The retimed frame sync (PAREQ) must stay high for the entire data window and meet the timing shown in Figure 3. A flip-flop is not nearly as effective because flip-flops are edge triggered. In this case, an early PCLK, ahead of frame sync, causes an asserted frame sync to be missed for an entire PCLK cycle.

Two NC7WZ04s (dual inverters) from Fairchild Semiconductor (or equivalent) can be used in series with the PCLK from the AD6652 to drive the enable pin of the latch. The specifications at a 3.3 V supply are given for 50 pF and 15 pF. For this application, the first inverter sees the input capacitance of the second inverter (4 pF), which sees the input capacitance of the latch enable pin (3 pF). Extrapolating the data gives a minimum combined propagation delay of approximately 1.4 ns over the temperature range  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

**Table 1. ADSP-BF531/ADSP-BF532/ADSP-BF533 Timing Requirements**

Parameter	Min
$t_{FSDL}$ External Frame Sync Delay	2.0 ns
$t_{FSDS}$ External Frame Sync to Data Sampling Edge	5.5 ns
$t_{SDPE}$ Receive Data Setup Before PPI_CLK	2.0 ns
$t_{HDRPE}$ Receive Data Hold After PPI_CLK	4.0 ns

One latch to consider is the NC7SZ373, also from Fairchild Semiconductor. Linearizing the worst-case (minimum) propagation delay from LE to the output (Q) at 3.3 V, over the industrial temperature range for an 8 pF load at the PPI\_FS1 input on the Blackfin processor, gives 0.9 ns. Because the NC7SZ373 latches data on the falling edge of latch enable, there is no setup time requirement. This is another important reason for setting POLC = 1. Additional margin obviously exists for designs in the commercial temperature range.

$$t_{FSD}(\min) = t_{PROP\_INV}(\min) + t_{PROP\_LE\_to\_Q}(\min) \text{ sec} \quad (1)$$

$$f_{PCLK}(\max) = 1/(2 \times (t_{PROP\_INV}(\max) + t_{PROP\_LE\_to\_Q}(\max) + 5.5 \text{ ns})) \text{ Hz for a 50\% PCLK and } t_{DPREQ}(\max) < t_{OP\_INV}(\min) \quad (2)$$

$$T_{latency} = MrCIC2 \times (MCIC5 + 7) + N_{taps} + 26 + \text{Start Holdoff Counter} \times t_{CLK} \text{ sec} \quad (3)$$

where:

$MrCIC2$  and  $MCIC5$  are decimation values for the rCIC2 and CIC5 filters.

$N_{taps}$  is the number of RCF taps chosen.

$$t_{CLK} = 1/f_{CLK\_AD6652}.$$

$$\text{Number of Blackfin processor wait states} = \lceil (SCLK/CLK_{AD6652})_{ceil} + 2 \rceil \quad (4)$$

where:

$ceil$  is the integer round-up of the fraction.

maximum number of wait states is 15.

It is important to evaluate the minimum propagation delays at temperature, voltage, and load for the selected inverters and latch to ensure that the minimum 2 ns  $t_{FSDL}$  is met (see Figure 3). Using the two NC7WZ04s and the NC7SZ373, Equation 1 gives a value for  $t_{FSDL}(\min)$  of 2.3 ns. This meets the specification in Figure 3. The maximum propagation delays are used to determine the maximum allowed PCLK frequency for an application. Extrapolating for the correct loads at 3.3 V over the industrial temperature range, the maximum combined inverter delay is approximately 7.8 ns— $t_{PROP\_INV}(\max)$ —and the maximum propagation delay of the latch is 4.5 ns— $t_{PROP\_LE\_to\_Q}(\max)$ . Given that PAREQ can lag PCLK by as much as 1 ns, Equation 2 shows the maximum allowed 50% duty cycle PCLK as 28 MHz— $f_{PCLK}(\max)$ . Jitter concerns are mitigated, as PCLK and PAREQ are correlated; it is PCLK that releases PAREQ on the AD6652.

This approach assumes tight proximity of the AD6652 to the Blackfin processor and singular connectivity of the clock and frame sync lines; that is, no fanout to drive other devices. Especially for high speed designs, any load placed on PAREQ must be considered in the timing, as it is assumed that the load seen on the AD6652 PAREQ pin is reasonably comparable to that seen by PCLK before the pair of inverters. Timing specifications for these signals are based upon 40 pF loads.

Because of the undesired effects that a non-50% duty cycle sampling would have on converter performance (including the AD6652), it should be assumed that, when interfacing to an ADSPBF533 Blackfin processor, 28 MHz is the maximum allowed PCLK (see the Interface Guidelines section). The PCLK duty cycle tracks the CLKAD6652 duty cycle, with the exception of small edge mismatches in the clock tree. But this PCLK limit does imply some essential constraints. ADSP-BF533 Blackfin processors should not be considered for most wide-band applications with the AD6652; the Universal Mobile Telecommunications System (UMTS) is an example.

Much work has been performed by Analog Devices with digital filter scripts tuned to a 61.44-MSPS sample rate. This allows simple modifications to be enabled for narrow-band standards like global system for mobile communication (GSM). As a result, with PCLK divisors of only 1, 2, 4, and 8 allowed, the maximum PCLK is 15.36 MHz. For systems that output all four channels of in-phase and quadrature information, PCLK is  $9 \times$  the output data rate,  $(2 \times 4) + 1$ , as shown in Figure 2. Even with the coprocessing capability of the AD6652, interlacing output data at 1.92 Mbps to generate an aggregate 3.84 Mbps (to the UMTS standard), the 9 PCLK cycles required to output this data is 586 ns ( $9 \times 1/15.36$  MHz). This is greater than the 521 ns needed to meet the output data rate. However, narrow-band applications like GSM are not affected by this limitation.

For lower speed applications, a buffer such as the NC7WV07 with a 4.0 ns maximum propagation delay, or alternatives with even higher delays, can be implemented in series with the converter frame sync signal. Another less robust option is to use an even number of inverters or a buffer in the frame sync path to act as a delay—2 ns is sufficient (see  $t_{FSDL}$  in Figure 3). It is important, though, to ensure that the delay is not too long, as the assertion edge of PAREQ must occur at least 5.5 ns ( $t_{FSDS}$ ) before the data sampling edge of PCLK to meet internal hold specifications.

In summary, the external logic shown in Figure 1 effectively converts a level-sensitive signal (PPI\_FS1) into an edge-sensitive frame sync. Again, designs for all future Blackfin processor derivatives incorporate this logic internally.

## CONFIGURING PPI AND DMA

The Blackfin processor PPI can be configured as an input or output bus for many different applications. For this application, the PPI is configured for general-purpose input mode, single frame sync, and clock polarity (POLC = 1).

The C code for configuring the PPI port and DMA is shown in Listing 2. The PPI\_FS1 signal is tied to PAREQ via the latch re-timing circuit. This signal frames all eight words of data from four channels (I and Q for each channel). The Blackfin processor DMA transfers eight words of data and interrupts on completion of each transfer. Although the data can be sorted between transfers by the core, the use of two-dimensional DMA is preferred, as it can be used efficiently to sort Channel 1 to Channel 4 (not shown in Listing 2).

## Listing 2

```
/* Configure PPI - RX, 16 bits, GP mode,
external frame sync FS1 */

*pPPI_CONTROL = 0x780c; /* POLC = 1
(default for POLS = 0, this is good as the
frame sync is active high)*/
*pPPI_DELAY = 0x0001; /* 1 PCLK delay to ignore
1st data from AD6652 */
*pPPI_COUNT = 0x0007; /* 8 words transferred */

/* Configure DMA0 - Memory write, 16 bits, 1D
interrupt, autobuffer mode */

*pDMA0_CONFIG = 0x1086;
*pDMA0_START_ADDR = PPI_Buffer;
*pDMA0_X_COUNT = 0x0008; /* 8 words */
*pDMA0_X_MODIFY = 0x0002; /* 16-bit data */
```

If the designer is prototyping with earlier X grade revisions of the ADSP-BF561 and ADSP-BF534/ADSP-BF536/ADSP-BF537 Blackfin processors, provisions should be made for production-grade silicon on the printed circuit board (PCB). Bypass the external logic with 0  $\Omega$  resistors.

This entire system can be built and tested using the

- [AD6652BC/PCB](#) converter board.
- [ADDS-BF-EZEXT-1](#) extender card.
- [ADDS-BF533-EZ-KIT Lite® evaluation board](#) or the [ADD-BF561-EZ-KIT Lite® evaluation board](#).

To connect the AD6652BC/PCB to the ADDSBF-EZEXT-1, a modified ribbon cable may be required to provide the necessary external logic discussed in this document.

## SUGGESTED READING

[ADSP-BF53x/ADSP-BF56x Blackfin Processor Programming Reference](#)

## INTERFACE GUIDELINES

In conclusion, follow these guidelines when interfacing parallel ADCs, like the [AD6652](#), to the Blackfin PPI port(s):

- The Blackfin CLKIN can drive the onboard phase-locked loop (PLL) for multiplication—see the specific data sheet for values. The output of the PLL voltage controlled oscillator (VCO) can then be divided by 1, 2, 4, or 8 to generate the core clock (CCLK) and can also be divided by integers from 1 to 15 to generate the system clock (SCLK).

$$SCLK \leq CCLK$$

- The Blackfin PPI\_CLK frequency cannot exceed 66 MHz.  
 $(PCLK = PPI\_CLK) \leq SCLK/2$
- Keep the assertion edge of frame sync at least 5.5 ns,  $t_{FSDS}$ , prior to the data sampling edge of PPI\_CLK (falling edge for POLC = 1) to meet internal Blackfin hold specifications (see Figure 3).
- Do not allow the external frame sync delay,  $t_{FSDL}$ , to be less than 2 ns (see Figure 3).
- The minimum attainable external frame sync delay,  $t_{FSDL}$ , for the ADSP-BF531/ADSP-BF532/ADSP-BF533 is set by the external logic:

$$t_{FSDL}(min) = t_{PROP\_INV}(min) + t_{PROP\_LE\_to\_Q}(min) \text{ sec}$$

- If PCLK is derived from the converter sampling clock, it is at a 50% duty cycle. The maximum allowed PCLK for Blackfin processors under this condition is 28 MHz. This can imply strict constraints on the application.
- The maximum PPI\_CLK frequency at a 50% duty cycle for this application is:

$$f_{PPI\_CLK}(max) = 1/[2 \times (t_{PROP\_INV}(max) + t_{PROP\_LE\_to\_Q}(max) + t_{DPREQ}(max) + 5.5)].$$

When using the AD6652 and the logic described in this article,  $f_{PPI\_CLK}(max) = 28 \text{ MHz}$ .

- Do not allow the PPI\_CLK high time to be less than 7.5 ns. This is restricted by the Blackfin PPI timing specifications, but, again, the maximum delays for the external logic determine the maximum PPI\_CLK frequency.
- Do not allow the PPI\_CLK low time to be less than 3 ns. This is restricted by the Blackfin PPI timing specifications, but be aware that the interfacing converter may have more stringent requirements (for example, the AD6652 minimum PCLK low time is 6.2 ns).
- Consider synchronization issues when moving multiple data channels. DMA data latencies through the PPI port can make it difficult to obtain the correct channel order.