ANALOG DEVICES

AN-750
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106 • Tel: 781/329-4700 • Fax: 781/326-8703 • www.analog.com

ADE7758 Phase Dropout Detection for VAR Calculation

by Rachel Kaplan

INTRODUCTION

The ADE7758 is a polyphase, multifunction energy metering IC that performs kWh, kVAh, kVARh, and rms current and rms voltage measurements. This application note describes how phase dropout affects VAR calculation in the ADE7758, the solution to detect phase dropout with the ADE7758, and how to avoid VAR errors.

PHASE DROPOUT AND THE ADE7758

The ADE7758 measures the line frequency of one phase at a time. If a phase drops out, the line frequency measurement on that phase can be incorrect due to offset or noise causing erroneous zero-crossing detection. Compensation for reactive power calculation is based on the line frequency measurement of one phase. If the phase used for frequency measurement drops out, this can induce error to the reactive power calculation of the other phases. To solve this problem, the meter needs to detect the phase dropout and switch the frequency measurement to an active phase. The phase used for frequency measurement can be changed using Bit 0 to Bit 1 in the measurement mode register (MMODE [7:0], Address 0x14). Table I shows the setting of the two bits, MMODE [1:0], for different phase frequency measurement.

Table I. Phase Selection for Frequency Measurement

MMODE [1]	MMODE [0]	Phase
0	0	A
0	1	B
1	0	C

VAR CALCULATION

Reactive power is defined as the product of the voltage and current waveforms when one of these signals is phase shifted by 90°. There is a phase-shift filter in the ADE7758 that introduces a 90° phase shift in the current channel of the reactive energy datapath. The magnitude and phase response of the phase-shift filter is shown in Figure 1 and Figure 2, respectively. Because the phase-shift filter has a nonunity magnitude response, a compensation based on line frequency is implemented to achieve accurate reactive power calculation around fundamental frequency.

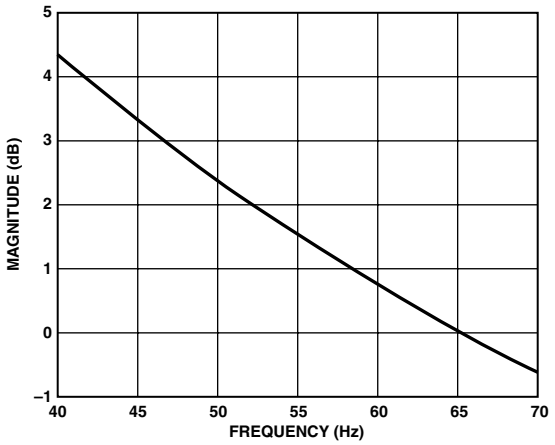

Figure 1. Magnitude Response

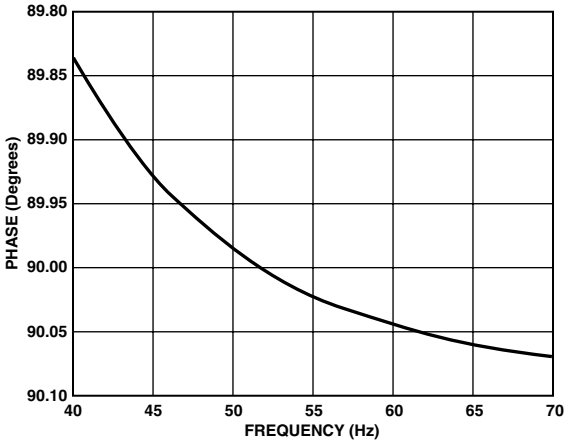

Figure 2. Phase Response

ZERO-CROSSING TIMEOUT

The ADE7758 measures the line frequency using zero-crossing detection circuits. Refer to the Zero-Crossing Detection section in the data sheet for more details about zero-crossing detection.

The ADE7758 has a zero-crossing timeout interrupt for each phase. If no zero crossing is detected for a time period determined by the zero-crossing timeout register (ZXTOUT [15:0], Address 0x1B), the corresponding zero-crossing timeout detection bit in the interrupt status register (STATUS [23:0], Address 0x19) is set. An active low on the IRQ output also appears if the corresponding bit in the interrupt mask register (MASK [23:0], Address 0x18) is set. Figure 3 shows the mechanism of the zero-crossing timeout detection when the line voltage of Phase A stays at a fixed dc level for more than 384/CLKIN × ZXTOUT seconds. Ideally, if one phase drops out, no zero crossing is detected for this phase and the zero-crossing timeout bit of the corresponding phase is set in the status register after 384/CLKIN × ZXTOUT seconds. However, noise due to possible channel offset may cause the part to continue detecting zero crossing during phase dropout. Thus, no zero-crossing timeout request is generated. SAG detection can be used in this case to detect if the phase has dropped out.

Note that the zero-crossing detection signal is used for the line-cycle accumulation mode, zero-crossing interrupt, and zero-crossing timeout interrupt. Thus, in phase dropout condition, the part should not use the dropped phase for zero-crossing detection.

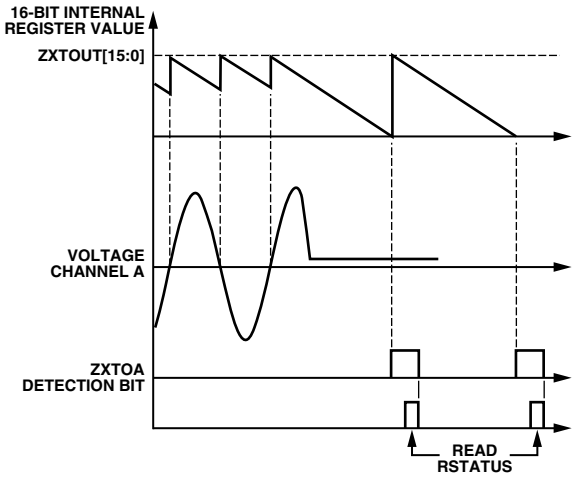

Figure 3. Zero-Crossing Timeout Detection

SAG DETECTION

The ADE7758 can also detect voltage SAG. When the absolute value of the line voltage of any phase drops below a peak value set by the SAG level register (SAGLVL [7:0], Address 0x1E) for a number of half cycles set by the SAG line cycle register (SAGCYC [7:0], Address 0x1D), the corresponding bit in the status register is set. An active low on the IRQ output pin also appears if the corresponding bit in the MASK register is set. Figure 4 shows a line voltage falling below the threshold set in the SAGLVL register for nine half cycles. Since the SAGCYC register is set to 6, the SAG event is recorded at the end of the sixth half cycle. In conjunction with ZXTOUT, SAG can be used to detect when a phase has dropped out.

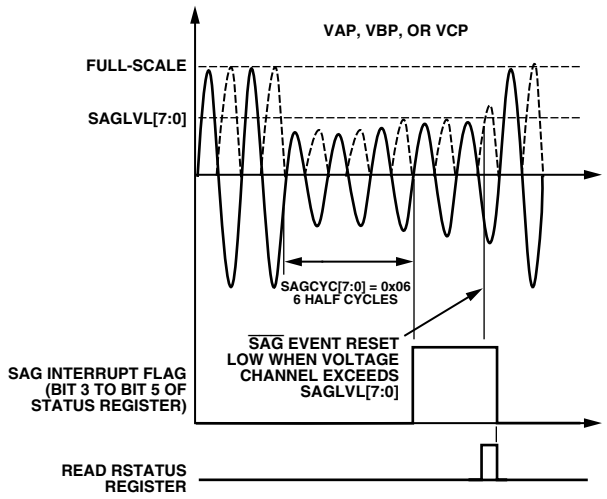

Figure 4. Voltage SAG Detection

SOLUTION

There are two solutions for phase dropout detection.

1. Use the combination of zero-crossing timeout interrupt and voltage SAG interrupt.

   Set the ZXTOUT register to a small value that satisfies the following equation: 384/CLKIN × ZXTOUT > 1/2*f*, where *f* is the line frequency. Set the ZXTO bits in the MASK register. If a phase drops out, an interrupt should occur after the time specified by the ZXTOUT register has elapsed. However, as mentioned previously, noise and offset on the voltage channel may cause the part to continue detecting zero crossing. Therefore, no ZXTOUT interrupt is generated. In this situation, SAG can be used to detect the phase dropout condition. If the SAG bits in the MASK register are also set and SAGLVL is set to a value that is larger than possible noise, an interrupt occurs after the number of half line cycles specified by the SAGCYC register. The SAGCYC register should be set to a very small value for the part to detect the phase dropout promptly. Once the interrupt occurs from either SAG or ZXTOUT, read the reset interrupt status register (RSTATUS [19:0], Address 0x1A) and check the SAG and ZXTO bits to determine which phase has dropped out. Then switch the frequency measurement to an active phase by changing Bit 0 to Bit 1 in MMODE register. Since zero-crossing detection is used for other measurement, the part should exclude the dropped phases from zero-crossing detection. The phases used for counting the number of zero crossings is selected by Bit 3 to Bit 5 in the line-cycle accumulation mode register (LCYCMODE [7:0], Address 0x17). Bit 3, Bit 4, and Bit 5 select Phase A, Phase B, and Phase C, respectively.

The steps to implement this phase dropout detection method are outlined as follows:

- Set ZXTOUT register, i.e., 0x12C(300d) for CLKIN of 10 MHz and line frequency of 50 Hz.
- Set SAGCYC register to a small value, i.e., 0x05.
- Set SAGLVL to a value larger than possible noise but smaller than the lowest expected value during normal operation, i.e., half full-scale value.
- Set Bit 3 to Bit 8 in the MASK register to enable SAG and ZXTO interrupts for all three phases.
- When an interrupt is detected, read the reset interrupt status register (RSTATUS [19:0], Address 0x1A) to find out which phase drops out by looking at the SAG and ZXTO bits.
- Switch the frequency measurement to an active phase by setting the MMODE register according to Table I.
- Exclude the dropped phase from zero-crossing detection by changing Bit 3 to Bit 5 in the LCYCMODE register.

2. Monitor the voltage rms value.

   We can read voltage rms registers periodically. When a phase drops out, the voltage rms register value of that phase is very small. If the phase used for frequency measurement drops out, change the frequency measurement to an active phase by setting the MMODE register according to Table I. However, this method is not recommended because continuously reading the voltage rms register may use a lot of system resources and power consumption.

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