INTRODUCTION

The ADN8831 is a thermoelectric cooler (TEC) controller that drives medium power TECs (<4 A current) with excellent temperature control resolution, stability, and high power efficiency. The ADN8831 integrates two high performance amplifiers dedicated to temperature sensing and thermal loop compensation, allowing direct interface to a thermistor, a resistive temperature device (RTD), or other temperature sensors.

When used in conjunction with the ADN8831 data sheet, this application note describes how to configure the ADN8831-EVALZ evaluation board (Version 4.0), and how to develop a real TEC control circuit with an ADN8831. The ADN8831 data sheet provides the detailed technical specifications and internal functional block diagrams, as well as the application design guidelines.

Important layout design guidelines are available in the Evaluation Board Layout section of this application note.

EVALUATION BOARD DESCRIPTION

The ADN8831 evaluation board offers a configurable design platform to work with various TECs and thermistors. On the evaluation board, the ADN8831 delivers and controls a bidirectional TEC current using two pairs of complementary MOSFETs in an H-bridge configuration.

With the on-board, adjustable components, the evaluation board provides configurability of temperature setpoint, temperature setpoint range, TEC current and/or voltage limits, and a PID compensation network. The temperature setpoint range (factory default) circuit, optimized to work with 10 kΩ negative temperature coefficient thermistors, can also work with other types of temperature sensors. The tunable PID compensation network allows the characteristic matching between the control circuit and the thermal load for achieving the fastest response time and temperature control stability. A green LED illuminates when the TEMOUT voltage is within ±100 mV of the TEMPSET setpoint voltage.

FUNCTIONAL BLOCK DIAGRAM

![Figure 1. Functional Block Diagram of ADN8831 Evaluation Board](image)
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GETTING STARTED

The ADN8831-EVALZ, shown in Figure 2, is set by factory default to deliver about 2 A bidirectional TEC current while working with a 10 kΩ thermistor at 25°C.

![Figure 2. Top View of the Evaluation Board](image)

The factory default setting determines the on-board component values of the temperature-to-voltage converter circuit and the PID circuit shown in Figure 3. With the on-board switches and potentiometers, the circuits in Figure 3 can be adapted to work with most TEC and thermistors used in telecommunications.

![Figure 3. Temperature and Compensation Network Circuits](image)

Referring to Figure 3, note that TEMPOUT refers to voltage signal outputs from Pin 4 (OUT1) and TEMPSET, a voltage signal, applied to Pin 5 (IN2P). These terms are used throughout this application note.

SWITCHES AND POTENTIOMETERS

<table>
<thead>
<tr>
<th>Switch</th>
<th>Function</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>CD</td>
<td>1 µF</td>
</tr>
<tr>
<td>S2</td>
<td>RD</td>
<td>24.9 kΩ</td>
</tr>
<tr>
<td>S3</td>
<td>RI</td>
<td>249 kΩ</td>
</tr>
<tr>
<td>S4</td>
<td>RP</td>
<td>249 kΩ</td>
</tr>
<tr>
<td>S5</td>
<td>CI</td>
<td>470 nF</td>
</tr>
<tr>
<td>S6</td>
<td>Standby/shutdown</td>
<td>Up/up</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Switch</th>
<th>Function</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>S6, Left Hand Side: Standby Control</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The ADN8831 is placed in standby mode when Switch S6 (the left hand side knob) is down. When the knob is up (default), the ADN8831 is released from standby mode. In standby mode, all circuits, with the exception of the VREF and SYNCO outputs of the ADN8831, are powered off.

Switch S6, Right Hand Side: Shutdown Control

The ADN8831 is in shutdown mode when Switch S6 (the right hand side knob) is down. When the knob is up (default), the ADN8831 is released from shutdown mode. In shutdown mode, the ADN8831 is powered off.

Switches S1, S2, S3, S4, and S5: Adjustable Components for an Optimal PID Compensation Network

Switches S1, S2, S3, S4, and S5 provide PID network component adjustability for CD, RD, RI, RP, and CI as shown in Figure 3. After connecting one TEC to an ADN8831-EVALZ, a thermal oscillation may occur. To squelch the oscillation, optimize the system settling time, and to control the TEC temperature precisely, PID network component tuning is necessary.

When a switch knob is in the up position, the value listed below the switch knob is an increment to the component. For example, Switch S1 determines the CD value in Figure 3 and Figure 9. Switch S1 shows the up knobs for the 4.7 µF and the 1 µF (note that these knobs are set to the upper position). In this example, the value of CD is

\[4.7 \, \mu F + 1 \, \mu F = 5.7 \, \mu F\]

The same principle applies to Switches S1, S2, S3, S4, and S5.

On-Board Potentiometers

The ADN8831-EVALZ has the following on-board potentiometers to adjust the component values (shown in Figure 3) and to configure the TEC current limitation at both cooling and heating modes.

The default settings are shown in Table 2.

<table>
<thead>
<tr>
<th>Potentiometer</th>
<th>Function</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>Temperature compensation network</td>
<td>17.5 kΩ</td>
</tr>
<tr>
<td>R2</td>
<td>Temperature compensation network</td>
<td>7.5 kΩ</td>
</tr>
<tr>
<td>R3</td>
<td>Temperature compensation network</td>
<td>81.3 kΩ</td>
</tr>
<tr>
<td>W1</td>
<td>TEMPSET</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>W2</td>
<td>VILIM</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>W3</td>
<td>VILIM, VILIM</td>
<td>20 kΩ</td>
</tr>
<tr>
<td>W4</td>
<td>VILIM, VILIM</td>
<td>20 kΩ</td>
</tr>
</tbody>
</table>
QUICK START
Connect the power supply, the TEC module, and the thermistor to an ADN8831-EVALZ as shown in Figure 5 and as described in Step 1 through Step 6.

![Quick Start Block Diagram](Image)

1. Verify that the on-board switches are set to the defaults.
2. Connect the thermistor between the board pads labeled RTH and AGND.
3. Connect the positive terminal of a thermoelectric cooler to the TECP board pad and connect the negative terminal to TECN.
4. Verify the on-board potentiometer default settings.
5. Ensure that the power supply is powered off and then connect it to board pads VDD and PGND. Maintain the power supply between 3.0 V and 5.5 V for proper operation.
6. Turn on the power supply.

The thermistor temperature-dependent voltage, TEMPOUT, locks to the programmed setpoint voltage, TEMPSET. The green LED illuminates within several seconds, indicating successful temperature lock.

CONFIGURE SETPOINT TEMPERATURE RANGE
The default values for Resistor R1, R2, and R3, listed in Table 2, are optimal for a 10 kΩ, \( \beta = 3450 \) (at 25°C) thermistor to lock a TEC temperature at 25°C. The sections that follow describe how to configure potentiometers for different negative temperature coefficient (NTC) thermistors.

Thermistor Values
Determine the three thermistor resistance values: \( R_{\text{HIGH}} \), \( R_{\text{MED}} \), and \( R_{\text{LOW}} \). To do this, refer to the thermistor R-T table in the appropriate thermistor data sheet. This is based on required TEC thermal control resolution and the target controllable temperature range.

These resistor values correspond to the high, middle, and low setpoint temperatures \( (T_{\text{HIGH}}, T_{\text{MED}}, \text{and } T_{\text{LOW}}) \). \( T_{\text{MED}} \) is the TEC system controllable setpoint temperature range.

\[
T_{\text{MED}} = \frac{T_{\text{HIGH}} + T_{\text{LOW}}}{2}
\]

\( T_{\text{MED}} \) is the average temperature, between \( T_{\text{HIGH}} \) and \( T_{\text{LOW}} \). \( V_{\text{TEMPOUT}} \) is the voltage output at the TEMPOUT pin. It is \( R_{\text{TH}} \) resistance dependent. \( V_{\text{TEMPOUT}} \) is a function of \( R_{\text{TH}}, R_{1}, R_{2}, \) and \( R_{3} \) as

\[
V_{\text{TEMPOUT}} = 0.5 \times V_{\text{REF}} \times R_{1} \times \left[ \frac{1}{R_{3}} - \frac{1}{R_{1}} + \frac{1}{R_{3} + R_{TH}} \right]
\]

In a design, let \( V_{\text{TEMPOUT}} \) equal the following values at the three thermistor resistances:

\[
\begin{align*}
R_{\text{TH}} &= R_{\text{HIGH}}(\text{at } T_{\text{HIGH}}): \quad V_{\text{TEMPOUT}} = V_{\text{REF}} \\
R_{\text{TH}} &= R_{\text{MED}}(\text{at } T_{\text{MED}}): \quad V_{\text{TEMPOUT}} = 0.5 \times V_{\text{REF}} \\
R_{\text{TH}} &= R_{\text{LOW}}(\text{at } T_{\text{LOW}}): \quad V_{\text{TEMPOUT}} = 0 \text{ V}
\end{align*}
\]

In this example, \( V_{\text{REF}} \) equals about 2.5 V and is a reference voltage at Pin 8 of the ADN8831.

Resistor Values
To achieve the required \( V_{\text{TEMPOUT}} \) outputs at the three different setting point temperatures, use the equation

\[
R_{1} = R_{\text{MED}} + \frac{R_{\text{MED}} (R_{\text{LOW}} + R_{\text{HIGH}}) - 2R_{\text{HIGH}} R_{\text{LOW}}}{R_{\text{HIGH}} + R_{\text{LOW}} - 2R_{\text{MED}}} \quad (1)
\]

\[
R_{2} = R_{1} - R_{\text{MED}} \quad (2)
\]

\[
R_{3} = \frac{R_{1} (R_{1} + R_{\text{LOW}} - R_{\text{MED}})}{R_{\text{LOW}} - R_{\text{MED}}} \quad (3)
\]

For example, setting the high setpoint temperature at 35°C and the low setpoint temperature at 15°C results in a middle setpoint temperature \( (35 + 15)/2 = 25°C \). Using the R-T table of a thermistor,

\[
\begin{align*}
R_{\text{HIGH}} &= 6.9 \text{ kΩ} \\
R_{\text{MED}} &= 10 \text{ kΩ} \\
R_{\text{LOW}} &= 14.8 \text{ kΩ}
\end{align*}
\]

Note that Equation 1 to Equation 3 result in

\[
\begin{align*}
R_{1} &= 17.5 \text{ kΩ} \\
R_{2} &= 7.5 \text{ kΩ} \\
R_{3} &= 81.3 \text{ kΩ}
\end{align*}
\]

Adjusting the Potentiometers \( R_{1}, R_{2}, \) and \( R_{3} \)
To adjust on-board potentiometers to get the proper \( R_{1}, R_{2}, \) and \( R_{3} \) values, turn off the power supply and then measure the resistance between

- TPR1 and TPR123, and adjust Potentiometer R1 to
  \( R_{1} = 17.5 \text{ kΩ} \).
- TPR2 and TPR123, and adjust Potentiometer R2 to
  \( R_{2} = 7.5 \text{ kΩ} \).
- Between TPR3 and TPR123, and adjust Potentiometer R3 to
  \( R_{3} = 81.3 \text{ kΩ} \).
Because these potentiometers connect to the active components inside the ADN8831, the measured result is not accurate if the internal components conduct a significant leakage current. These components have a turn on voltage of ~0.8 V.

After R1, R2, and R3 are configured, the output voltage of the first amplifier, \( V_{\text{TEMPOUT}} \), equals

\[
V_{\text{TEMPOUT}} = 0.5 \times V_{\text{REF}} \times R_1 \times \left[ \frac{1}{R_3} - \frac{1}{R_1} + \frac{1}{R_3} \right]
\]

where:
- \( R_{TH} \) is the thermistor resistance within the setpoint temperature range.
- \( V_{\text{REF}} \) is the voltage reference value of the ADN8831, nominally 2.5 V.

When the setpoint temperature range is narrow, such as <20°C, the relationship between the thermistor temperature and the temperature voltage, \( V_{\text{TEMPOUT}} \), is almost linear, and the error is less than 0.15%. The linear equations is

\[
V_{\text{TEMPOUT}} = V_{\text{REF}} \times \left[ \frac{T_{\text{SET}} - T_{\text{LOW}}}{T_{\text{HIGH}} - T_{\text{LOW}}} \right]
\]

where:
- \( T_{\text{HIGH}} \) is the upper temperature limit in °C.
- \( T_{\text{LOW}} \) is the lower temperature limit in °C.
- \( T_{\text{SET}} \) is the setpoint temperature value in °C.

In the case where the second part of Equation 1 is negative, that is

\[
\frac{R_{\text{MID}}(R_{\text{LOW}} + R_{\text{HIGH}})}{R_{\text{HIGH}} + R_{\text{LOW}} - 2R_{\text{MID}}} \leq 0
\]

Set \( R_1 = R_{\text{MID}} \) and \( R_2 = 0 \).

For some applications, the setpoint temperature is not a range, but a single point temperature. In this case, set the single point temperature to be the midpoint temperature, \( T_{\text{MID}} \), and set \( T_{\text{HIGH}} = T_{\text{MID}} + 5 \)°C, and \( T_{\text{LOW}} = T_{\text{MID}} - 5 \)°C. At the same time, set \( R_1 = R_{\text{MID}} \) and \( R_2 = 0 \). Because the setpoint temperature is a single point, there is no need to linearize the \( V_{\text{TEMPOUT}} \) vs. temperature response curve. After calculating R3, check to see if the gain of the first stage is between 10 and 30. The gain calculates as

\[
\text{GAIN} = 2 \times \frac{R_3}{R_{\text{MID}}}
\]

If the gain is too high, increase the span between \( T_{\text{HIGH}} \) and \( T_{\text{LOW}} \), otherwise, decrease the span.

Note that the lower limit on the TEMPOUT pin cannot be 0 V. The minimum output voltage is 50 mV. Configure the setpoint temperature range so that some margin exists in the lower limit. For example, for a temperature range of 35°C to 15°C, use 14.5°C (2% lower than the 15°C limit) as the lower limit.

### CONFIGURE THE SETPOINT TEMPERATURE

The \( V_{\text{TEMPSET}} \) voltage corresponds to a TEC setpoint temperature. Configure the \( V_{\text{TEMPSET}} \) using Potentiometer W1. There are two cases in which to use Equation 4. In the first case, the setpoint temperature is known. Use the R-T table in the thermistor data sheet to find the specific value of \( R_{TH} \), then solve for \( V_{\text{TEMPSET}} \). Apply \( V_{\text{TEMPSET}} \) to the TEMPSET pin.

In the second case, the voltage at Pin TEMPOUT is known. Solve the equation for \( R_{TH} \) and use the R-T table in the thermistor data sheet to find the setpoint temperature.

\[
V_{\text{TEMPSET}} = 0.5 \times V_{\text{REF}} \times R_1 \times \left[ \frac{1}{R_3} - \frac{1}{R_1} + \frac{1}{R_3} \right]
\]

where:
- \( R_{TH} \) is the thermistor resistance at the setpoint temperature.
- \( V_{\text{REF}} \) is the voltage reference value of the ADN8831, nominally 2.5 V.

An alternative method is to assume that there is a linear relationship between temperature and voltage; this is similar to the linear relationship described for the TEMPOUT pin. When the setpoint temperature range is narrow, such as <20°C, the relationship between the thermistor temperature and the temperature voltage, \( V_{\text{TEMPOUT}} \), is almost linear, and the error is less than 0.15%. It is possible to derive the setpoint temperature by the upper and lower temperatures and the voltage limit. The equation is

\[
V_{\text{TEMPSET}} = 0.5 \times V_{\text{REF}} \times R_1 \times \frac{T_{\text{SET}} - T_{\text{LOW}}}{T_{\text{HIGH}} - T_{\text{LOW}}}
\]

where:
- \( T_{\text{HIGH}} \) is the upper temperature limit in °C.
- \( T_{\text{LOW}} \) is the lower temperature limit in °C.
- \( T_{\text{SET}} \) is the setpoint temperature value in °C.

### SET THE OUTPUT CURRENT LIMITS

Use Potentiometers W3 and W4 to determine the TEC current limits at cooling and heating modes. Then, use Equation 5 and Equation 6 to determine the required voltage levels applied to the ILIMC and ILIMH pins.

\[
V_{\text{ILIMC}} = \frac{V_{\text{REF}}}{2} + 25 \times I_{\text{TMAX}} \times R_s
\]

\[
V_{\text{ILIMH}} = \frac{V_{\text{REF}}}{2} - 25 \times I_{\text{TMAX}} \times R_s
\]

where:
- \( V_{\text{ILIM}} \) is the voltage applied to Pin ILIMC.
- \( V_{\text{ILIMH}} \) is the voltage applied to Pin ILIMH.
- \( I_{\text{TMAX}} \) is the maximum TEC current for cooling.
- \( I_{\text{TMAX}} \) is the maximum TEC current for heating.
- \( R_s \) is the resistance value of a current sense resistor. In Figure 9, \( R_s = 0.02 \Omega \).
- \( V_{\text{REF}} \) is the reference voltage. When taken from the ADN8831, \( V_{\text{REF}} = 2.5 \text{ V} \).
For example, to set $I_{\text{TCMAX}}$ and $I_{\text{THMAX}}$ equal to 2 A and 1.5 A, respectively, use the following equations:

$$V_{\text{ILMC}} = \frac{2.5}{2} + 25 \times 2 \times 0.02 = 2.25 \text{ V}$$

$$V_{\text{ILMH}} = \frac{2.5}{2} - 25 \times 1.5 \times 0.02 = 0.5 \text{ V}$$

Turn Potentiometer W3 while measuring the voltage at Pin 1 (ILMC); set this value to be equal to 2.25 V. Turn W4 while measuring the voltage at Pin 32 (ILIMH); set this value to equal 0.5 V.

**SET THE OUTPUT VOLTAGE LIMIT**

To protect the TEC from being overdriven, adjust W2 to set up the $V_{\text{LIM}}$ voltage. The maximum voltage applied across the TEC can be limited by setting the voltage on Pin 31 ($V_{\text{LIM}}$). This voltage is

$$V_{\text{LIM}} = \frac{V_{\text{MAX}}}{5}$$

where:

$V_{\text{LIM}}$ is the voltage set at the VLIM pin.

$V_{\text{MAX}}$ is the maximum voltage across the TEC.

For example, to set a maximum TEC voltage equal to 4 V, use the following equation:

$$V_{\text{LIM}} = 4/5 = 0.8 \text{ V}$$

**MONITOR THE TEC VOLTAGE**

The voltage across the TEC, $V_{\text{TEC}}$, is monitored in real time by measuring the voltage $V_{\text{VTEC}}$ from Pin 30 (VTEC).

$$V_{\text{TEC}} = V_{\text{LFB}} - V_{\text{SFB}} = (V_{\text{VTEC}} - 0.5 \times V_{\text{REF}}) \times 4$$

where:

$V_{\text{TEC}}$ is the voltage across the TEC.

$V_{\text{LFB}}$ is the voltage measured at the LFB pin.

$V_{\text{SFB}}$ is the voltage measured at the SFB pin.

$V_{\text{VTEC}}$ is the voltage measured at the VTEC pin.

$V_{\text{REF}}$ is the reference voltage. When taken from the ADN8831, $V_{\text{REF}} = 2.5 \text{ V}$.

Alternatively, measuring the voltage difference between the LFB and SFB pins also results in the voltage across the TEC ($V_{\text{TEC}}$). Typically, the LFB pin connects to the positive terminal of the TEC, and the SFB pin connects to the negative terminal of the TEC. The definition of the TEC voltage is the voltage difference between the TEC positive and negative terminals.

$V_{\text{TEC}}$ can be positive or negative. When $V_{\text{TEC}}$ is positive, the TEC is in cooling mode. When $V_{\text{TEC}}$ is negative, the TEC is in heating mode.

When the ADN8831 is set to standby mode, knowing the voltage across the TEC is useful. This voltage, called the Seebeck voltage, is generated by the temperature difference between the two TEC plates. This measurement is useful for determining the condition of the TEC and/or the TEC working status for high end systems.

**MONITOR THE TEC CURRENT**

The TEC current is monitored in real time by measuring the voltage, $V_{\text{ITEC}}$, on the ITEC pin (Pin 29). To calculate the TEC current from the ITEC pin voltage, use the following equation:

$$I_{\text{TEC}} = \frac{V_{\text{ITEC}} - 0.5 \times V_{\text{REF}}}{25 \times R_s}$$

where:

$I_{\text{TEC}}$ is the TEC current; defined as the current flowing in through the TEC positive terminal (TECP) and out the TEC negative terminal (TECN).

$R_s$ is the current sense resistor value, set to 0.02 Ω on the evaluation board.

**TEMPERATURE COMPENSATION**

Temperature stability and settling time are control loop gain and bandwidth dependent. This includes the gain of the ADN8831 and the TEC/thermistor feedback. To achieve the highest dc precision, the control loop uses a proportional integral differential (PID) compensation network. Because thermal loads can vary widely from TEC to TEC, a tunable compensation network is available on the evaluation board. To tune the PID compensation network, apply a low frequency square wave to the LP2 solder pad and monitor the OUT2 test point using an oscilloscope.
2. When the compensation loop is stable, it is possible to adjust the component values in the network to decrease the overall loop response time. This is accomplished by slowly decreasing CI, increasing RP, decreasing RD, increasing CD, and decreasing RI. Adjust these such that the output at Pin OUT2 has a fast rise and fall time with little or no overshoot. In applications where fast response time is critical, allow for a small amount of overshoot (10% to 20%).

3. After tuning the compensation network to satisfactory values, it is recommended to replace the tunable compensation network components with the discrete components to be used in the future system and repeat the test. After soldering the discrete components, turn off the tunable compensation network components by placing all the switches into the lower position.

4. The capacitors used in the compensation network should be multilayer ceramic capacitors of X7R material. This type of capacitor maintains a stable capacitance over temperature and bias drifts. X7R type capacitors also have a very low leakage current and low noise.

Typical performance for a butterfly-packaged laser with a settling time of 1°C change in setpoint temperature is approximately 0.2 second to 1 second; for a large mass laser head of 1 W to 3 W, the settling time is about 5 seconds to 20 seconds. For more details of the temperature compensation network, see the ADN8831 data sheet.

**ADJUST THE PWM SWITCHING FREQUENCY**

The ADN8831 evaluation board is default set to a free-run PWM clock at 1 MHz. To modify $R_{FREQ}$, adjust the PWM switching frequency (see Figure 7). Reducing the frequency of the PWM switching frequency improves the system power efficiency, but requires the use of a large physical size LC filter inductor and capacitors.

For telecommunication applications, the recommended setting (default) is 1 MHz for the switching frequency. However, for applications where efficiency is critical, a 500 kHz clock is an option.

**Table 3. Switching Frequencies vs. $R_{FREQ}$**

<table>
<thead>
<tr>
<th>$f_{SWITCH}$</th>
<th>$R_{FREQ}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>250 kHz</td>
<td>484 kΩ</td>
</tr>
<tr>
<td>500 kHz</td>
<td>249 kΩ</td>
</tr>
<tr>
<td>750 kHz</td>
<td>168 kΩ</td>
</tr>
<tr>
<td>1 MHz</td>
<td>118 kΩ</td>
</tr>
</tbody>
</table>
EVALUATION BOARD LAYOUT

Figure 10 through Figure 13 show the layout of the ADN8831 evaluation board.

Seven important guidelines are helpful when designing an ADN8831 evaluation board layout. Refer to Figure 9 for the part numbers listed here.

1. The ground terminals of decoupling capacitors from the PVDD to PGND and the PWM LC output filter capacitors must be tied together to reduce the power rail ripple. Using PCB traces or a ground plane (with long current paths) to connect these two components may generate, rather than reduce, the power rail ripple (supply pumping).

2. The two source terminals of the PWM MOSFETs must be connected directly or through a thick trace (>1 mm) to the terminals of the power supply decoupling capacitors (C16 and C19).

3. ADN8831-EVALZ uses a 4-layer PCB layout. Several recommendations to consider when using a 4-layer PCB follow.
   - Use one internal layer as the ground plane, the other internal layer for signal traces. Use both top and bottom layers as heat sinks for the ADN8831 IC, the output filter inductor, and the output MOSFETs (both on the linear and on the PWM sides).
   - Avoid conducting high current on the ground plane.
   - Always differentially run the PCB traces for critical signal paths. For example, run a dedicated parallel trace for the analog ground (AGND) with the R2 Pin 1 trace; both are for connecting the two terminals of the thermistor. This ensures that any interference coupled on the thermistor traces can cancel each other.
   - The low frequency temperature control circuit can be degraded easily by high frequency interference due to the rectifier effect. This effect refers to the phenomenon that occurs when a high frequency signal interferes with a low frequency circuit; the interference signal is rectified, or coupled, onto dc or lower frequency signals, thus affecting the operation of the circuit. When high frequency interference is unavoidable, use a small capacitor of up to 100 nF connected across the thermistor and mounted close to the controller to decouple the high frequency interference.

4. Ensure that the power supply decoupling capacitors have a total value of >40 μF. SMT multilayer ceramic capacitors of type X5R or X7R are the recommended capacitors. These types of capacitors have stable capacitance over temperature and very low equivalent series resistance (ESR).

5. The resistor placed between AVDD and PVDD is 1 Ω to 10 Ω in value.

6. Design the AGND and PGND carefully and connect both grounds at where the lowest current density exists on the PCB.

7. Because the ADN8831 and the MOSFETs take huge amounts of current, heat can build up quickly. For stable component performance, a metal heat sink design can relieve the component heat dissipation problem, especially at the PWM MOSFET side. When designing your layout, it is good practice to leave adequate space between the components. To ensure that your heat sink design is adequate, contact Analog Devices for design review support of your layout before fabricating the PCB.
Figure 9 shows the schematic of the ADN8831 evaluation board (Version 4.0). Note that THPAD, shown as Pin 33 in this schematic, refers to the exposed thermal pad underneath the chip set. Connect THPAD to AGND to dissipate heat.
Figure 12. Middle Layer 2 Layout

Figure 13. Bottom Layer Layout
## BILL OF MATERIALS

Table 4.

<table>
<thead>
<tr>
<th>Qty</th>
<th>Designator</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>R14</td>
<td>Resistor 1 Ω 0603</td>
<td>Yageo</td>
<td>RC0603FR-071RL</td>
</tr>
<tr>
<td>1</td>
<td>L1</td>
<td>1.5 µH 3A, 0.2 mm × 6.2 mm × 2 mm</td>
<td>Toko</td>
<td>#A918CY-1R5M=P3</td>
</tr>
<tr>
<td>2</td>
<td>R11, R12</td>
<td>Resistor 1 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF1001V</td>
</tr>
<tr>
<td>2</td>
<td>R15, R5</td>
<td>Resistor 1 mΩ</td>
<td>Panasonic</td>
<td>ERJ-3EKF1004V</td>
</tr>
<tr>
<td>1</td>
<td>C5</td>
<td>Capacitor ceramic 1 nF 0603 X7R 50 V</td>
<td>Kemet</td>
<td>C0603C102J5RACTU</td>
</tr>
<tr>
<td>3</td>
<td>C8, CD2, CI5</td>
<td>Capacitor ceramic 1 µF 0603 X5R 6.3 V</td>
<td>Murata</td>
<td>GRM188R61C105KA93D</td>
</tr>
<tr>
<td>1</td>
<td>CD3</td>
<td>Capacitor ceramic 2.2 µF 0603 X5R 6.3 V</td>
<td>Murata</td>
<td>GRM188R60J225KE19D</td>
</tr>
<tr>
<td>1</td>
<td>C10</td>
<td>Capacitor ceramic 4.7 nF 0603 X7R 50 V</td>
<td>Yageo</td>
<td>CC0603KRX7R9BB472</td>
</tr>
<tr>
<td>1</td>
<td>CD4</td>
<td>Capacitor ceramic 4.7 µF 0603 X5R 6.3 V</td>
<td>T-Y</td>
<td>JMK107B475KA-T</td>
</tr>
<tr>
<td>1</td>
<td>R13</td>
<td>Resistor 4.75 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF4751V</td>
</tr>
<tr>
<td>1</td>
<td>R1B</td>
<td>Resistor 10 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF1002V</td>
</tr>
<tr>
<td>1</td>
<td>CF</td>
<td>Capacitor ceramic 10 nF 0805 X7R 50 V</td>
<td>Murata</td>
<td>GRM216R71H103K</td>
</tr>
<tr>
<td>7</td>
<td>C14, C15, C16, C17, C18, C19, CD5</td>
<td>Capacitor ceramic 10 µF 0603 X5R 6.3 V</td>
<td>Murata</td>
<td>GRM188R60J106ME47D</td>
</tr>
<tr>
<td>1</td>
<td>CD1</td>
<td>Capacitor ceramic 10 nF 0603 X5R 50 V</td>
<td>Murata</td>
<td>GRM188R60J106ME47D</td>
</tr>
<tr>
<td>1</td>
<td>CI1</td>
<td>Capacitor ceramic 47 nF 0603 X7R 16 V</td>
<td>Panasonic</td>
<td>ECJ-1VB1C473K</td>
</tr>
<tr>
<td>1</td>
<td>RD1</td>
<td>Resistor 12.4 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF1242V</td>
</tr>
<tr>
<td>1</td>
<td>R4, R5, R6</td>
<td>Resistor 20 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3GEYJ203V</td>
</tr>
<tr>
<td>6</td>
<td>TPR1, TPR2, W1, W2, W3, W4</td>
<td>Trimmer potentiometers multiturns 20 kΩ</td>
<td>Murata</td>
<td>PVG5A203C01R00</td>
</tr>
<tr>
<td>1</td>
<td>R5</td>
<td>Resistor 20 mΩ 0805</td>
<td>Vishay</td>
<td>WSL0805R0200FEA18</td>
</tr>
<tr>
<td>1</td>
<td>RD2</td>
<td>Resistor 24.9 kΩ 0603</td>
<td>SUSUMU</td>
<td>RR0816P-2492-D-39C</td>
</tr>
<tr>
<td>1</td>
<td>C11</td>
<td>Capacitor ceramic 47 nF 0603 X7R 50 V</td>
<td>Panasonic</td>
<td>ECJ-1VB1C473K</td>
</tr>
<tr>
<td>1</td>
<td>RD3</td>
<td>Resistor 49.9 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF4992V</td>
</tr>
<tr>
<td>2</td>
<td>R11, R1P</td>
<td>Resistor 61.9 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF6912V</td>
</tr>
<tr>
<td>2</td>
<td>R10, RD4</td>
<td>Resistor 100 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF1003V</td>
</tr>
<tr>
<td>6</td>
<td>C1, C2, C3, C4, CI2, C13</td>
<td>Capacitor ceramic 100 nF 0603 X7R 10 V</td>
<td>Kemet</td>
<td>C0603C104K8RACTU</td>
</tr>
<tr>
<td>1</td>
<td>C9</td>
<td>Capacitor ceramic 100 µF 0603</td>
<td>Yageo</td>
<td>CC0603JRNP09BN101</td>
</tr>
<tr>
<td>3</td>
<td>R9, R12, RP2</td>
<td>Resistor 124 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF1243V</td>
</tr>
<tr>
<td>1</td>
<td>R8</td>
<td>Resistor 200 Ω 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF200V</td>
</tr>
<tr>
<td>1</td>
<td>RD5</td>
<td>Resistor 200 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF2003V</td>
</tr>
<tr>
<td>1</td>
<td>TPR3</td>
<td>Trimmer potentiometers multiturns 200 kΩ</td>
<td>Murata</td>
<td>PVG5A204C01R00</td>
</tr>
<tr>
<td>1</td>
<td>CI3</td>
<td>Capacitor ceramic 220 nF 0603 X5R 10 V</td>
<td>Murata</td>
<td>GRM188R71A224KA01D</td>
</tr>
<tr>
<td>2</td>
<td>R13, RP3</td>
<td>Resistor 249 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF4993V</td>
</tr>
<tr>
<td>2</td>
<td>CD1, CI4</td>
<td>Capacitor ceramic 470 nF 0603 X5R 6.3 V</td>
<td>Murata</td>
<td>RM188R71E474KA12D</td>
</tr>
<tr>
<td>3</td>
<td>R7, R4, RP4</td>
<td>Resistor 499 kΩ 0603</td>
<td>Panasonic</td>
<td>ERJ-3EKF4993V</td>
</tr>
<tr>
<td>1</td>
<td>U1</td>
<td>TEC controller</td>
<td>Analog Devices</td>
<td>ADN8831ACPZ</td>
</tr>
<tr>
<td>2</td>
<td>Q1, Q2</td>
<td>Dual N- and P-channel MOSFET</td>
<td>Fairchild</td>
<td>FDS8960C</td>
</tr>
<tr>
<td>1</td>
<td>D1</td>
<td>LED SMT green</td>
<td>OSRAM</td>
<td>LG T67K-H2K1-24-Z</td>
</tr>
<tr>
<td>1</td>
<td>S6</td>
<td>Switch, 2PST</td>
<td>C&amp;K</td>
<td>SDA02H15BD</td>
</tr>
<tr>
<td>5</td>
<td>S1, S2, S3, S4, S5</td>
<td>Switch, 5PST</td>
<td>C&amp;K</td>
<td>SDA05H15BDA</td>
</tr>
</tbody>
</table>