ANALOG DEVICES

AN-617
Application Note

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Wafer Level Chip Scale Package

by the Wafer Level Package Development Team

GENERAL DESCRIPTION

The wafer level chip scale package (WLCSP) is a variant of the flip-chip interconnection technique where all packaging is done at the wafer level. With WLCSPs, the active side of the die is inverted and connected to the printed circuit board (PCB) using solder balls. The size of these solder balls is typically large enough (250 µm to 300 µm pre-reflow) when compared to the flip-chip interconnects that underfill is not required. This interconnection technology offers several advantages.

Some advantages include the following:

- Considerable space savings resulting from the elimination of the first level package (mold compound, lead frame, or organic substrate). For example, an 8-bump WLCSP occupies only 8% of the board area taken up by an 8-lead SOIC.
- Improved electrical performance, such as reduced inductance, due to the elimination of wire bonds and leads used in standard plastic packaging.
- Lighter weight and thinner package profile, due to the elimination of lead frame and molding compound.
- High assembly yields resulting from the self-aligning characteristic of the low mass die during solder attachment.

PURPOSE

This application note provides the end-user with information on

- WLCSP construction and configurations
- Typical WLCSP dimensions
- PCB design
- Surface-mount guidelines
- WLCSP reliability
- Thermal performance
- Rework
- Shipping media

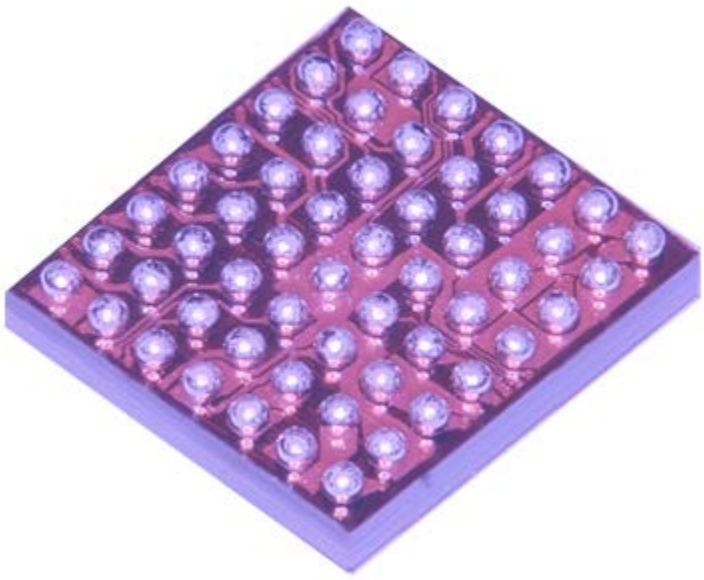

Figure 1. Photograph of a 7 × 8 Array—Wafer Level Chip Scale Package (WLCSP)

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CONSTRUCTION AND CONFIGURATION

WLCSP CONSTRUCTION

WLCSPs can be categorized into two construction types: direct bump and redistribution layer (RDL).

A direct-bump WLCSP consists of an organic repassivation layer that acts as a stress buffer on the active die surface. The polyimide covers the entire die area except for openings around the bond pads. An under-bump metallurgy (UBM) layer is deposited over this opening. The UBM is a stack of different metal layers serving as diffusion layer, barrier layer, wetting layer, and anti-oxidation layer. The solder ball is dropped (which is why it's called ball-drop) over the UBM and reflowed to form a solder bump (see Figure 2).

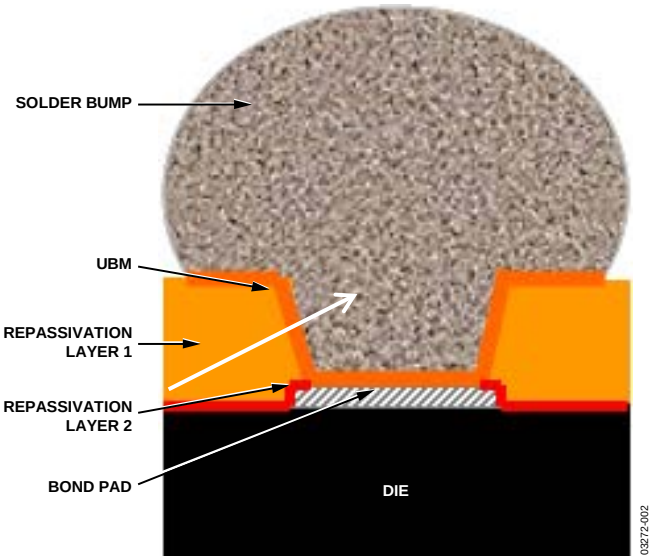

Figure 2. Typical Construction of a Direct Bump WLCSP

RDL technology allows a die designed for wire bonding (with bond pads arranged along the periphery) to be converted into a WLCSP. In contrast to a direct bump, this type of WLCSP uses two polyimide layers. The first polyimide layer is deposited over the die, keeping the bond pads open. An RDL layer is deposited to convert the peripheral array to an area array. The construction then follows the direct bump, with a second polyimide layer, UBM, and ball drop (see Figure 3).

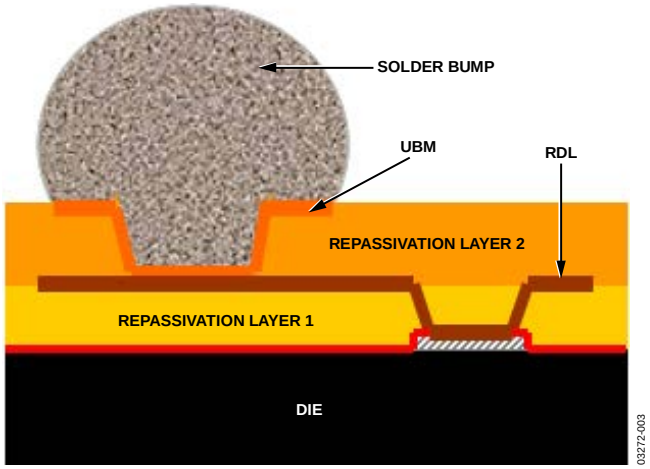

Figure 3. Typical Construction of a WLCSP Redistributed Die

Post ball-drop, the wafers are back-grinded, laser-marked singulated, and put onto the tape and reel. There is also an option of applying a backside laminate after the back-grinding process to reduce die chip-outs induced during sawing and to ease the handling of the package.

WLCSP CONFIGURATION

All WLCSP parts from Analog Devices, Inc., have a standard pitch of 0.5 mm or 0.4 mm. For this reason, each array offered has a minimum die size (package size) to accommodate the standard bumps and pitches. Table 1 provides details of standard WLCSP arrays, which have an array pitch of 0.5 mm or 0.4 mm.

Table 1. Minimum Die Size for WLCSP Arrays at 0.5 mm and 0.4 mm Pitch

Array	Maximum I/O	Minimum Die Size	
		Pitch = 0.5 mm	Pitch = 0.4 mm
2 × 2	4	1.0 mm × 1.0 mm	0.8 mm × 0.8 mm
2 × 3	6	1.0 mm × 1.5 mm	0.8 mm × 1.2 mm
3 × 3	9	1.5 mm × 1.5 mm	1.2 mm × 1.2 mm
3 × 4	12	1.5 mm × 2.0 mm	1.2 mm × 1.6 mm
4 × 4	16	2.0 mm × 2.0 mm	1.6 mm × 1.6 mm
4 × 5	20	2.0 mm × 2.5 mm	1.6 mm × 2.0 mm
5 × 5	25	2.5 mm × 2.5 mm	2.0 mm × 2.0 mm
5 × 6	30	2.5 mm × 3.0 mm	2.0 mm × 2.4 mm
6 × 6	36	3.0 mm × 3.0 mm	2.4 mm × 2.4 mm
6 × 7	42	3.0 mm × 3.5 mm	2.4 mm × 2.8 mm
7 × 7	49	3.5 mm × 3.5 mm	2.8 mm × 2.8 mm
7 × 8	56	3.5 mm × 4.0 mm	2.8 mm × 3.2 mm
8 × 8	64	4.0 mm × 4.0 mm	3.2 mm × 3.2 mm
8 × 9	72	4.0 mm × 4.5 mm	3.2 mm × 3.6 mm
9 × 9	81	4.5 mm × 4.5 mm	3.6 mm × 3.6 mm
9 × 10	90	4.5 mm × 5.0 mm	3.6 mm × 4.0 mm
10 × 10	100	5.0 mm × 5.0 mm	4.0 mm × 4.0 mm

WLCSP DIMENSIONS

The typical ball diameter, ball height, and silicon thickness dimensions with their tolerances are shown in Table 2.

Table 2. Package Dimension for WLCSP Arrays at 0.5 mm and 0.4 mm Pitch

Dimension	Tolerance	0.5 mm Pitch	0.4 mm Pitch	
Bump Diameter	±40 µm	320 µm	260 µm	
Bump Height	±30 µm	240 µm	200 µm	
Silicon Thickness	±30 µm	360 µm	400 µm	300 µm
Total Package Height	±60 µm	600 µm	600 µm	500 µm

PCB DESIGN

STANDOFF

The actual separation between the surface of the die and the substrate (standoff) after assembly varies with the amount of solder screen printed on to the substrate and pad diameter. Typical dimensions are shown in Table 3. The 300 µm ball was mounted on a 250 µm diameter NSMD pad, the 250 µm ball was mounted on a 200 µm diameter NSMD pad, and the 150 µm ball was mounted on a 110 µm diameter NSMD pad

Table 3. Typical WLCSP Dimensions After Assembly

Solder Ball Size (µm)	Total Package Height Before Board Mount (mm)	Standoff Height (mm)
300	0.600 ± 0.06	0.190 ± 0.03
250	0.500 ± 0.06	0.140 ± 0.03
150	0.315 ± 0.015	0.120 ± 0.03

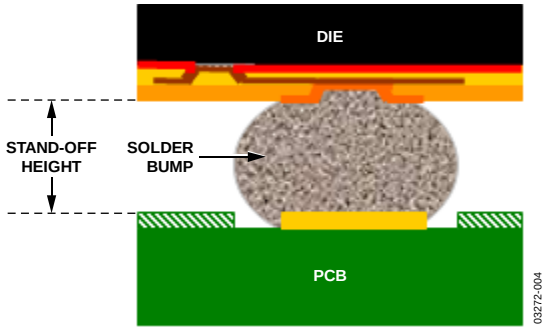

Figure 4. Typical WLCSP Dimensions After Assembly

SOLDER MASK DESIGN

For PCB fabrication, the following two types of PCB pads/land patterns are used for surface mount assembly:

- Nonsolder mask defined (NSMD). The metal pad on the PCB (to which a package I/O is attached) is smaller than the solder mask opening.
- Solder mask defined (SMD). The solder mask opening is smaller than the metal pad.

The difference between these two types of land patterns is shown in Figure 5.

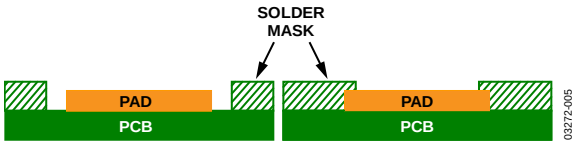

Figure 5. Cross-Sections of NSMD and SMD Pads/Land Patterns

Because the copper pad etching process has tighter control than the solder mask opening process, NSMD is preferred over SMD. The solder mask opening on NSMD pads is larger than the copper pads, allowing the solder to attach to the sides of the copper pad (as seen in Figure 4) improving the reliability of the solder joints.

For an NSMD pad, the trace width connecting to the pad diameter should be no more than 60% of the pad diameter. If the PCB design uses via-in-pad, the via should be filled and plated flat to prevent voiding of the solder joint.

When designing the board, the solder mask registration capability of the board manufacturer should be checked to ensure that the correct solder mask opening dimension is 50 µm on each side of the copper pad. The actual size of the copper pad to be used should be 80% of the diameter of the WLCSP solder bump. A copper thickness of less than 1/2 oz. is required to achieve the required definition. Trace width < 2/3 × Pad Size is recommended. Mask opening should be Pad Diameter + 100 µm. The recommended pad dimensions are shown in Table 4.

Table 4. Recommended Pad Dimensions

Bump Diameter (mm)	Pad Diameter (mm)	Mask Diameter (mm)
0.320 ± 0.04	0.250 ± 0.015	0.350 ± 0.015
0.260 ± 0.04	0.200 ± 0.015	0.300 ± 0.015
0.160 ± 0.04	0.110 ± 0.015	0.210 ± 0.015

BOARD MATERIAL

Standard epoxy glass substrates are compatible with the WLCSP. Assembly can be performed on standard epoxy glass substrate; however, changing from standard FR-4 to high temperature FR-4, which has a smaller coefficient of thermal expansion (CTE), improves package reliability. The CTE of a PC board can also be affected by factors such as number of metal layers, laminate material, trace density, and so on. Ideally, the glass transition temperature of the substrate should be above the application temperature of the assembled part.

The finish layer on the metal pads has a significant effect on assembly yield and reliability.

- Organic surface preservative (OSP) is recommended as the most appropriate finish. Suggested shelf-life is six months.
- Immersion silver or tin is an acceptable alternative to OSP.
- Electroless nickel immersion gold (ENIG) is acceptable, provided the thickness of gold is limited to 0.02 µm to 0.05 µm to prevent embrittlement.
- Thinner boards are more flexible and, consequently, show better reliability during thermal cycling. Standard board thicknesses used in the industry ranges from 0.4 mm to 2.3 mm. The thickness selected depends on the required robustness of the populated system assembly.

MISCELLANEOUS RECOMMENDATIONS

- Pad and solder mask registration tolerance = ± 25 µm.
- Solder Mask should be laser direct imageable (LDI)
- Use local fiducials
- Keep the silk screen away from the device footprint

BOARD DESIGN

With the increase in device functionality and decrease in the size of the device, the board fabrication becomes more difficult. As we move to large array sizes with finer pitches (400 µm) routing only on the top surface layer of the board is usually not feasible, due to the limitations of the geometries imposed by the board fabrication technology. The trace (width and space) must fit between the limits of the solder mask openings. Typical clearance for a trace with 75 µm width is 25 µm on each side. Thus, the total clearance is 25 µm + 75 µm + 25 µm = 125 µm. To route a 75 µm trace through two adjacent pads, the clearance between adjacent mask openings should be at least 125 µm. Typical PCB track and space rules are shown in Figure 6 and Table 5.

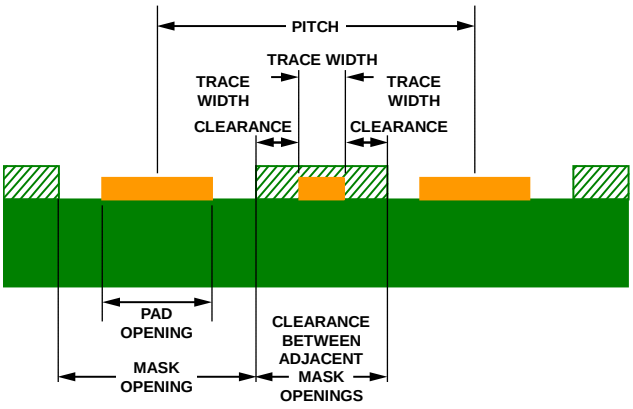

Figure 6. Typical PCB Track and Space Rules

Given a pitch of 500 µm with a typical solder mask opening diameter of 350 µm, there is 150 µm clearance between the solder mask openings. This exceeds the required trace clearance of 125 µm. Thus, the traces can be routed on the top layer. Similarly, for a pitch of 400 µm with a typical solder mask opening diameter of 300 µm, there is only 100µm distance between the solder mask openings. This clearance distance is less than 125 µm, thus trace cannot be routed on the top layer. The suggested alternative to this is to route using Microvia.

Table 5. Pad Dimensions for Trace Width = 75 µm

Pitch (µm)	Mask Size (µm)	Clearance Between Adjacent Mask Openings (µm)	Comments
500	350	500 – (350/2 + 350/2) = 150	No issues routing (150 µm > 125 µm)
400	300	400 – (300/2 + 300/2) = 100	Issues routing (100 µm < 125 µm)

By placing the vias in the pad, the clearance is increased. However, a standard via opening of 300 µm causes the solder to wick down into the via, resulting in weak or open solder joints. In addition, the capture pad is larger than the solder pad. The use of laser-drilled microvias allows a hole of 100 µm to be drilled in the board that, after plating, is further reduced to 50 µm. To maximize assembly yield, filled vias must be planar and void free. An example of this is shown in Figure 7.

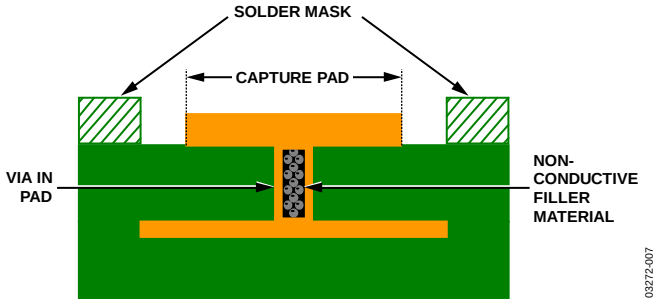

Figure 7. Plated Laser-Drilled Microvia Before Filling

ASSEMBLY CONSIDERATIONS

Board assembly requires solder paste to be screen printed on the board prior to reflow. The suggested process flow is

1. Boards should be baked out for 24 hours at 125°C prior to assembly
2. Incoming WLCSP tape and reel inspection
3. Solder paste print and inspection
4. Chip placement on PCB
5. Solder reflow and inspection
6. Optional flux clean
7. Inspection

SOLDER PRINTING PROCESS

Particular attention should be paid to the solder paste printing. All in-process inspections, such as height and registration, need to be carefully monitored. In addition

- Stencil type: laser-cut or electroformed
- Suggested stencil thickness
  - 0.5mm pitch devices with 300 µm solder ball size = 100 µm (4 mils)
  - 0.5mm pitch devices with 150 µm solder ball size = 100 µm (4 mils)
  - 0.4mm pitch devices with 250 µm solder ball size = 75 µm (3 mils)
- Squeegees
  - Type: metal
  - Angle = 60°
  - Suggested solder paste: Alpha OM338T or Senju S70G — alloy composition—SAC305—Type4 paste.

COMPONENT PLACEMENT PROCESS

- Automated placement with vision alignment should be used to place the parts.
- Placement force should be kept to a minimum, typically 150 grams.
- Local fiducials are recommended for higher placement accuracy.
- X-ray inspection for alignment, bridging, and so on prior to reflow.

REFLOW PROCESS

- Reflow profile and peak temperature can have a strong influence on void formation. Lower peak temperatures may require longer time above liquidus (TAL).
- The peak reflow temperature should not exceed the maximum temperature for which the package is qualified, according to the moisture sensitivity level (MSL1).
- The furnace should have a nitrogen purge, and the oxygen content should be kept below 100 ppm.

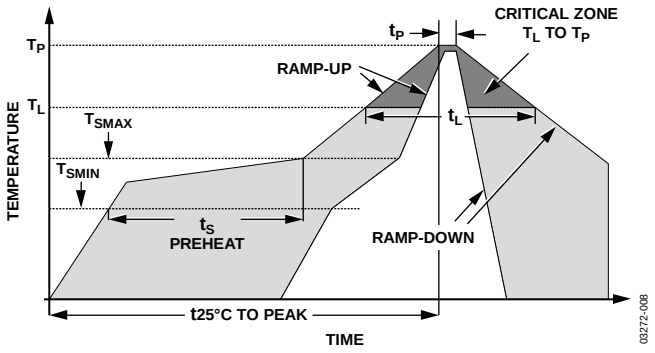

Figure 8. Recommended Soldering Profile Limits

Table 6. Recommended Soldering Profile Limits

Profile Feature	Pb Free
Average Ramp Rate (T_L to T_P)	1.25°C/sec max
Preheat	
Minimum Temperature (T_{SMIN})	100°C
Maximum Temperature (T_{SMAX})	200°C
Time (T_{SMIN} to T_{SMAX}), t_S	60 sec to 75 sec
Ramp-Up Rate (T_{SMAX} to T_L)	1.25°C/sec
Time Maintained Above Liquidous (t_L)	~50 sec
Liquidous Temperature (T_L)	217°C
Peak Temperature (T_P)	260°C +0°C/−5°C
Time Within 5°C of Actual Peak Temperature (t_P)	20 sec to 30 sec
Ramp-Down Rate	3°C/sec max
Time 25°C (t25°C) to Peak Temperature	5 min max

Actual reflow temperature settings need to be determined by the end-user, based on density and thermal loading effects. Refer to the solder paste manufacturer's data sheet for additional information.

Caution: WLCSP (especially with larger balls/higher standoffs) typically do not need underfill. If required, the material selected should be selected carefully and validated to ensure compatibility with the board assembly process and materials

WLCSP RELIABILITY

The usual package-related effects due to the encapsulant surrounding the die rarely impact an encapsulant-free WLCSP package. For example, high temperature electrical failure is often due to movement of ionic impurities derived from the molding compound. Also, moisture can become trapped within the encapsulant, and popcorning or corrosion may occur. Neither of these failure modes is observed with WLCSP packaging technology. Nevertheless, because the die is mounted on a printed circuit board, second-level packaging concerns, such as solder fracture during thermal cycling, need to be considered.

Electromigration within the solder ball occurs at the point of highest current density, namely at the passivation opening. At sufficiently high current density, phase separation occurs and voids can form between the solder bump and the UBM.

As with electromigration in thin films, such as aluminum, there is a strong dependence on temperature. Data sheet maximum current limits should be observed.

Analog Devices follows a comprehensive new product/new process qualification procedure that is failure mechanism driven. Tests performed accelerate failure mechanisms that may occur under normal life conditions. Failure mechanisms associated with the WLCSP technology and appropriate stress tests are detailed in Table 7.

Table 7. WLCSP Failure Mechanisms

Failure Mechanism	Description	Stress Test
Corrosion	Corrosion of bump or UBM may result in several types of failures. Chemical reactions may result in an open circuit, or dentritic formation may result in shorts or current leakage.	Autoclave/Highly Accelerated Stress Test (HAST)
Diffusion	May cause solder bump failure due to the excessive formation of intermetallics that can cause solder joint enbrittlement.	High Temperature Storage (HTS)
Thermomigration/ Electromigration	Describes the migration of bump solder over time. Excessive Sn/Cu or Sn/Ni can result in an open bump at the UBM/solder interface.	High Temperature Operating Life (HTOL)
Underbump Fracture	The fracture of the silicon or passivation under a bump during thermal cycling, resulting in a loss of functionality. The primary factors for controlling fracture are design/layout, brittle passivation, and the manufacturing environment.	Bump/Die shear
Solder Fatigue Due to Thermo-Mechanical Loading	Results from the mismatch between coefficient of thermal expansion of the bumped chip and the substrate. This produces high stress at the solder joint, and the bump fails at a low cycle fatigue.	Board level temperature cycling
Solder Fatigue Due to Mechanical Loading	Evaluates and compares drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure.	Board Level Drop Test
	The repeated flexing (cyclic bending) of board during various assembly and test operations and in actual use can cause electrical failures due to circuit board and trace cracks, solder interconnects cracks, and the component cracks	Board Level Bend Test.

THERMAL PERFORMANCE

Thermal performance is determined by heat transfer through the solder balls to the PCB board. This means that WLCSP thermal comparisons need to include the number of balls, board construction, and density of copper traces. Thermal balls that are connected to the ground plane also need to be considered.

The comparison simulations can be simplified by assuming the die is mounted on standard boards (JESD51-9 1s0p and JESD51-9 2s2p), the die is fully populated, and die size increases in approximately 500 µm increments. Table 8 lists the series of arrays, die sizes, and thermal ball counts that were modeled with a three-dimensional finite element analysis based on the commercial code from ANSYS.

Table 8. Package Constructions Considered for FEA

Array	Max I/O	Thermal Ball	Min Die Size (mm)
2 × 2	4	0	0.96 × 0.96
2 × 1 × 2	5	0	1.3 × 0.9
2 × 3	6	1	0.95 × 1.45
3 × 3	9	1	1.3 × 1.3
3 × 4	10	1	1.5 × 2.0
4 × 4	16	2	2.0 × 2.0
4 × 5	20	2	2.0 × 2.5
5 × 5	25	2	2.5 × 2.5
6 × 6	36	4	3.0 × 3.0
8 × 8	64	7	4.0 × 4.0

Each of the 10 arrays is modeled at 0.25 W power dissipation and 1.25 W power dissipation, with an ambient temperature of 85°C on both 1s0p and 2s2p substrates at three different air flow conditions. Typical results are shown in Table 9, and graphs of the overall trends are shown in Figure 9. The most common thermal metric is the junction-to-air thermal resistance (θ_{JA}), which is the difference in temperature between the junction and ambient, divided by the total power dissipated by the device.

The value of θ_{JA} is dependent on board construction. More copper layers enable heat to be removed more effectively. This relationship is demonstrated by comparing the low effective thermal conductivity test board (JESD51-9 1s0p) with the high effective version (JESD51-9 2s2p) (see Figure 9).

As shown in Figure 9, in the absence of a heat sink attached to the backside (not recommended), the most effective heat transfer occurs through the board.

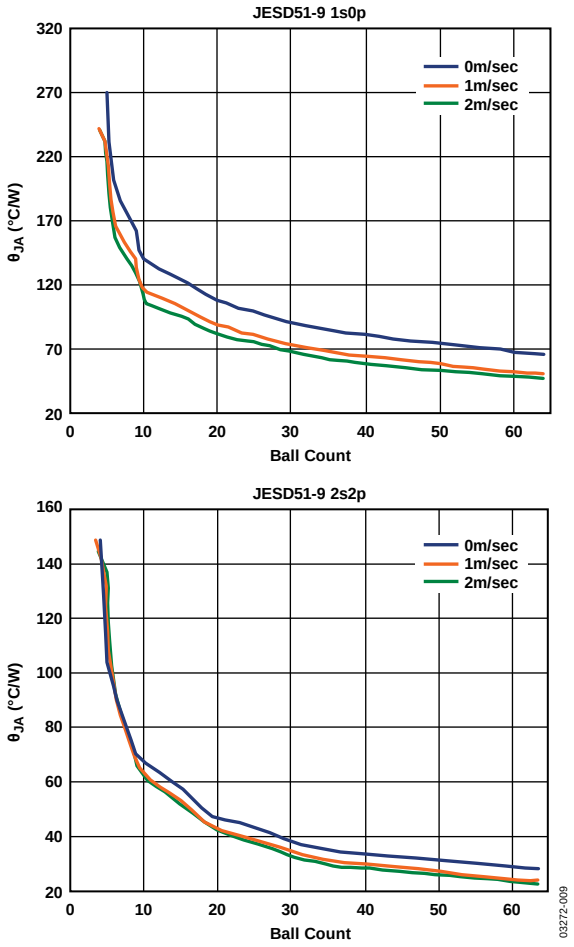

Figure 9. Comparison of θ_{JA} with 1-Layer and 4-Layer Boards (0.25 W)

Table 9. Typical Results From Modeling Package Constructions Shown in Table 8

Package Type	PCB	Power	θ_{JA} (°C/W)			θ_{JC} (°C/W)	θ_{JB} (°C/W)
			0 m/sec	1 m/sec	2 m/sec		
5L WLCSP	1S0P	0.25 W	266.6	231.5	217.2	2.5	57.6
		1.25 W	249.5	224.3	212.1	2.7	56.3
	2S2P	0.25 W	148.7	139.7	136.5	2.5	54.6
		1.25 W	146.9	139.4	136.4	2.6	55.2
20L WLCSP	1S0P	0.25 W	108.5	89.0	82.3	0.6	17.1
		1.25 W	101.1	87.3	81.2	0.6	17.5
	2S2P	0.25 W	47.9	43.4	42.1	0.7	9.1
		1.25 W	46.8	43.3	42.1	0.7	9.2
64L WLCSP	1S0P	0.25 W	65.5	50.4	45.8	0.1	7.1
		1.25 W	60.6	49.7	45.4	0.2	7.3
	2S2P	0.25 W	28.0	23.8	22.8	0.2	4.5
		1.25 W	26.9	23.7	22.7	0.2	4.5

REWORK

WLCSP rework is similar to that of a ball grid array (BGA) package. The rework steps are as follows:

1. Bake the board to prevent moisture damage during the rework process. The components/device for rework should also be heated to approximately 125°C to 130°C.
2. Duplicate original reflow profile used for SMT assembly on the rework station.
3. When the temperature reaches the Pb-free melting temperature of ~217°C, remove the device that needs to be reworked. The device can be removed either by the vacuum wand available on the rework station.
4. After the device is removed, redress the pads so that there is a uniform distribution of the leftover solder.
5. Reflux (using a no-clean flux) the redressed site and place the new device.
6. Using a nozzle-directed hot air flow available, simulate the original reflow profile on the rework station, reflow the new device.

SHIPPING MEDIA

Today's placement machines can pick and place thousands of components per hour with a very high degree of accuracy. To achieve this performance, the component delivery system must be capable of feeding parts at high speeds in a consistent orientation, positively indexed to the demands of the machine. The preferred packing material available today for these demands is tape and reel. Analog Devices' tape and reel system is fully compatible with the detaping equipment that is standard in most automated placement equipment.

SPECIFICATIONS

Analog Devices' tape and reel specifications are in conformance with the EIA Standard 481, "Taping of Surface-Mount Components for Automatic Placement."

ESD PROTECTION

The Analog Devices and reel delivery system is designed to offer a very high degree of protection against electrostatic discharge (ESD).

All tape and reel materials are static-dissipative. In addition, dry packed reels are shipped in moisture barrier bags; nondry packed reels are shipped in a box with ESD conductive coating or in a conductive ESD bag. To retain the benefits of this protection, the bags should be opened only at ESD-controlled work stations.

PEEL BACK STRENGTH

The peel back force is between 10 g and 100 g for 8 mm wide tape and 10 g to 130 g for tapes 12 mm and wider when tested at room temperature and pulled at a 175° to 180° angle with a peel-off speed of 300 ± 10 mm/min.

DIRECTION OF FEED

Direction of feed is defined as the direction in which the end user unreels the tape. The direction of feed for all products is counterclockwise when the reel is held with the round sprocket holes facing the observer (see Figure 10).

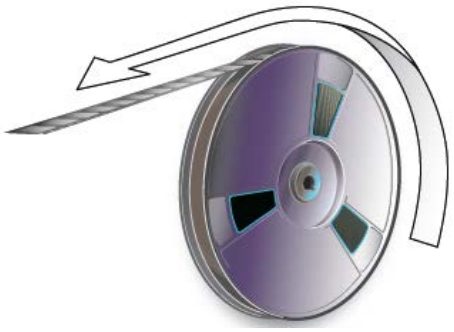

Figure 10. Direction of Feed

PIN 1 ORIENTATION

Devices are reeled so that Pin 1 is oriented properly with the direction of feed and round sprocket holes. Pin 1 orientation is denoted as C1 to C4 with respect to the direction of feed and round sprocket holes, as illustrated in Figure 11.

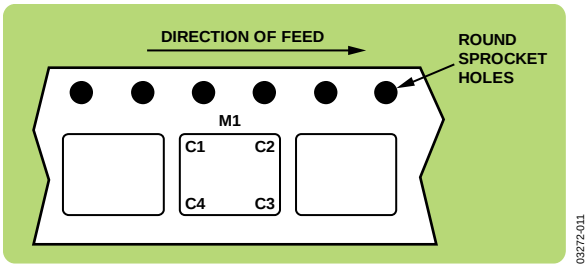

Figure 11. Pin 1 Orientation

NOTES

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