

Chopping on Σ - Δ ADCs

By Adrian Sherry

INTRODUCTION

Chopping is a technique that can be used to cancel offset voltages and other low frequency errors. This Application Note outlines how chopping is implemented on the AD7708/AD7718, AD7709, AD7719, AD7782/AD7783 high resolution Σ - Δ ADCs and discusses the resulting benefits it brings.

OFFSET ERRORS

Offset voltage errors can arise at many points within a signal processing chain, e.g., the temperature dependent thermocouple voltage that arises when two dissimilar metals are joined. Within an integrated circuit such as an ADC, there are numerous sources of internal offset errors, such as mismatch between the input devices of an amplifier, charge injection onto the sampling capacitor when a sampling switch is closed, or interference from EMI radiation. These offsets are generally undesirable and are particularly problematic if they change with temperature because a one-time calibration is not sufficient to remove offset errors across all temperatures and supplies.

CHOPPING

An offset that arises within the various amplifiers of a Σ - Δ modulator can generally be nulled out, either by local chopping or auto-zeroing the amplifier. However, other offset errors cannot be removed by these means. The solution implemented on these ADCs is to chop the entire analog signal chain within the ADC. This removes any offset and low frequency errors, giving extremely low offset errors and drift. The scheme is illustrated in Figure 1.

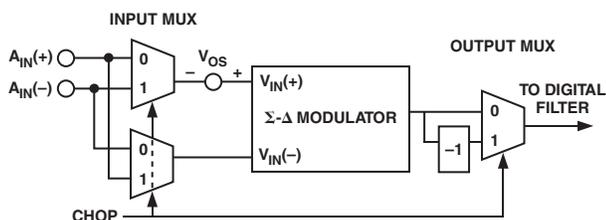


Figure 1. Chopping

The differential input to the modulator is alternately inverted (or chopped) at the input mux and an ADC conversion is performed for each phase of Chop. The modulator chopping is reversed in the output mux before passing to the digital filter.

If we model the offset in the Σ - Δ modulator as a term V_{OS} added to the input signal, then the output when Chop = 0 is:

$$(A_{IN(+)} - A_{IN(-)}) + V_{OS}$$

and the output when Chop = 1 is:

$$-[(A_{IN(-)} - A_{IN(+)} + V_{OS})]$$

The error voltage, V_{OS} , is removed by averaging these two results in the digital filter, leaving:

$$(A_{IN(+)} - A_{IN(-)})$$

which equals the differential input voltage without any offset term.

RESULTS/CALIBRATION

The effect is to virtually eliminate any offset errors arising within the ADC, and, more importantly, to minimize any offset drift with temperature. The drift of these ADCs is specified as ± 10 nV/ $^{\circ}$ C typical. In fact it is virtually unmeasurable. The entire analog circuitry is chopped from the input mux to the modulator output. ADC offset calibrations are therefore not required. The offset error specification of the ADC is ± 3 μ V typical. This is measured with 0 V applied externally to the part sitting in a PCB socket, so mostly comprises thermocouple errors due to different metals used in the various contacts (PCB track, solder, lead frame, bond wire, die metallization, and so on).

UNDERSTANDING THE STEP RESPONSE

Since the ADC needs to perform a conversion for Chop = 0 and Chop = 1, the first output from the ADC takes two conversion periods ($2 \times T_{ADC}$), so there is a settling time of two conversion periods for the first output. Subsequent outputs occur every conversion period (T_{ADC}).

This delay of two conversions occurs after a channel is changed, after the PGA gain is changed, or after an ADC mode change, for example, after exiting power-down, so there are no intermediate/invalid outputs produced—the first output after a channel change is 100% settled to the new channel voltage.

If the analog input undergoes a step change external to the ADC, for example, if a sensor output changes suddenly or an external mux is switched, the ADC will not automatically “know” a change has occurred. It will produce outputs that are a weighted average of the new input and the old input, unless the ADC is directed to start a fresh conversion by means of interrupting the converter when the external mux is switched, then restarting the ADC so it produces an output $2 \times T_{ADC}$ later.

There is nothing unusual about the ADC producing intermediate values after a change in the input signal. This behavior is identical to that of an analog filter. If a step change is applied to the input of an analog low-pass filter, for a period of time the output will reflect a combination of the old analog input and the new analog input. It’s only after a sufficient number of time constants have elapsed that the output of the filter fully reflects the new input value.

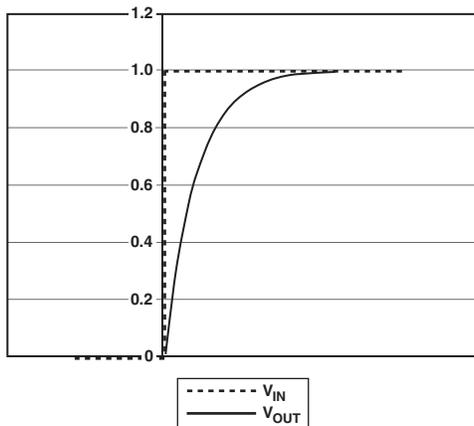


Figure 2. Analog Filter Step Response

These Σ - Δ ADCs contain a low-pass FIR filter with a given 3 dB frequency and settling time, so its response is similar in discrete time, although with a finite duration impulse/step response.

The only characteristic of these ADCs that may be unexpected is that there can be two intermediate outputs after a change in analog input. This is a consequence of chopping. As explained above, a chopped ADC output is the average of the current ADC conversion and the previous one. If the analog input changed part way through an ADC conversion period, then the current ADC conversion will reflect a combination of the old analog input and the new input, and the averaged result will be an intermediate value. The next (unaveraged) conversion will

purely reflect the new input. However, when averaged with the previous conversion, it will not yet give the final value, so it produces the second unsettled output. Only the third output will be fully settled (see Figure 3 (i)).

Some other Σ - Δ ADCs restrict the ADC to producing outputs effectively every $2 \times T_{ADC}$, i.e., at half the possible throughput. In this case there is at most one intermediate result after a change in analog input, due to the slower ADC conversion rate (see Figure 3 (ii)). This has been referred to as having “no latency,” but in fact such ADCs have a higher latency in response to a step input than these ADCs from Analog Devices.

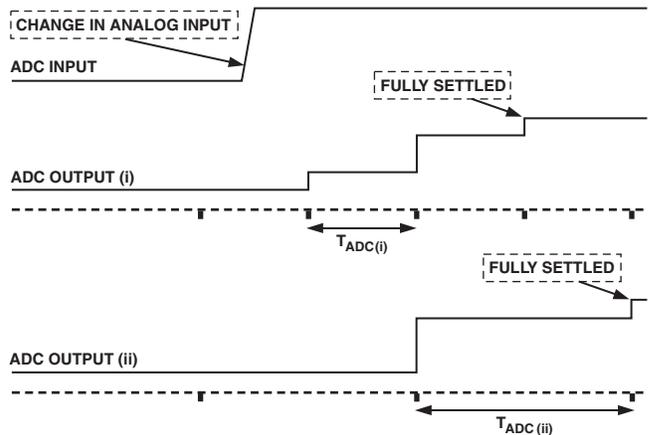


Figure 3. Comparison of ADC Latency with (i) and without (ii) Extra ‘Intermediate’ Results

Which scheme is the best? In most applications the need to get information as fast as possible is most important. For example, in safety-critical control systems the sooner you get an indication that a reaction is going to overheat, the sooner corrective action can be taken.

With faster outputs from the ADC, there is an earlier indication that the analog input has changed than there is if the ADC only provides an output every $2 \times T_{ADC}$. This reduces the effective latency of the ADC.

If the step change is due to a change in an external mux, it usually is best to interrupt the ADC at the same time, and get a settled result $2 \times T_{ADC}$ later. But if the input change arises from a sudden change in a sensor output, it is more important to get an indication of this change as soon as possible because it is probably important.

FREQUENCY RESPONSE

Chopping also impacts the frequency response but primarily in a beneficial way. The action of the average-by-2 places notches in the response at odd multiples of $f_{OUT}/2$, which can provide improved 50 Hz/60 Hz rejection. See the accompanying Application Note on 50 Hz/60 Hz rejection.

SUMMARY

The primary purpose of chopping is the elimination of offset errors. On these ADCs from Analog Devices, the chopping does an excellent job of removing offsets. The fact that two ADC conversions are required for one output could be a downside, however, the method implemented in these ADCs means there is little degradation in response time to detecting changes of the input signal. There is some misleading information available about the latency response of Σ - Δ ADCs, so this Application Note attempts to show how this family of ADCs provides a more optimal solution.

