

Input Buffers on Σ - Δ ADCs

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INTRODUCTION

The AD7708/AD7718, AD7709, AD7719, AD7782/AD7783 high resolution Σ - Δ ADCs from Analog Devices feature a high impedance buffer at the input to the ADC, as shown in Figure 1.

This application note discusses the significant benefits and various system design considerations that result from the integration of on-chip buffers.

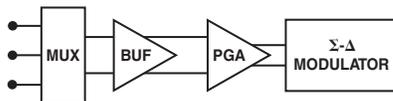


Figure 1. Typical Σ - Δ ADC Input Stage Including On-Chip Buffer

WHY BUFFERS?

The AD7708/AD7709/AD7718/AD7719/AD7782/AD7783 ADCs use a switched capacitor input stage to the Σ - Δ modulator.

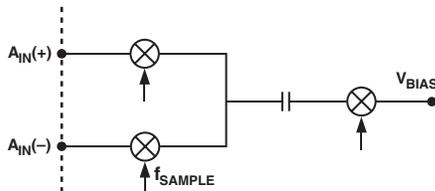


Figure 2a. Switched Capacitor Input

This structure has very high impedance in the steady state but requires a charging current every time the switches open and close to charge the sampling capacitor to the input voltage.

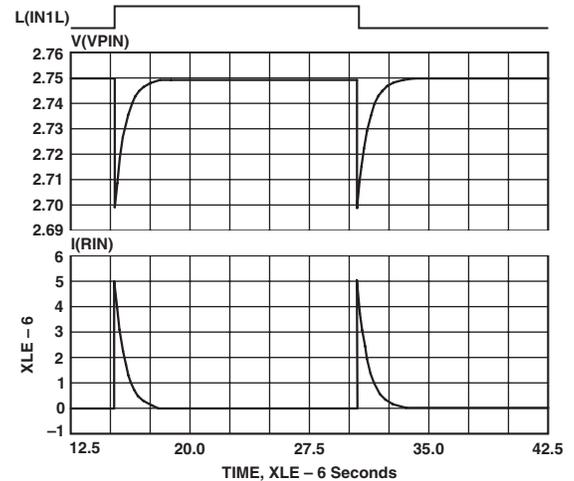


Figure 2b. Charging Current with $R_{EXT} = 10\text{ k}\Omega$, $C_{EXT} = 50\text{ pF}$

The magnitude of this current depends on the sampling frequency, differential input voltage, and capacitor size, but in general the average current increases for higher performance (lower noise) ADCs. The average current required on these parts is typically 125 nA/V, but if the PGA is on a range setting other than $\pm 2.56\text{ V}$, the required current increases, reaching 1 $\mu\text{A/V}$ on the $\pm 0.32\text{ V}$ range.

If a buffer is not present, this dynamic load places restrictions on the maximum values of external resistance and capacitance that may be used. Excessive values of R and C can result in ADC gain errors as a result of the input signal not being able to fully charge the input capacitor during the sampling period. The AD7719 can operate without a buffer by setting the $\overline{\text{BUF}}$ bit in the MODE register. The maximum external resistance that can be tolerated in this mode for less than 15 ppm gain error (one 16-bit LSB) is 110 k Ω when C = 0 while on the 2.56V range.

The allowable resistance decreases rapidly for higher accuracies, gains, and capacitances, e.g., the maximum resistance is 1.3 k Ω for 1 ppm (20-bit) gain error with $C = 100$ pF on the 320 mV range. See the AD7719 data sheet. The current drawn is quite stable over temperature, so does not directly contribute to gain drifts. However, external components often drift in value over temperature so the voltage dropped across them due to the input current will vary and could result in a significant gain drift.

For signals with low source impedance, an unbuffered input may be suitable. However, many common sensors have significant source impedances. In addition, it's often necessary to place R-C filters in front of the ADC for protection or for filtering. In these situations an input buffer is required. Finding an external low power amplifier to drive this dynamic load is a difficult task, so one is provided on the ADC.

INPUT BUFFER CHARACTERISTICS

The input buffer on these ADCs has a guaranteed maximum input current of 1 nA over the full temperature range (-40°C to $+85^{\circ}\text{C}$) with a drift of typically 5 pA/ $^{\circ}\text{C}$. Guaranteeing low leakage over temperature is significant because many semiconductor components suffer elevated reverse leakage currents at high temperatures. The specifications on the design and implementation of the buffer are stringent; it must have high open-loop gain to maintain the sub ppm/ $^{\circ}\text{C}$ gain drift of the ADC over temperature, and it must have sufficient bandwidth to source the dynamic currents into the switched capacitor load of the ADC. Although drawn as a single buffer in Figure 1, the two signals comprising the differential input have individual buffers.

RAIL-TO-RAIL INPUTS

Buffers have been used on high resolution Σ - Δ ADCs for some time (for example, on the AD7714), but there have been some limitations to their use. Possibly the most severe limitation has been the restriction on the input voltage range. On the AD7714 the input was constrained to be at least 1.5 V lower than the analog supply voltage. This limits the input signal swing, particularly when operating with 3 V supplies (see Figure 3a).

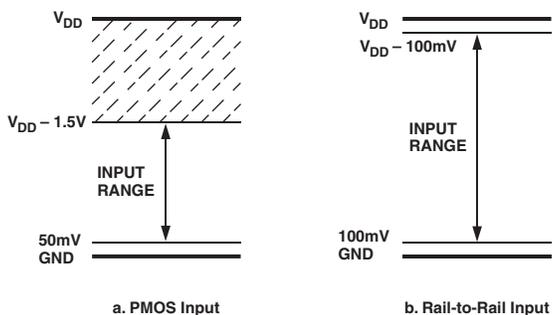


Figure 3. Input Ranges

This restriction arises from the input devices of the buffer. With a PMOS differential pair as the input structure, the input signal must be significantly below the supply voltage to keep the input devices and current mirrors in their active region. An NMOS input stage can accept signals up to V_{DD} but cannot accept signals near ground.

Attempts have been made to use both PMOS and NMOS pairs in the input stage to accept any input voltage, but problems arise because the signal transitions between pairs. Typically the two input pairs have different offsets, and chopping is not completely effective at canceling the offset error in the transition region.

Another attempt at avoiding this problem is to partition the sampling period so that the buffer is used to charge the capacitor to approximately the correct value, and is then bypassed for completing the charging. However, this method still requires dynamic current to be sourced from the signal, and this current varies with buffer offset, input voltage, and so on. In addition, the spike of current occurs shortly before the critical sampling instant—exactly when the signal must be stable. This scheme may give the impression of low input currents when averaged over a full sampling period, but the signal must source this spike of current in a short time before the sampling instant, so the allowable source impedance is smaller than it first appears.

These recent parts from Analog Devices use a novel scheme (patent pending) that discretely switches between an NMOS and PMOS input pair, depending on the input voltage level. This switching is synchronized with the modulator sampling frequency.

The result is the best of both worlds, a PMOS pair when the signal is near ground and an NMOS pair when the signal is near V_{DD} , with a controlled switchover between the two input stages. This allows almost complete removal of offset at any input voltage by chopping (see Figure 3b). The input devices for each of the two signals comprising the differential input are separately selected in the respective buffers.

The only remaining limitation is that the signal must be within 100 mV above ground and 100 mV below V_{DD} , due to headroom requirements on the buffer output stage. The buffered input cannot be grounded. For many sensor systems with bridge configurations, this is not an issue, so the buffer can be used with a wide signal swing. On the AD7719, the input buffer can be bypassed, allowing the input signal swing from -30 mV to $AV_{DD} + 30$ mV, but it must be low impedance.

GROUNDING INPUTS

The restriction that the input must be greater than 100 mV raises a potential problem for high impedance signals that are ground-referenced, i.e., $A_{IN(-)} = 0$ V. Since there are two buffers available, there is a solution. The AD7708/AD7709/AD7718 uniquely address this issue by allowing the buffer on the negative input to be bypassed when the ADC is configured to accept single-ended inputs (CH3 bit in ADCCON[7] = 0 on AD7708/AD7718 or CH2 bit in CONFIG[6] = 0 on AD7709.) In this case, AINCOM can be tied directly to ground while the positive input is buffered, so it can still have significant impedance. Ground should be a low impedance node so there are no gain error concerns with driving the switched capacitor load. The positive input must always be above 100 mV. Single-ended signals are typically large scale, so this is unlikely to cause too many problems. (This feature can be disabled on the AD7708/AD7718 by setting the NEGBUF bit in MODE[6].)

NOISE, OFFSET, AND POWER CONSIDERATIONS

The noise contribution of this buffer is small, roughly 10% extra, so there is no performance penalty in using the buffer. Any offset errors within the buffer are automatically removed by chopping, which draws virtually no input current. The buffers typically require 0.4 mA supply current for the two when active, which is very competitive compared to external op amps.

REFERENCE INPUT

The reference inputs on the ADC also go directly to a switched capacitor input stage, so similar comments with regards to maximum resistance and capacitance apply. The reference signal is usually low impedance so this is generally not a problem. Because these ADCs can accept a reference voltage of V_{DD} , it means that bridge circuits can use V_{DD} and GND as the bridge excitation voltages and that these low impedance nodes can be tied directly to the ADC reference inputs. For other circuit configurations, a reference such as the AD780 is capable of driving the ADC load directly. If the reference is generated by a resistor divider or by a current through a resistor, the resistance should be kept below approximately 10 k Ω to help avoid gain errors.

SUMMARY

The primary benefit of an integrated high impedance input buffer is that it enables an ADC to be connected directly to almost any type of sensor, regardless of impedance. This is illustrated most clearly in Figure 4, which shows the AD7719 main ADC connected directly to an external (voltage excited) strain gage.

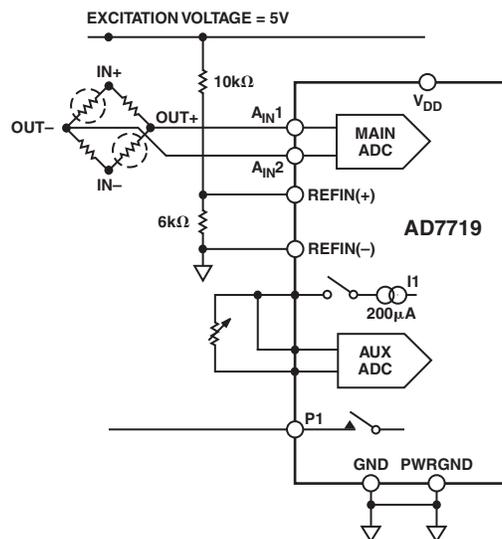


Figure 4. Direct Connection to Resistive Sensor

The auxiliary ADC is also connected directly to an external resistive temperature detector (RTD), facilitating optional temperature compensation of the main ADC measurement. The direct connection to the high resistance strain gage sensor is made possible by the on-chip input buffer.

Rail-to-rail operation eliminates the restricted signal swing of previous generations of buffers, while the noise contribution of the buffer is minimal, even for such high resolution ADCs. The automatic negative buffer bypass on the AD7708/AD7709/AD7718 is a novel solution for applications with ground-referenced single-ended inputs.

The cost of using buffers is higher operating current, although this is usually acceptable, especially considering that extra current would also be required when using an external buffer, and the internal buffer offers a much neater single-chip solution.

