AN-591
APPLICATION NOTE

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ADM1070 Hot Swap Controller

by Alan Moloney

INTRODUCTION

The ADM1070 is a negative voltage (−48 V) hot swap controller. The device provides robust current limiting, protects against transient and nontransient short circuits, and offers single-pin undervoltage and overvoltage protection. The ADM1070 has many applications, such as central office switching, −48 V distributed systems, and negative power supply control. This application note describes the operation of the ADM1070 under various hot swap insertion and removal conditions. This document should be consulted in conjunction with the ADM1070 data sheet and evaluation board documentation. All of the tests described in this application note can be recreated with the ADM1070 evaluation board.

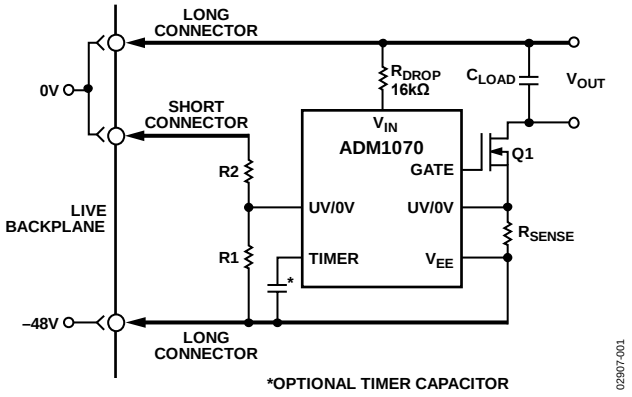

Figure 1. Circuit Diagram (ADM1070 Residing on a Plug-In Module)

The ADM1070 is designed to reside on a plug-in board or a live backplane and uses a FET in the power path to control the load current. It requires a few other external components to operate, such as a shunt resistor, two divider resistors, and a SENSE resistor. A 16 kΩ shunt resistor is required between the 0 V line and the V_{IN} pin to power the part.

Resistors R1 and R2 form a resistor divider that scales down the supply voltage to a range that the device can measure. The divider output is used for undervoltage/overvoltage detection at the UV/OV pin. By choosing the values of R1 and R2 carefully, the part can be programmed to apply the supply voltage to the load only when the supply is in the desired range. The default evaluation board resistor values give an operating range of around −36 V to −75 V. Refer to the Resistance Ratios and Operating Voltage Windows table of the ADM1070 data sheet for a full description of how the operating voltage window can be programmed.

The SENSE resistor, R_{SENSE}, is used for current limiting. The ADM1070 continually senses the voltage across R_{SENSE} and can detect whether the load current is above the maximum permitted load current value. If it is, the ADM1070 reduces the voltage on the GATE of the FET to reduce the load current to an acceptable level. The load current limit is set by the choice of R_{SENSE}. The $I_{LOAD(MAX)}$, $I_{LIMIT(MIN)}$, and $I_{LIMIT(MAX)}$ for Different Values of R_{SENSE} table in the ADM1070 data sheet shows the value of the load current permitted to flow during inrush and quiescent conditions for the different choices of R_{SENSE}.

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REVISION HISTORY

5/13—Rev. A to Rev. B

Updated Format ..... Universal
Changes to Introduction 1

9/02—Rev. 0 to Rev. A

POWERING UP

The timing waveforms associated with the live insertion of a plug-in board using the ADM1070 are shown in Figure 2. In a system that has been mechanically designed such that the power rails connect first, the GND–V_{EE} potential climbs to 48 V. As this voltage is applied, the voltage at the V_{IN} pin ramps above the undervoltage lockout (V_{LKO}) of 8.5 V (internal to device) to a constant 12.3 V and is held at this level by the internal Zener diode. Because of the staggered configuration of the connection pins, the R1/R2 resistor divider is the last to connect to the backplane.

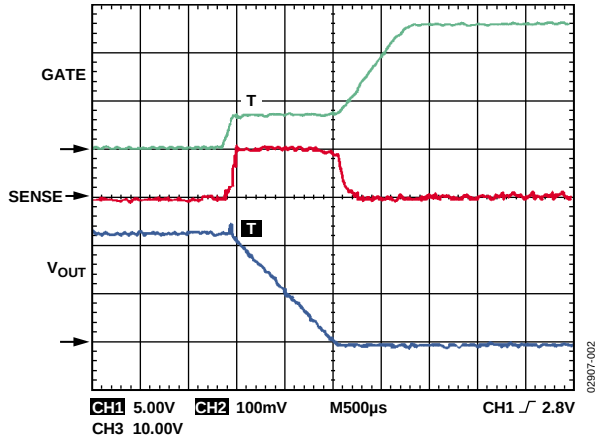

Figure 2. Timing Waveforms Associated with a Power-Up Sequence

When the voltage at UV/OV crosses the undervoltage rising threshold of 0.91 V, it is now inside the operating voltage window and the −48 V supply must be applied to the load. After a time delay, t_{POR}, the ADM1070 begins to ramp up the GATE drive. Initially, the load capacitance may attempt to draw a large current. When the voltage on the SENSE pin reaches 100 mV (the analog current limit), the GATE drive is held constant. When the board's capacitance is fully charged, the SENSE voltage begins to drop below the analog current limit voltage and the GATE voltage is free to ramp up further. The GATE voltage eventually reaches its maximum value of 12.3 V (as set by V_{IN}).

Note that long/short connector configuration is not a requirement.

OVERVOLTAGE CONDITION

The waveforms for an overvoltage glitch are shown in Figure 3. When UV/OV rises above the overvoltage rising threshold of 1.97 V, an overvoltage condition is detected and the GATE voltage is pulled low. UV/OV begins to drop back toward the operating voltage window and the GATE drive is restored when the overvoltage falling threshold of 1.93 V is reached.

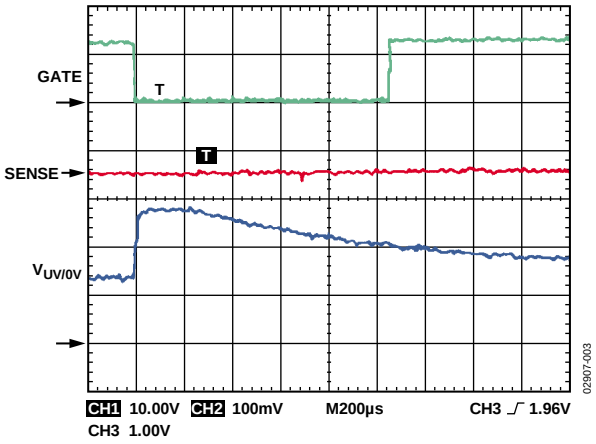

Figure 3. Timing Waveforms Associated with an Overvoltage Glitch

UNDERVOLTAGE CONDITION

An undervoltage glitch is dealt with in a similar way. When UV/OV falls below the undervoltage falling threshold of 0.86 V, the GATE voltage is pulled low. If UV/OV subsequently rises back above the undervoltage rising threshold of 0.91 V, the GATE voltage is restored. Figure 4 illustrates the ADM1070 operation in an undervoltage situation.

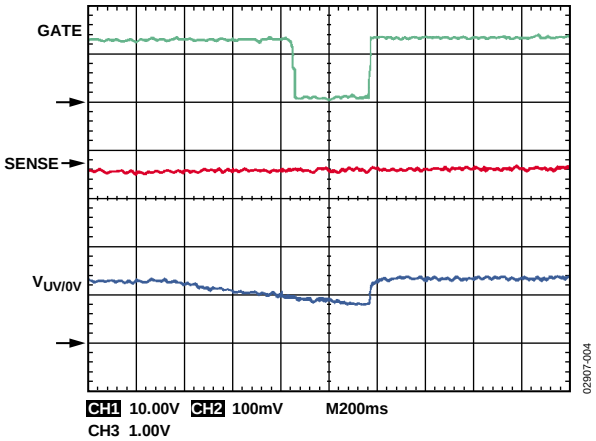

Figure 4. Timing Waveforms Associated with an Undervoltage Glitch

CURRENT FAULT PLOTS

Some timing waveforms associated with over current faults are shown here. Figure 5 shows how a current glitch (of approximately 500 µs) is dealt with when the output is shorted after power-up. The GATE voltage is at a constant 12.3 V before the glitch occurs. When the SENSE voltage reaches 100 mV (V_{ACL}), the ADM1070 reduces the GATE voltage to stop the load current from increasing any further. When V_{SENSE} drops back below V_{ACL}, the GATE voltage is increased again.

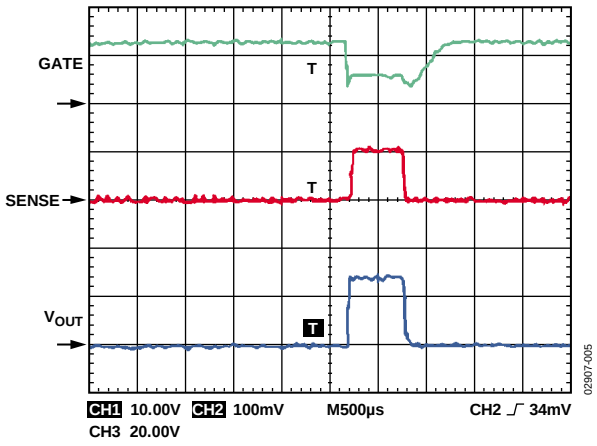

Figure 5. Timing Waveforms Associated with a Current Fault (after Power-Up)

Figure 6 to Figure 8 show the operation of the ADM1070 unique limited consecutive retry function. Figure 6 highlights what happens when a current fault occurs for more than 14 ms (default $t_{LIMITON}$ when TIMER pin tied to V_{EE}) and a current fault is registered. In this case, GATE is previously low and the part is being powered up into a current fault situation (shorted load). When power is applied, GATE is allowed to ramp until SENSE reaches 100 mV. Gate is then held constant to keep SENSE at this level. After $t_{LIMITON}$, the PWM cycle begins and GATE is reduced to zero.

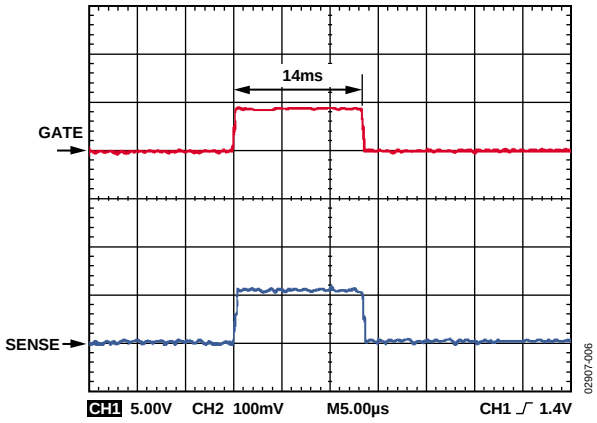

Figure 6. Timing Waveforms Associated with a Current Fault

Figure 7 shows a current fault on a wider time base. The first spike on the SENSE line represents the first current fault. The SENSE voltage is allowed to ramp up to 100 mV before the GATE voltage is reduced to compensate. The GATE and SENSE voltages remain at these levels until the time, t_{ON}, has expired.

A current fault is then registered and the GATE voltage and thus the SENSE voltage are both held low for the time period t_{OFF}. Note that the PWM ratio (t_{ON}/t_{OFF}) is equal to 3%. The cycle then restarts and the SENSE voltage is free to ramp up to 100 mV again (it will if the fault is still present). This cycle repeats itself a total of seven times. Figure 8 shows the seven consecutive faults occurring on an even wider time base. If the ADM1070 detects seven consecutive current faults, the part then latches off (after a total time t_{SHORT}).

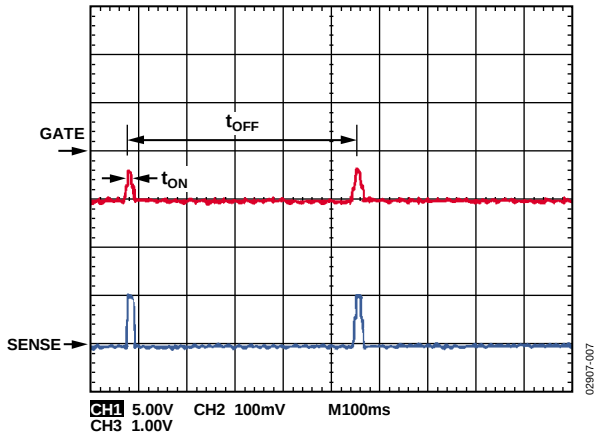

Figure 7. Illustration of the PWM Ratio (t_{ON}/t_{OFF})

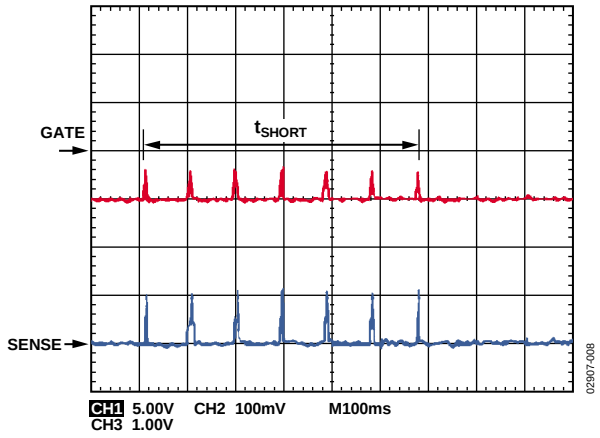

Figure 8. Illustration of the Limited Consecutive Retry Function (Seven Retries and Latch Off)

TEMPORARY CURRENT FAULT

The ADM1070 behaves in the following way when a temporary current fault occurs. When the fault occurs, the SENSE voltage rises to 100 mV. The GATE voltage is reduced to keep the SENSE voltage at this level. When the 3% duty cycle ON time has elapsed, the GATE and SENSE voltages both drop to zero for the remainder of the cycle. When the cycle is complete, GATE is free to ramp up again to a level that maintains SENSE at 100 mV. If the current fault is removed before seven retries have occurred (and the ADM1070 latches off), the SENSE voltage will drop back below 79 mV (the circuit breaker limit voltage [falling]), allowing GATE to ramp back up to 12.3 V and turning the FET fully on.

TEMPORARY CURRENT FAULT FOLLOWED BY A PERMANENT CURRENT FAULT

Figure 9 shows the behavior of ADM1070 when a temporary current fault is followed by a permanent current fault. When the first overcurrent fault occurs, the first 100 mV spike on the SENSE line can be seen. During the t_{OFF} time, this current fault is removed. After this time period, a no fault condition is detected and the limited consecutive counter is reset. GATE is driven fully on. When the overcurrent fault returns permanently, the limited consecutive retry circuitry detects seven consecutive faults and the part latches off.

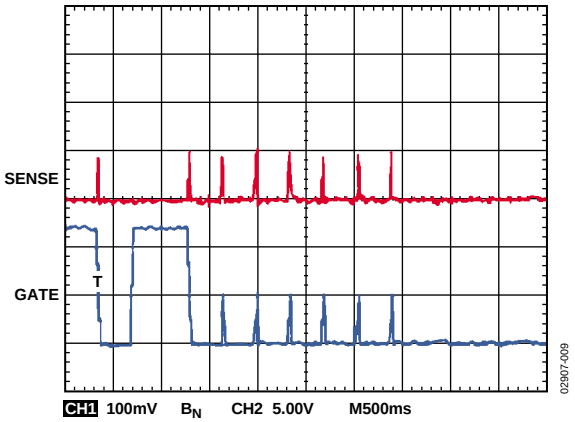

Figure 9. Waveforms Associated with a Temporary Current Fault Followed by a Permanent Current Fault

RESEATING A CARD

A standard reset procedure used in central office systems is to reseat a card/module (that is, the operator removes the card from the live backplane and reinserts it again quickly). Not all hot swap supervisory solutions monitor the load current continuously. In these cases, the GATE voltage is simply slew rate limited to control the rate at which the load current is allowed to ramp up at startup.

In Figure 10, V1 = −48 V backplane supply, V2 = the voltage across the input connector of the plug-in card, and V3 = the hot swapped voltage (the voltage across the load of the card).

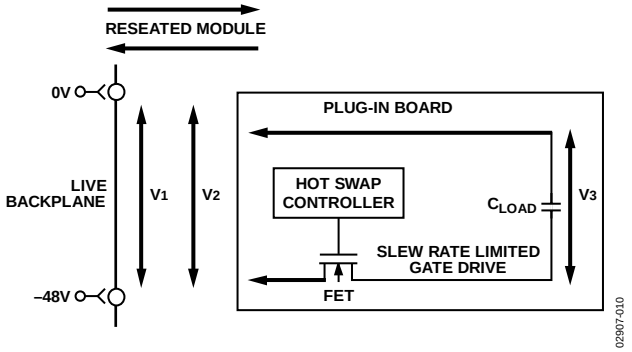

Figure 10. Reseating a Module with a Slew Rate Limited Hot Swap System

Initially, V1 = −48 V and V2 and V3 = 0. When the plug-in module is initially connected, V2 instantly ramps to −48 V. The hot swap controller ramps the GATE voltage at its maximum slew rate, which ensures that the load current is applied in a controlled manner. V3 ramps to −48 V.

If the card is now disconnected, V2 floats, but V3 does not fall instantly because it must be discharged by the board load current (this may take some time). The FET is still on at this time, holding V2 at a voltage close to V3. The hot swap device thinks the supply is still good and will therefore not try to turn off the FET.

If the card is now reseated, V2 instantly charges to −48 V, but the load capacitance holds V3 at some voltage between 0 V and −48 V. The drain source of the FET now has to handle the voltage difference between V2 and V3 (V3 − V2). So the FET now has this voltage across its drain source terminals with its GATE drive fully on. Unlimited current can now flow and board failure will occur.

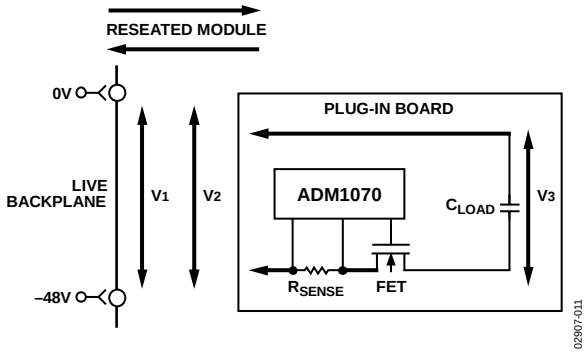

Figure 11. Reseating a Module Containing the ADM1070

The ADM1070 uses a SENSE resistor to limit the load current in both inrush and short-circuit situations. The voltage across the SENSE resistor is continually sensed to make sure the load current is below the level permitted (by the choice of R_{SENSE}). The GATE voltage is increased or decreased based on the current level, which in turn drives the FET out of or into the resistive region, increasing or decreasing the current flowing in the load.

If a short circuit does occur, then the ADM1070's limited consecutive retry function will be employed. This unique function offers an ideal trade-off between single-fault latched shutdown and infinite auto-retry features. It also ensures that the system has adequate time to recover if the current fault is temporary, but it will not enter an infinite retry loop if the fault is permanent (which is usually the case with a current fault).

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