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## AN-582 Resolution Enhancements of Digital Potentiometers with Multiple Devices

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### Introduction

Digital potentiometers usually come with standard resistance values of 10k, 100k, and 1M $\Omega$  at a given number of adjustable steps. If an application requires a resistance range that falls between these values, users will most likely apply a part with a resistance larger than needed sacrificing resolution. Fortunately, users can parallel, stack, or cascade multiple digital potentiometers to optimize the resolution for a given application. In this article, we will share some of the ideas that may solve the challenge.

### Paralleling Digital Potentiometers

If an application requires a value adjustment from 1k $\Omega$  to 5k $\Omega$ , the user may parallel two 10k $\Omega$  digital potentiometers. Figure 1 shows a simple paralleling scheme of two digital potentiometers in the rheostat mode. In order to adjust half of the resistance per step, the user needs to program the devices coherently with the same settings.

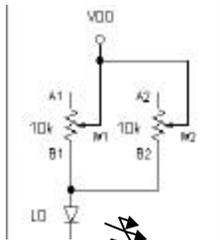


Figure 1. Paralleling Digital Potentiometers in Rheostat Mode

When using digital potentiometers in the voltage divider mode, the user may scale the window of adjustment and parallel multiple devices for finer resolution as shown in Figure 2.

In these methods, the user should be aware of the tolerance mismatch in order to predict the worst case conditions.

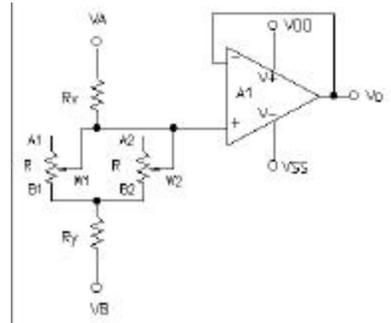


Figure 2. Paralleling Digital Potentiometers in voltage divider mode

### Stacking Digital Potentiometers

If an application requires 20k $\Omega$  with maximum number of adjustable steps, the user may stack two 10k $\Omega$  parts along with a SPDT switch. Digital potentiometers such as AD5242, AD5231, and AD5233 that feature extra logic output controls are particularly suitable in such application. Refer to Figure 3, here the output control  $O_1$ , from AD5242, can be used to toggle the switches of ADG752 such that  $S_1$  and  $S_2$  turn on interchangeably. As a result, the user can program  $V_0$  from 0 to  $V_i/2$  when  $S_2$  is on. Similarly, the user can program  $V_0$  from  $V_i/2$  to  $V_i$  when  $S_1$  is on. In this example, the number of adjustable steps increases from 256 to 512. Similarly, stacking four AD5231 and using a 4x1 MUX ADG704 increases the numbers of adjustable steps from 1024 to 4096, see Figure 4.

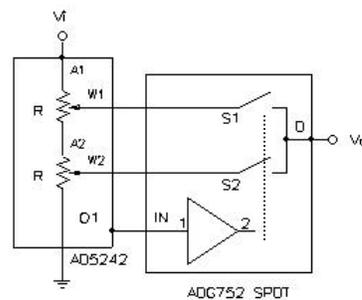


Figure 3. Stacking Two Digital Potentiometers Doubles the Numbers of Steps.

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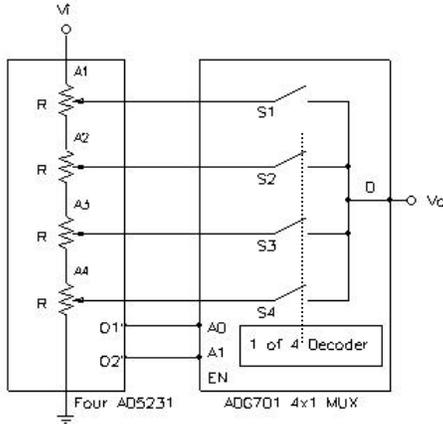


Figure 4. Stacking Four Digital Potentiometers Quadruples the Numbers of Steps.

### Cascading Digital Potentiometers

The user may also optimize the adjustment range by cascading two digital potentiometers as shown in Figure 5. Here the user controls the first digital potentiometer to achieve the desired window of adjustment and then controls the second device to obtain the  $2^N$  number of adjustable steps within this window. This approach is only good for low voltage range of adjustment. For example, when  $R_1$  is set at a very low value, further fine steps can be adjusted by  $R_2$ . However, the user who attempts to use the full range of  $R_1$  will find there are many redundant steps in such approach.

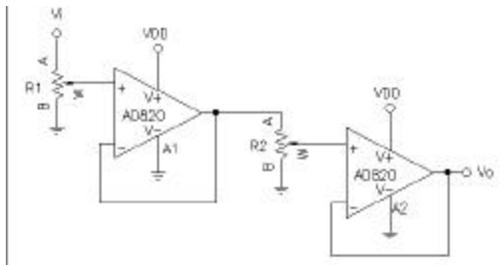


Figure 5. Cascading Digital Potentiometers.

An alternate approach is shown in Figure 6. It is possible to double the resolution, for example from 64 to 4096 adjustable steps (from 6-bit to 12-bit) by cascading three channels of digital potentiometer AD5233. In this architecture, it can be shown that  $V_o$  equals

$$V_o = \underbrace{\left[ \frac{D}{2^N} V_A \right] \frac{2^N + 1}{2^N + 2}}_{\text{coarse } 2^N \text{ adjustment}} + \underbrace{\left[ \frac{D_3}{2^N} V_A \right] \frac{1}{2^N + 2}}_{\text{fine } 2^{2N} \text{ adjustment}} \quad (1)$$

where  $D$  is the decimal equivalent of the data bits of  $U_1$  and  $U_2$  adjusted coherently.  $D_3$  is the decimal equivalent of the data bits of  $U_3$ . By examining equation 1 closely, we can determine that  $V_o$  is the sum of two terms. The first term represents a standard  $2^N$  adjustment since the scale factor  $(2^N + 1)/(2^N + 2)$  approaches unity. The second term represents the fine  $2^{2N}$  adjustment if we approximate the scale factor  $1/(2^N + 2)$  as  $1/2^N$ . This idea is in fact borrowed from ADI's patented RDAC segmentation design, which optimizes chip size and resolution. There are some caveats of this approach. First, it is essential to adjust  $D_1$  and  $D_2$  coherently, meaning to program  $U_1$  and  $U_2$  one after another or simultaneously with the same settings. Second, it is also important to choose an  $R_p$ , equal to a step resistance of the digital potentiometer, to achieve the fine  $2^{2N}$  adjustment. Finally, the user must consider the tolerance mismatch and tempco mismatch between  $R_p$  and the digital potentiometer. Notice also that this approach is simply a low cost alternative of 12-bit DAC. It offers the same numbers of steps adjustment. However, it is not as accurate as the conventional DACs because of its wiper resistance effects that skews the linearity.

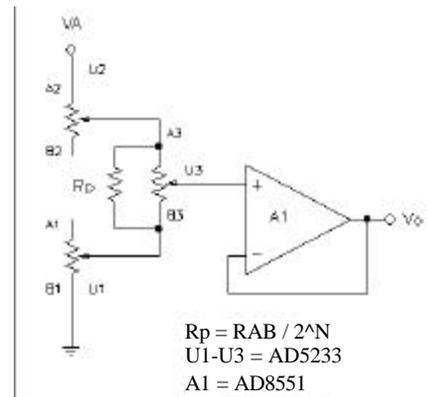


Figure 6. Digital Potentiometers with 12-bit resolution.

### Conclusion

While enhancing the resolution is desirable by using multiple digital potentiometers, the user should be aware the trade-off of accuracy and add-on programming complexity.