

Layout Considerations when Adding Energy Monitoring to a System Using the **ADE9153A**

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INTRODUCTION

Adding energy measurement to a system typically involves an extensive calibration process. The [ADE9153A](#), an energy metering IC with an *mSure*® autocalibration feature, simplifies the calibration process of the energy measurement system. The [ADE9153A](#) can be integrated into a variety of applications for systems such as street lighting, the measurement of data center energy efficiency, smart power distribution, smart plugs, and machine health.

Figure 1 shows the basic connection of the [ADE9153A](#) to a single phase system configuration with a shunt resistor used for current sensing and potential dividers for voltage sensing. The isolation barrier separates the controller from the [ADE9153A](#) device, which is a requirement for many applications because the [ADE9153A](#) ground is at a hazardous voltage.

This application note describes layout considerations when adding an [ADE9153A](#) energy monitoring circuit to an existing system.

In addition to this application note, refer to the [ADE9153A](#) data sheet, the [ADE9153A Technical Reference Manual](#), and the [EV-ADE9153ASHIELDZ](#) user guide.

TABLE OF CONTENTS

Introduction	1	Power Supply.....	7
Revision History	2	Grounding and Isolation	8
ADE9153A Layout Recommendations.....	4	Application Examples	11
Phase Current Channel.....	4	Smart Street Lighting.....	11
Neutral Current Channel (Optional).....	4	Energy Measurement on Multiple Outputs	11
Voltage Channel.....	5	Conclusion.....	12
Antialias Filters.....	6		
Crystals and Capacitors.....	6		

REVISION HISTORY

12/2018—Revision 0: Initial Version

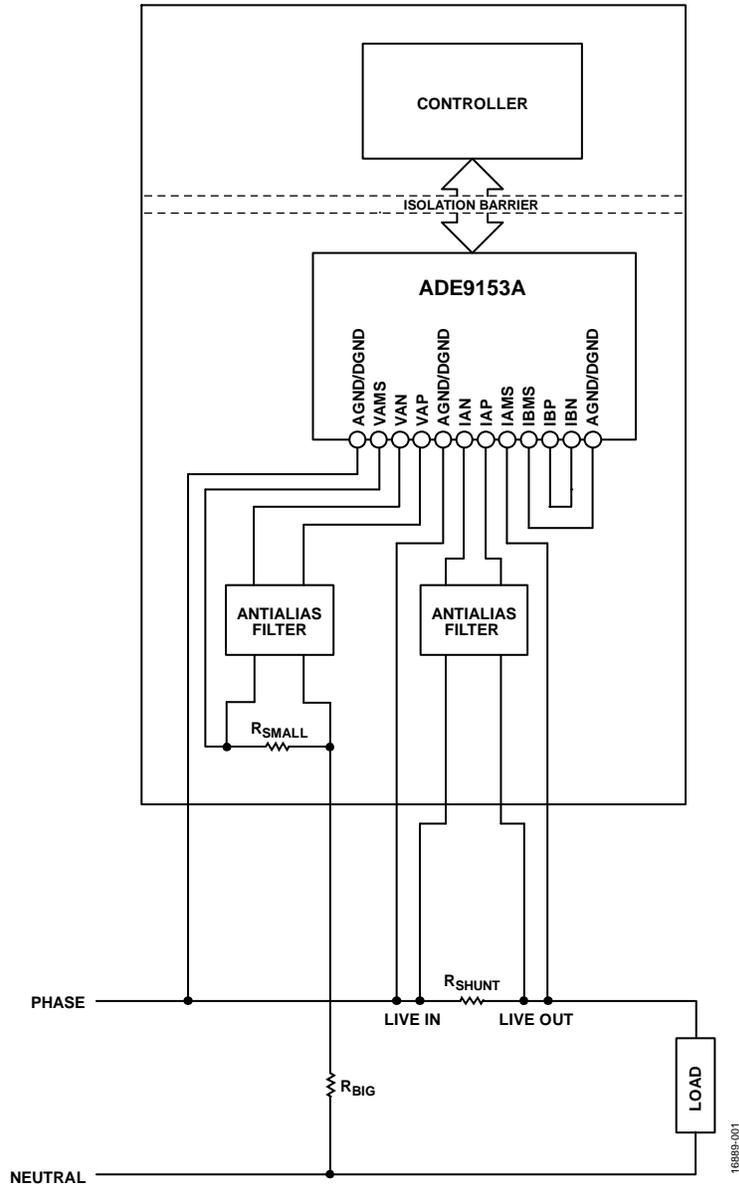


Figure 1. ADE9153A Connection to a Primary System (All Connections Not Shown)

ADE9153A LAYOUT RECOMMENDATIONS

The *mSure* feature of the ADE9153A requires special design considerations for the shunt, current transformer (CT), and printed circuit board (PCB) layout.

PHASE CURRENT CHANNEL

The current channel of the ADE9153A is different from current channel designs of other energy metering ICs because the ADE9153A requires additional terminals for the sensor and the PCB for *mSure* functionality.

The ADE9153A IAMS pin enables *mSure* injection into the current shunt. Layout is critical to the performance of the energy measurement system.

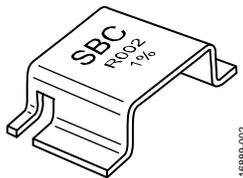


Figure 2. Surface-Mount Device (SMD) Current Shunt

Figure 2 shows an SMD current shunt with the EV-ADE9153ASHIELDZ. There is an additional footprint in the PCB that connects to the IAMS pin of the ADE9153A and the ground (GND) plane for *mSure* functionality.

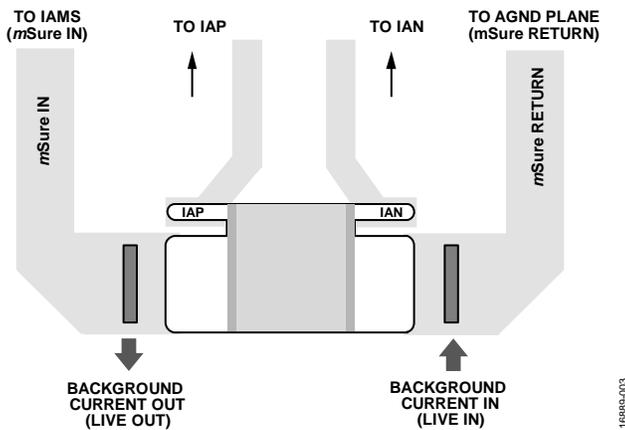


Figure 3. Recommended PCB Footprint and Trace for the SMD Current Shunt

Figure 3 shows the top view of the SMD current shunt with its recommended PCB footprint and trace. The IAP terminal of the shunt is the positive differential terminal of the current channel, and the IAN terminal of the shunt is the negative differential terminal of the current channel. Whenever, for design reasons, the signal of the current channel is more easily routed through the IAN pin, the background current to the shunt is reversed and the AI_SWAP bit in the AI_PGAGAIN register must be set to 0x0.

Figure 3 also shows an *mSure* in trace directly connected to the IAMS pin (Pin 6) and *mSure* return trace connected to the GND plane.

Keep the *mSure* in trace and the *mSure* return trace away from the analog-to-digital converter (ADC) input traces (IAP and

IAN). The *mSure* return signal must have the shortest return path possible to the ground plane, which connects to DGND (Pin 1).

During autocalibration, the IAMS pin of the ADE9153A outputs the *mSure* signal through the *mSure* in trace, and the signal is injected into the shunt. A capacitor with a value between 0.1 μF and 1 μF must be placed across the IAMS pin and GND plane close to the IAMS pin. This capacitor protects the circuit from electric fast transients (see Figure 4).

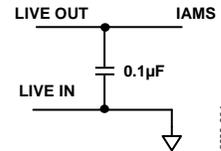


Figure 4. IAMS Capacitor for Immunity to Electric Fast Transients

The trace farthest from the IAMS pin must be approximately 1.5 mm wide to effectively manage the current flow from the IAMS pin. This trace slowly tapers off as it gets closer to the pin, until the trace reaches approximately 0.25 mm to match the pin width.

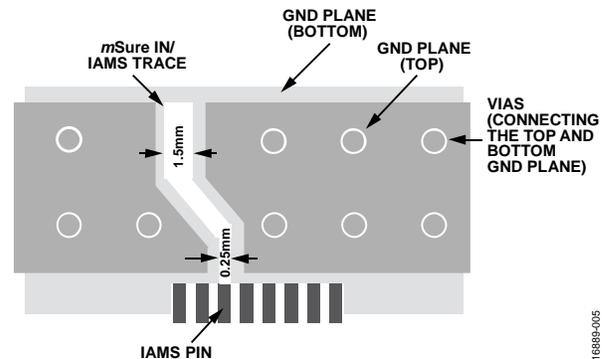


Figure 5. IAMS Trace

Figure 5 shows the PCB trace for IAMS (*mSure* in). This trace is surrounded by a GND plane on the top and bottom layers of the PCB, which are interconnected through vias.

NEUTRAL CURRENT CHANNEL (OPTIONAL)

Figure 6 shows the recommended use of a current transformer in the IB terminals (IMBS, IBN, and IBP). The *mSure* winding must be galvanically isolated from the neutral winding. Connect the IBMS terminal of the CT burden resistor directly to the IBMS pin (Pin 19) of the chip, and connect the IBMS_BACK terminal, the return wire or the *mSure* winding connected to the GND plane.

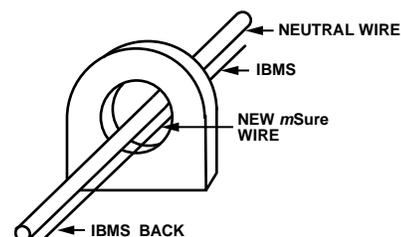


Figure 6. CT Design with *mSure* Injection Terminals

The IBMS pin of the [ADE9153A](#) outputs the *mSure* signal that is induced to the primary winding of the neutral wire CT. This signal must have the shortest possible return path to the GND plane, which connects to DGND (Pin 20). Place a capacitor between the IBMS trace and the GND plane close to the IBMS pin for immunity to electric fast transients. The recommended schematic and layout for IBMS is similar to the recommended schematic and layout for IAMS, shown in Figure 4 and Figure 5.

If the energy measurement system does not require a neutral current measurement, short the neutral current channel inputs IBN (Pin 11) and IBP (Pin 12). Additionally, short IBMS (Pin 19), which connects to the GND plane and to DGND (Pin 20), as shown in Figure 7.

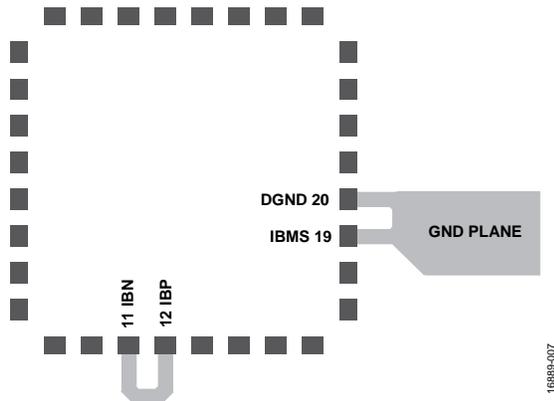


Figure 7. Recommended Trace Connection for Unused IBP Pin, IBN Pin, and IBMS Pin

VOLTAGE CHANNEL

Figure 8 shows the interface circuit to measure the mains voltage. The VAMS pin of the [ADE9153A](#) outputs the *mSure* signal, and this signal is injected into the bottom of the potential divider. The attenuation network on the voltage channels is designed so that the corner frequency (3 dB) of the network matches that of the antialiasing filters in the current channel inputs.

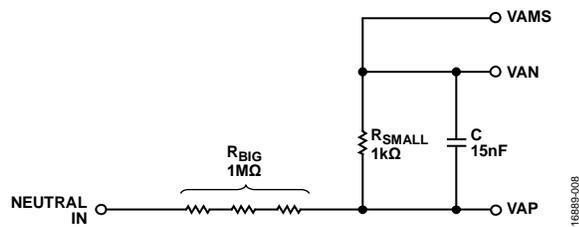


Figure 8. Voltage Channel Schematic

Short the VAN pin to the VAMS pin and create a full guard around the VAP trace, as shown in Figure 9. Create the guard with a bare copper VAMS trace all the way around the VAP trace, 0.1 mm in width.

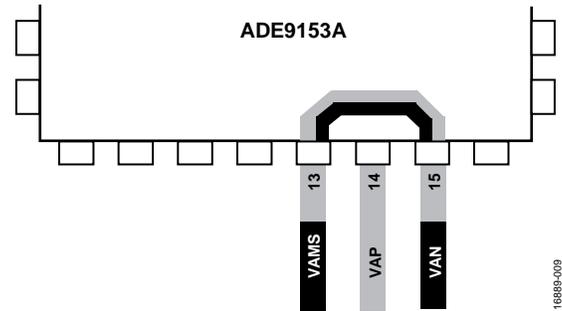


Figure 9. VAP Trace

A guard trace must pass under the [ADE9153A](#) package and connect the VAMS pin to the VAN pin. The trace must be as close to the VAP pin as possible and include a small portion of bare copper, as indicated by Label 3 in Figure 10.

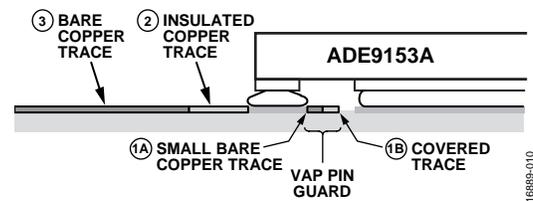


Figure 10. Side View of [ADE9153A](#) and VAP Pin Guard

Figure 10 shows a side view of the [ADE9153A](#) mounted to the PCB layout of the VAP pin guard. The numbered labels in the figure are as follows:

- Label 1A and Label 1B indicate the guard behind the VAP pin. Shorting this bare copper trace to the exposed pad of VAMS (Pin 13) and VAN (Pin 15) of the [ADE9153A](#) footprint does not have any negative effects on the performance of the device. Ensure that this trace has enough space to avoid shorting the trace to the exposed pad in the center of the [ADE9153A](#) footprint.
- Label 2 indicates a covered trace between the bare copper trace and the exposed pad of Pin 13 and Pin 15. Ensure that this trace is insulated for easy soldering of the device.
- Label 3 indicates the full bare copper that follows the trace to the potential divider. For easy soldering, ensure that this bare copper trace does not extend to the exposed pad of Pin 13 and Pin 15 of the [ADE9153A](#) footprint. Ensure that the trace near the pins is completely insulated and not bare.

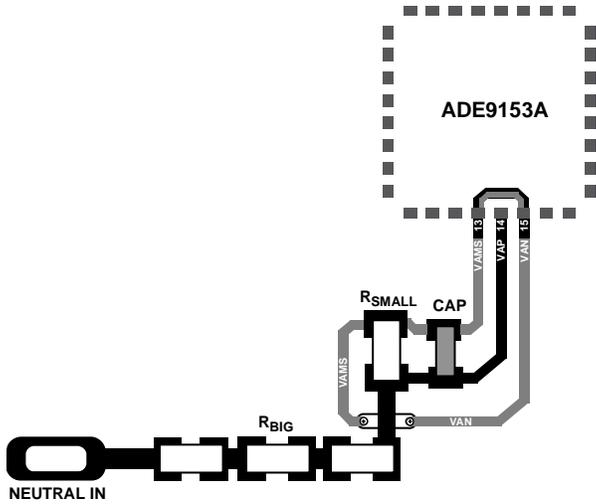


Figure 11. VAMS and VAN Guard

For noise immunity purposes, a small trace surrounds the VAMS and VAN guard connection through vias and the bottom layer trace (see Figure 12).

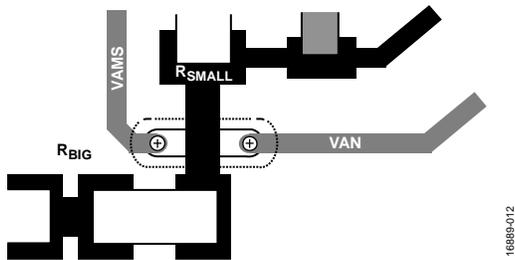


Figure 12. VAMS and VAN Interconnection Through Vias

ANTIALIAS FILTERS

Figure 13 and Figure 14 are schematics of the antialias filters of the current channels. The filters must be placed close to the terminals of the current shunt, or the CT if there is a neutral channel. In the layout, ensure that the antialiasing capacitors are symmetric and close to the analog front end, with parallel traces feeding into the pins. The Voltage Channel section describes the antialias filter for the voltage channel.

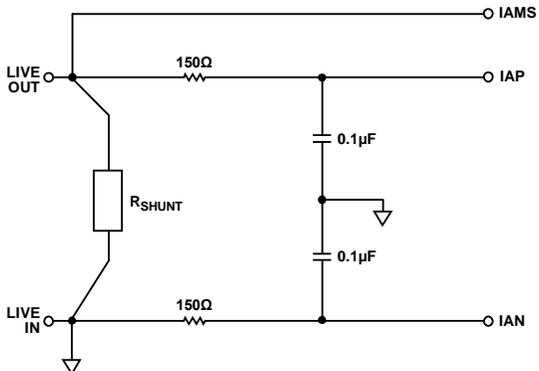
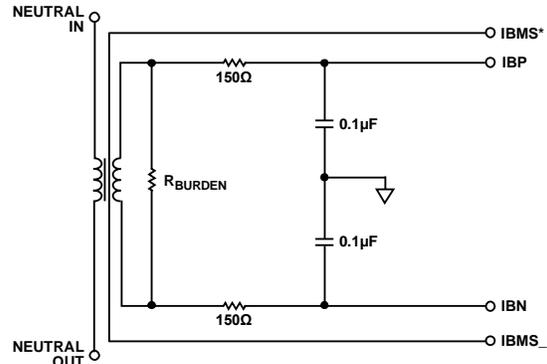


Figure 13. Phase Current Channel Antialias Schematic



*IBMS and IBMS_BACK CAN BE INTERCHANGED

Figure 14. Neutral Current Channel Antialias Schematic

CRYSTALS AND CAPACITORS

For optimal performance of the *m*Sure autocalibration, consider the parameters for crystal selection and antialiasing capacitors selection provided in the Crystal section and the Antialiasing Capacitors section.

Crystal

Select the crystal according to the following specifications:

- Operating temperature: -40°C to $+85^{\circ}\text{C}$
- Frequency tolerance: $\leq \pm 50$ ppm
- Frequency stability: $\leq \pm 30$ ppm

To protect the CLKIN pin and CLKOUT pin from noise and disturbances, avoid long connections from the load capacitors and the CLKIN pin and CLKOUT pin because these connections can create large loops in the crystal layout.

Keep the load capacitor for the CLKIN pin as close to the pin as possible. Keep the load capacitor for the CLKOUT pin close to the pin, but the distance can be greater than the distance between the CLKIN load capacitor and the CLKIN pin.

Avoid long connections from the load capacitors that create large loops in the crystal layout. This configuration protects the CLKIN pin and CLKOUT pin from noise and disturbances.

To prevent the coupling of the fast signals of the clock to the signal traces, do not route signal traces near the crystal layout.

Refer to the [ADE9153A Technical Reference Manual](#) for more details on calculating the values of the load capacitors and selecting the crystal.

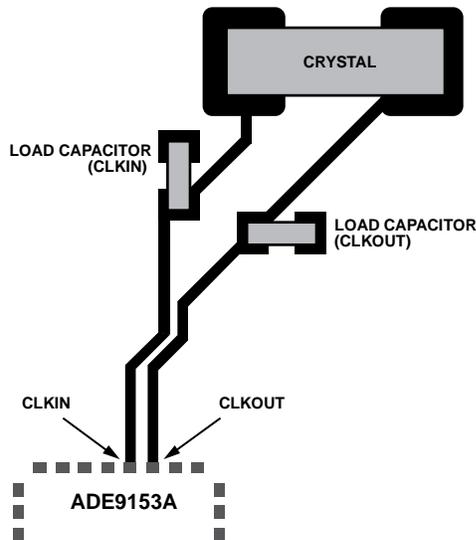


Figure 15. Recommended Layout for Crystal and Load Capacitors

Antialiasing Capacitors

Use the C0G (NP0) antialiasing capacitor at the inputs of the phase current channel, the neutral current channel, and the voltage channel.

Decoupling Capacitors

The recommended capacitance values for the decoupling capacitors are 4.7 μF and a 0.1 μF . When positioning these capacitors, ensure that the 0.1 μF capacitors are the closest capacitors to the chip and that the connections between the capacitors and the device pins are as short as possible (see Figure 16).

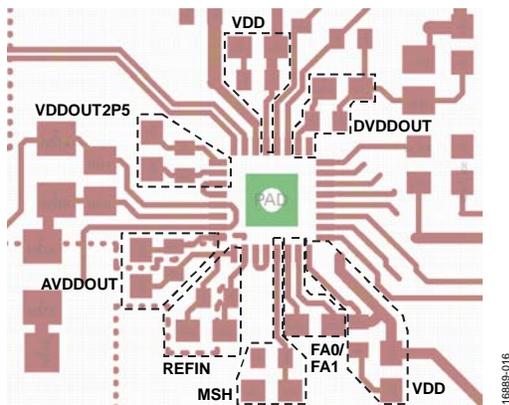


Figure 16. Layout of Capacitors on the ADE9153A

Connect the AGND pin and the DGND pin to the GND plane on the top layer of the PCB. Place a via close to these pins to connect the pins to the GND plane on the bottom layer of the PCB.

The REFIN and AVDDOUT decoupling capacitors connect to the AGND pin (Pin 17) through GND, as shown in the Figure 17. A via to the GND plane on the bottom layer of the PCB near the AGND pin improves the routing of the grounds in this area.

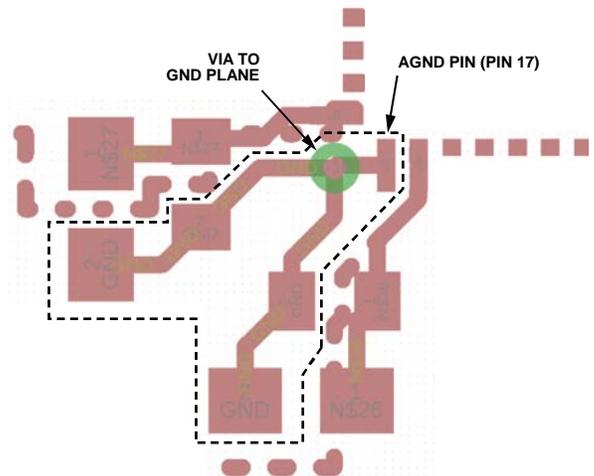


Figure 17. REFIN and AVDDOUT Ground Decoupling Capacitors Connection

POWER SUPPLY

The EV-ADE9153ASHIELDZ uses the ADuM6000 isolated dc-to-dc converter to power up the ADE9153A.

This board has an isolated power supply. However, the power supply of the system for the ADE9153A can be isolated or nonisolated. Selecting which power supply to use depends on the type of application and design of the system.

Connections Using an Isolated Power Supply

The power supply input for the meter requires a connection to both the live in terminal and the neutral terminal. When using an isolated power supply, ground the transformer input to the live in terminal, which is connected to the current shunt. Only connect the transformer input to the live in terminal through the current shunt, not to the GND plane. Ensure that the only meeting point of the GND plane and the transformer input is the live in terminal.

Connect a metal oxide varistor (MOV) across and near the live in terminal and the neutral terminal. This MOV protects the power supply and the potential divider, the only parts of the device affected by the high voltage that can cause high current flowing in the phase line and neutral line. When pulling the neutral terminal, the traces must not disrupt the GND plane beneath the IAMS trace and IBMS trace. The ground of the power supply output must be connected to the GND plane. Figure 18 shows the suggested power supply connection.

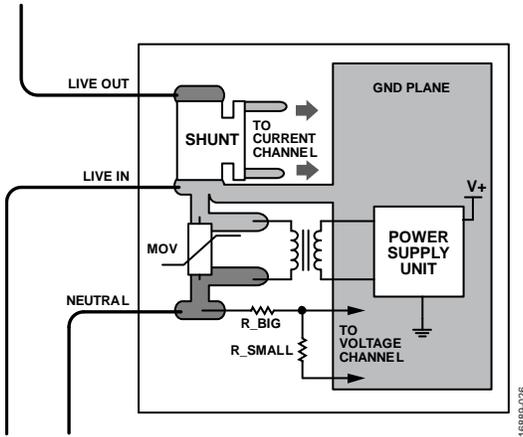


Figure 18. Isolated Power Supply Ground Connection

Connections Using a Nonisolated Power Supply

When using a nonisolated power supply, connect the live in terminal through the current shunt to an MOV. Connect the other terminal of the MOV to both the neutral terminal and a positive temperature coefficient (PTC) thermistor that connects to the power supply. In the event of an error, the MOV protects the device from a sudden increase in current of the power supply. Figure 19 shows a nonisolated power supply connection.

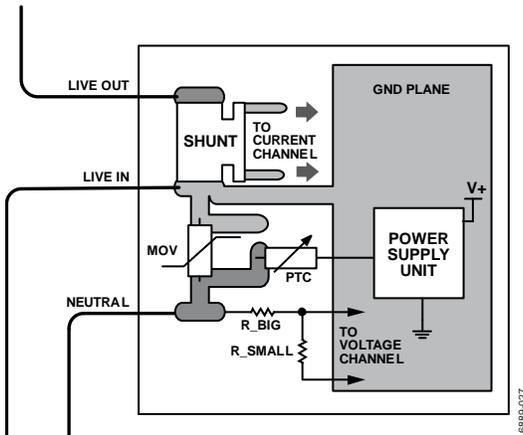


Figure 19. Nonisolated Power Supply Connection

GROUNDING AND ISOLATION

The ground of the [ADE9153A](#) and the ground of the micro-controller must be isolated properly. Consider the position of the device, sensors, power supply, and other components of the device when configuring the layout for the primary ground. This section uses the ground layout of the [EV-ADE9153ASHIELDZ](#) to explain the division of the ground into primary and secondary grounds (see Figure 20).

Ground Planes

The ground must be designed properly to minimize noise coming from the internal and external sources. Incorrect ground design causes noise to enter the device and affect the performance and functionality of the analog circuitry and the *m*Sure channels. It is recommended to have a GND plane on both the top and bottom layers of the PCB.

The left side of Figure 20 describes the layout of the GND plane on the bottom layer.

The secondary ground plane (SGND) is where the controller is grounded and is completely isolated from all of the ground of the [ADE9153A](#) and from live in.

The antialias filter, current shunt, and potential divider (upper) do not disrupt the GND plane. See the Power Supply section for details on the power supply.

Primary Ground Plane

Follow these guidelines when constructing the primary ground plane:

- Tie the AGND pins and DGND pins of the [ADE9153A](#) with the lowest impedance connection possible through the GND plane.
- Connect the live in to the GND plane on the top layer through the current shunt.
- The analog grounds terminate in the GND plane. (The GND plane also provides the ground reference for the digital circuitry in the [ADE9153A](#).)
- Connect the DGND pins to the GND plane on the top layer. The decoupling capacitors, crystal oscillators, power supply output ground, and many of the other support components for the [ADE9153A](#) are grounded in the GND plane.

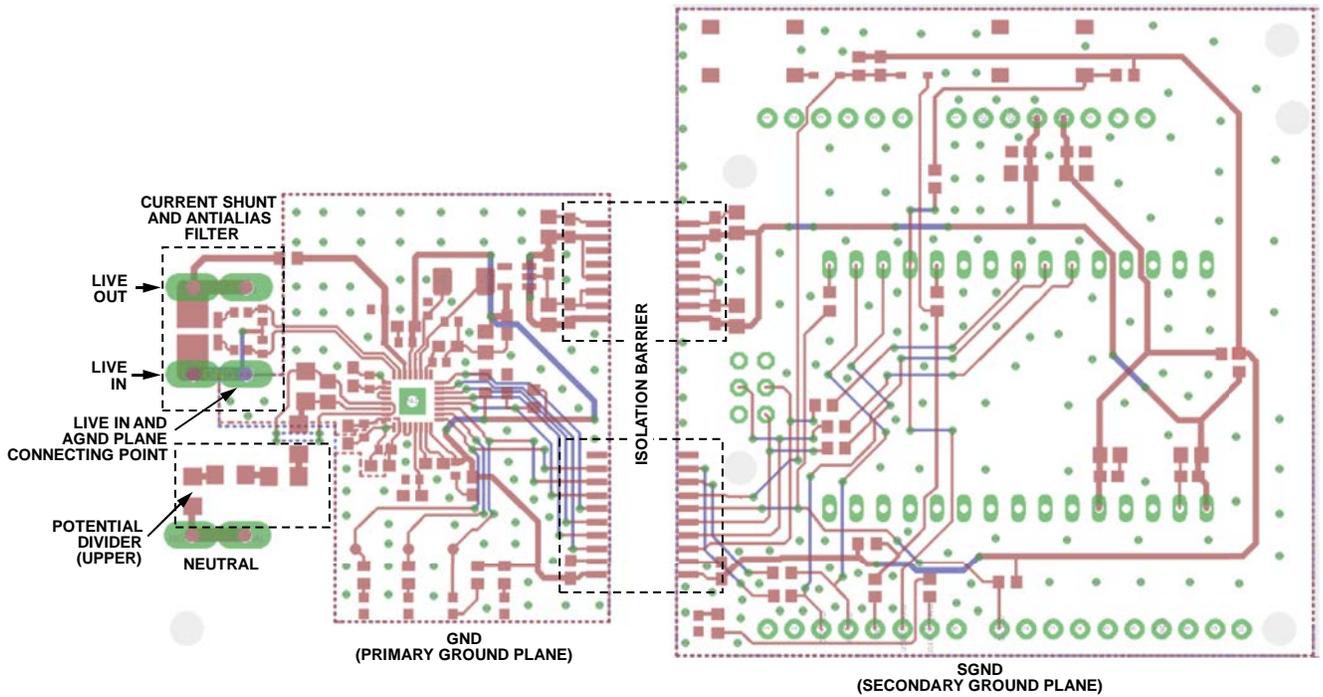
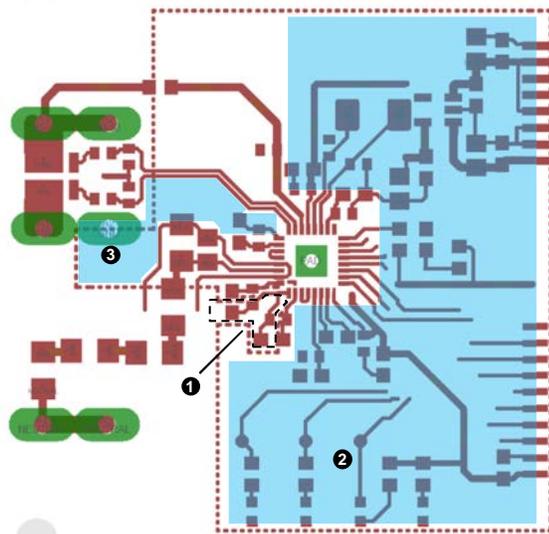


Figure 20. EV-ADE9153ASHIELDZ PCB

16889-020



- NOTES
1. REFIN AND AVDD GROUND TO GND PLANE.
 2. GND PLANE SURROUNDING THE TOP LAYER.
 3. GND PLANE CONNECTED TO LIVE IN.

Figure 21. GND Plane (Top Layer)

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Figure 21 shows a typical ground plane connection for the ADE9153A. Label 2 indicates the GND plane. The ground for REFIN and AVDDOUT goes directly to the AGND pin and does not form a plane (see the Crystals and Capacitors section).

Vias connect the ground planes on the top and bottom layers of the PCB (see Figure 22). The DGND pins and AGND pins must be connected to the GND planes on the top and bottom layers through vias located near the pins.

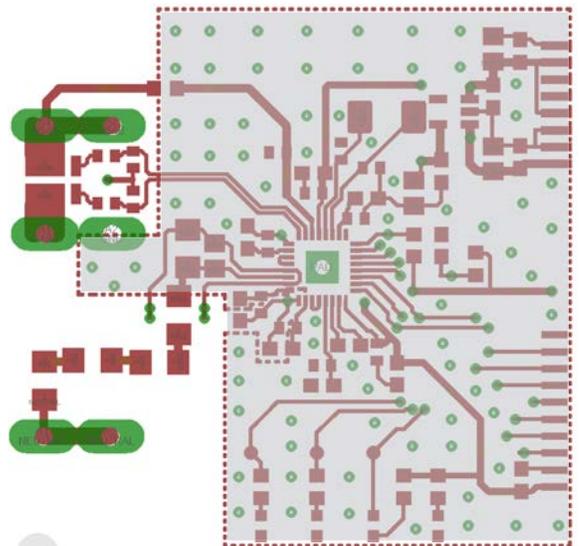


Figure 22. GND Plane (Bottom Layer) with Vias

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The GND plane is located under the VAN and VAMS guard as shown in Figure 23. This GND plane guards the lower resistance of the potential divider and antialias filter of the voltage channel. No GND plane is located under the upper high voltage side of the potential divider.

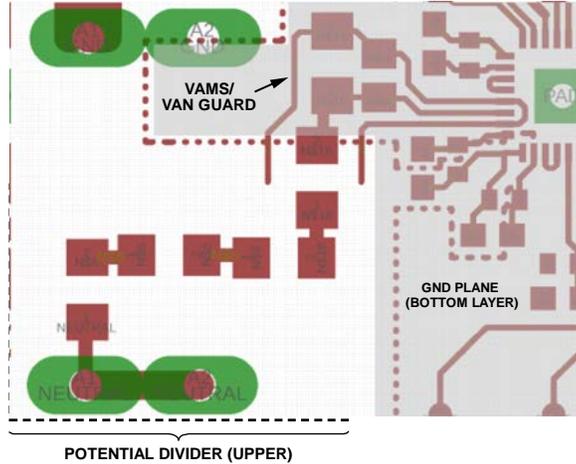


Figure 23. GND Plane Under VAMS and VAN Guard

Isolation

Adding energy measurement to system level applications requires an isolation barrier to separate the voltages and the grounding of the energy measurement circuitry from the controller.

The ADE9153A is floating at the mains voltage. As such, isolation in the application is necessary for safety. One common location for isolation is between the ADE9153A and the microcontroller unit (MCU). Alternatively, the isolation can be placed between the MCU and communication.

The isolation barrier must contain isolators or an IC with power supply isolation and data isolation channels to separate the high voltage side that contains the energy measurement system from the safe side that contains the controller or processor of the system (see Figure 24). On the EV-ADE9153ASHIELDZ, the ADUM6000ARIZ provides isolated power and the ADUM4152BRIZ SPI Isolator® isolates the serial peripheral interface (SPI) and low speed digital interface signals.

When selecting an isolation device, consider critical requirements such as data rate, space requirements, and voltage requirements.

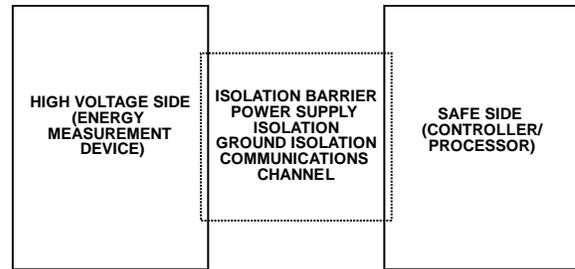


Figure 24. Isolation Barrier of EV-ADE9153ASHIELDZ

APPLICATION EXAMPLES

SMART STREET LIGHTING

Smart street lighting integrates revenue grade energy metering into a system designed for energy efficiency with automatic switch control, dimming control, and fault alarms. A special feature of smart street lighting is remote maintenance and development, for which the autocalibration technology of the [ADE9153A](#) is suited.

In utility metering, the consumption of the power supply for the meter is not billed to the customer and, therefore, the power supply for the meter is attached before the shunt resistor. In some applications, such as certain street lighting applications, there are configurations where it is desirable to measure the power consumption of the entire load, including the measurement module. In this case, the power supply is connected after the shunt resistor. The modulation in power

consumption going through the shunt sensor required for *mSure* can cause errors in the *mSure* results that vary with the power supply design. These errors are specific to power supply design and must be measured on each complete system. These errors can be on the order of a few tenths of a percent. Follow the standard recommendation to connect the power supply for the module before the shunt resistor.

ENERGY MEASUREMENT ON MULTIPLE OUTPUTS

Power distribution units (PDUs) in data centers have multiple single phase receptacles for distributing electric energy. Use the [ADE9153A](#) to monitor the energy consumed by one receptacle. Figure 26 shows a basic illustration of several [ADE9153A](#) devices in a PDU application.

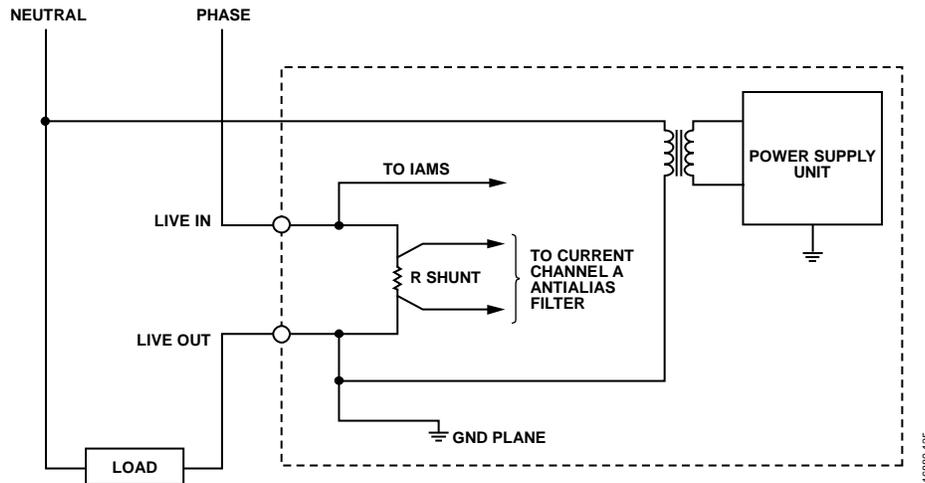


Figure 25. Power Supply Connection After the Shunt Resistor

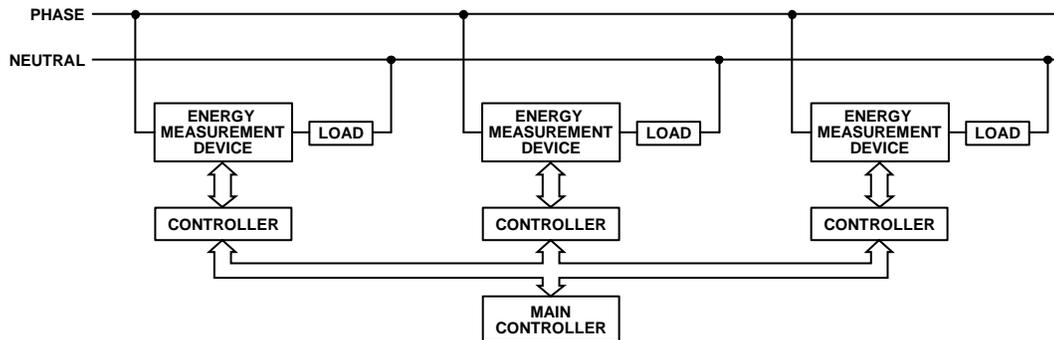


Figure 26. Energy Measurement on Multiple Outputs

CONCLUSION

The guidelines and recommendations in this application note are critical when adding the [ADE9153A](#) as an energy measurement device to a system.

A short summary of these recommendations follows:

- The layout for the SMD current channel must consist of the *mSure* in and *mSure* return for the IAMS injection. Ensure to place a capacitor across the IAMS and ground for immunity to electric fast transients.
- Most applications do not require neutral current measurements. In this case, the IBP pin and IPN pin must be shorted together and the IBMS pin and DGND pin must be shorted together. When using a current transformer to measure the neutral current channel, an extra wire is required for IBMS injection.
- The VAP trace for the potential divider must be surrounded by the VAMS and VAN guard. Follow the recommended layout and copper trace requirements.
- The antialias filters must be symmetrical and are located near the sensors with parallel traces feeding into the pins of the [ADE9153A](#).
- The crystal must have a frequency tolerance of $\leq \pm 50$ ppm and a frequency of stability of $\leq \pm 30$ ppm. Keep the load capacitors of the crystals close to the pins.
- The system can use the power source from the controller part or a separate power supply for the [ADE9153A](#). Follow the recommended layout.
- All of the grounds of the device must meet at the ground plane. Ensure that the high voltage side and the safe side of the system are isolated.