ANALOG DEVICES

AN-1445
APPLICATION NOTE

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Upgrading from the ADF4355 to the ADF4356

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INTRODUCTION

The ADF4356 is the improved, next generation of the ADF4355. Benefits of switching to the ADF4356 include the following:

- 4 dB improvement in both integer-N and fractional-N normalized phase noise floors figures of merit (FOMs)
- 5 dB improvement in 1/f flicker noise
- 5 dB to 10 dB improvement in spurs

This user guide details the hardware and software changes required.

HARDWARE INSTALLATION

1. Remove the ADF4355BCPZ.
2. Install the ADF4356BCPZ.
3. Optional: remove R_{SET} resistor (connected to Pin 22). The ADF4356 R_{SET} can be left connected to NIC, Pin 22.

WRITE SEQUENCES

The ADF4356 initialization sequence and the frequency update sequence are similar to the ADF4355 initialization sequence, with the addition of Register 13 to the ADF4356. See the ADF4356 data sheet for full details.

REGISTERS

Table 1 and Table 2 list the differences in the register writes between the ADF4355 and the ADF4356. Refer to the ADF4355 and the ADF4356 data sheets for full details.

Table 1. ADF4355 Register Values for $RF_{OUT}A\pm/RF_{OUT}B\pm$ = 5 GHz

Register(s)	Contents	Bit No.	Bit Description Changes
0 to 5	Not applicable	Not applicable	No changes to these bits.
6	0x350180F6	DB31 DB25	Reserved bit, set to 0. Reserved bit, set to 0.
7	0x120000E7	DB28 DB27 DB26	Reserved bit, set to 1. Reserved bit, set to 0. Reserved bit, set to 0.
8	0x102D0428	Not applicable	Not applicable.
9	0x1A19FCC9	Not applicable	VCO band division (Bits[DB31:DB24]) = ceiling (f_{PFD}/2,400,000), where ceiling rounds up to the nearest integer.
10	Not applicable	Not applicable	No changes to these bits.
11	0x0061300B	DB24 DB12	Reserved bit, set to 0. Reserved bit, set to 1.
12	0x0001041C	[DB31:DB16] [DB15:DB11] [DB9:DB5]	Resync clock bits. Reserved bits, set to 0. Reserved bits, set to 0.
13	Does not exist	Not applicable	Not applicable.

Table 2. ADF4356 Register Values for $RF_{OUT}A\pm/RF_{OUT}B\pm$ = 5 GHz

Register(s)	Contents	Bit No.	Bit Description Changes
0 to 5	Not applicable	Not applicable	No changes to these bits.
6	0x350300F6	DB31 DB25	Bleed polarity bit. For the ADF4356 new bleed current rule, see the ADF4356 data sheet. RF Output B select.
7	0x060000E7	DB28 DB27 DB26	Reserved bit, set to 0. LE SEL sync edge bit. Reserved bit, set to 1.
8	0x15596568	Not applicable	New default reserved value.

Register(s)	Contents	Bit No.	Description
9	0x2719FCC9	Not applicable	VCO band division (Bits[DB31:DB24]) = ceiling (f_{PFD}/1,600,000).
10	Not applicable	Not applicable	No changes to these bits.
11	0x0061200B	DB24 DB12	VCO band hold bit. Reserved bit, set to 0.
12	0x000015FC	[DB31:DB12] DB10 [DB8:DB5]	Phase resync clock value bits. Reserved bit, set to 1. Reserved bits, set to 1.
13	Exists	Not applicable	Added MSB registers for FRAC2 and MOD2 values. See the ADF4356 data sheet.