

One-Stage Amplifier Design Consideration of a High Fidelity System

by Roy He

INTRODUCTION

With an increasing demand of built in, high fidelity systems for portable devices, for example, mobile phones and active headphones, amplifiers for larger driving power are widely implemented into high fidelity systems.

As part of a high fidelity system, the output amplifier is a critical element for both objective and subjective performances of the whole audio performance by providing ample output power toward its load, the headphones. Analog Devices, Inc., offers a wide range of low noise, high performance amplifiers for such applications, like the [ADA4841-2](#), [ADA4896-2](#), [ADA4075-2](#), [AD8599](#), [AD8610](#), [AD8397](#), and [ADA4807-2](#). These amplifiers are widely used in a high fidelity related system circuit design.

Because there are various methods for high fidelity system design, each scenario cannot be described in this application note. This application note discusses the one-stage amplifier structure, which is low cost, easy to design, and widely used by mobile phone companies.

ONE-STAGE SIMPLE AMPLIFIER HIGH FIDELITY DESIGN

For better understanding of the high fidelity system structure as a whole, the amplifier design is discussed in this section.

The amplifier block in Figure 2 shows there are different kinds of circuit designs based on the general audio amplifier that amplify, filter, buffer, and signal condition. When compared with a two-stage or three-stage amplifier design, a one-stage design method solution provides less components in the design, such as lower cost and a simplified printed circuit board (PCB) layout, while still providing excellent audio performance.

Therefore, one-stage design method is more suitable for scenarios that require high performance to price ratio products, such as mobile phones.

Figure 2 shows the typical connection diagram of a high fidelity system.

A high fidelity design is a system level design where each device has its own functions and performs together as a whole. The typical desired specification of codec or digital-to-analog converter (DAC) in portable devices is usually indicated as follows:

- Voltage swing up to 2 V rms.
- R_{OUT} is low enough to achieve optimal performance and to be ignored, which helps attain better damping coefficient and output amplitude levels.
- Differential voltage output.

The simple and low cost typical circuit is shown in Figure 1.

In Figure 1, V_{AC} is the audio signal and V_{DC} is the internal bias from the audio DAC.

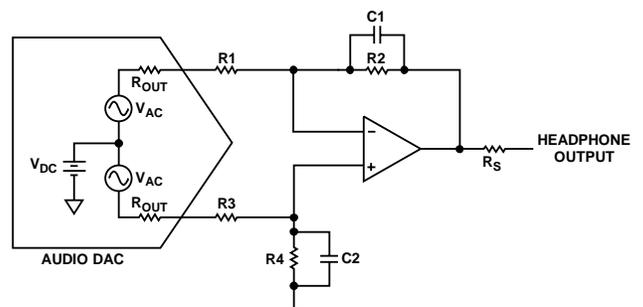


Figure 1. Diagram of Typical One-Stage Simple Amplifier Structure

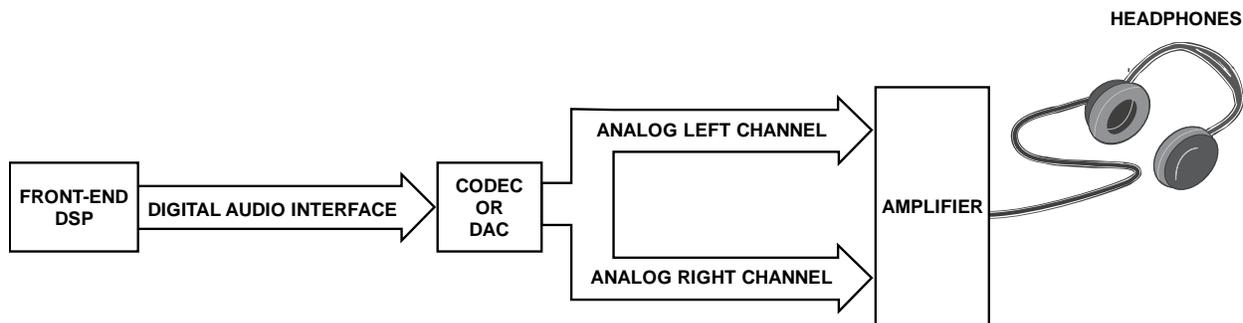


Figure 2. Typical Connection Diagram of a High Fidelity System

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REVISION HISTORY

12/2016—Revision 0: Initial Version

CALCULATION GUIDANCE AND DESIGN PARAMETERS

CALCULATION

The standard testing method of a high fidelity audio system performance includes subjective and objective tests.

In a subjective hearing test, the performance is due to the standard subjective hearing style of a human in regards to how they feel while music is played, which is not easy to calculate.

The audio DAC setting and the circuit design component values can be tuned based on the various expected hearing styles. The focus of this application note is only on how to improve objective performance by tuning circuit design at the hardware level.

Among plenty of test items, total harmonic distortion plus noise (THD plus N) are important factors for objective performance tests.

Typically, for small signal levels, N is the dominant factor, which is deduced in the following calculations based on the indicated circuit in Figure 2. The capacitor has little effect on the formula, which is why the capacitor effect is ignored.

Assume the following statements:

- E_N and I_N are the voltage and current noise spectral density of the one-stage amplifier shown in Figure 1.
- Frequency cutoff (f_c) is the system bandwidth.

To make the circuit more symmetrical, select the resistor values as

$$R_1 = R_3, R_2 = R_4$$

$$R_{P1} = R_1 \parallel R_2$$

$$R_{P2} = R_3 \parallel R_4$$

Then,

$$RTI_{NOISE}(f) \approx \sqrt{4KTR_{P1} + 4KTR_{P2} + E_N^2 + I_N^2 \times (R_{P1}^2 + R_{P2}^2)} \quad (1)$$

where:

RTI_{NOISE} is the referred to input noise, in $V/\sqrt{\text{Hz}}$.

K is the Boltzmann's constant, $= 1.3806505(24) \times 10^{-23}$ J/K.

T is the temperature.

R_{P1} and R_{P2} are the parallel resistor values.

E_N is the voltage noise spectral density.

I_N is the current noise spectral density.

$$RTO_{NOISE}(f) = RTI_{NOISE} \times \left(1 + \frac{R2}{R1}\right) \quad (2)$$

where:

RTO_{NOISE} is the referred to output noise, in $V/\sqrt{\text{Hz}}$.

$R2$ is the feedback resistor, shown in Figure 1.

$R1$ is the series input resistor, shown in Figure 1.

$$RTO_{RMS} =$$

$$\frac{1}{2\pi} \int_0^{f_c} RTO_{NOISE}(f) \approx RTO_{NOISE} \times \sqrt{1.57 \times f_c} \quad (3)$$

where:

RTO_{RMS} is the rms value of the referred to output noise.

f is the frequency.

$$THD + N = 20 \log \frac{RTO_{NOISE} + THD}{V_{IN} \times \left(\frac{R2}{R1}\right)} \quad (4)$$

where V_{IN} is the input voltage.

See Equation 5 to calculate $THD + N$.

$$THD + N \text{ (dB)} \approx 20 \log \frac{\sqrt{4KTR_{P1} + 4KTR_{P2} + E_N^2 + I_N^2 \times (R2_{P1} + R2_{P2})} \times \left(1 + \frac{R2}{R1}\right) \times \sqrt{1.57 \times f_c} + THD}{V_{IN} \times \left(\frac{R2}{R1}\right)} \quad (5)$$

DESIGN CONSIDERATION

For a small signal level scenario, THD is small enough to be ignored because it is almost equal to zero, which has no effect on the system due to the electrical characteristics of an integrated circuit (IC) design. Thus, noise is the dominant factor affecting the THD + N results under such small signal level situations.

Taking the [ADA4807-2](#) as an example, the approximate noise performance within a 22 kHz bandwidth is calculated if $R1 = R3 = 1\text{ k}\Omega$ and $R2 = R4 = 1\text{ k}\Omega$. Figure 3 shows the calculated result using the mathematic tool, wxMaxima.

The noise result is improved when using test equipment like the SYS-2712 or the APx555 to analyze audio in dBA because the equipment adds an A weighted filter to reduce noise, which simulates the response to sound of the human ear.

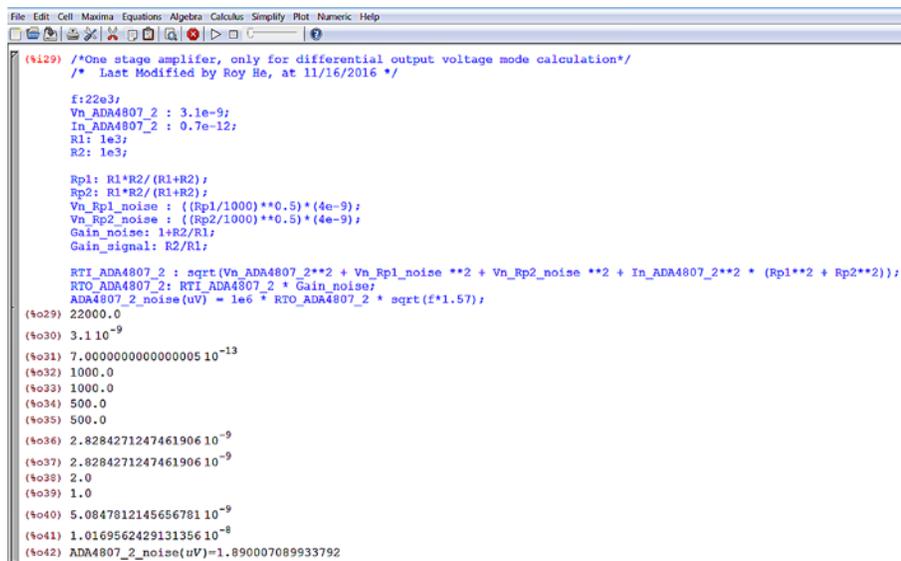
To improve performance, power, noise, and electromagnetic interference (EMI) must be taken into design consideration as well. Audio performance is sensitive and easily affected by WiFi or radio frequency (RF) environments; therefore, good shielding and layout are required.

Usually, THD is much more serious if the desired load power exceeds the limit for output of any amplifier, which means, unlike in light load conditions, THD must be carefully considered, especially in heavy load scenarios.

Therefore, voltage and current noise, bandwidth, resistors, output capability, and gain setting affects objective test results at the hardware level.

As a result, users can choose and judge related parameters, as shown in Figure 1 and Figure 3.

Moreover, other parameters, like slew rates, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR), and voltage swing, are system factors that must be taken into consideration during audio system design.



```

(*i29) /*One stage amplifier, only for differential output voltage mode calculation*/
/* Last Modified by Roy He, at 11/16/2016 */

f:22e3;
Vn_ADA4807_2 : 3.1e-9;
In_ADA4807_2 : 0.7e-12;
R1: 1e3;
R2: 1e3;

Rp1: R1*R2/(R1+R2);
Rp2: R1*R2/(R1+R2);
Vn_Rp1_noise : ((Rp1/1000)**0.5)*(4e-9);
Vn_Rp2_noise : ((Rp2/1000)**0.5)*(4e-9);
Gain_noise: 1+R2/R1;
Gain_signal: R2/R1;

RTI_ADA4807_2 : sqrt(Vn_ADA4807_2**2 + Vn_Rp1_noise **2 + Vn_Rp2_noise **2 + In_ADA4807_2**2 * (Rp1**2 + Rp2**2));
RTO_ADA4807_2: RTI_ADA4807_2 * Gain_noise;
ADA4807_2_noise(uV) = 1e6 * RTO_ADA4807_2 * sqrt(f*1.57);

(*o29) 22000.0
(*o30) 3.110^-9
(*o31) 7.0000000000000005 10^-13
(*o32) 1000.0
(*o33) 1000.0
(*o34) 500.0
(*o35) 500.0
(*o36) 2.8284271247461906 10^-9
(*o37) 2.8284271247461906 10^-9
(*o38) 2.0
(*o39) 1.0
(*o40) 5.0847812145656781 10^-9
(*o41) 1.0169562429131356 10^-8
(*o42) ADA4807_2_noise(uV)=1.890007089933792

```

Figure 3. Calculating Results of the [ADA4807-2](#) with wxMaxima

15221-003

DEBUGGING METHODS AND ANALYSIS SHIELDING

A shielding case to cover a high fidelity audio circuit is highly recommended. Layout must be carefully treated to avoid possible interference from other parts of the whole circuit system. The layout is critical because the audio performance is related to signal integrity and electrical environment, for instance, strong interference appears around dc to dc parts or a RF power amplifier. Proper layout, including trace routing and PCB stackup, is expected to help avoid noise and distortion.

OUTPUT SERIES RESISTOR

An output series resistor, shown as R_S in Figure 2, is recommended for the following reasons:

- Guarantees the stability of the amplifier and covers varieties of headphone loads.
- Prevents the output power from exceeding the limit of the amplifier.
- Tunes for output signal amplitude, as well as subjective hearing.

BANDWIDTH SETTING

Theoretically, a narrower bandwidth results in lower noise while limiting the flatness of frequency response, thus requiring a trade-off point. Typically, the best cutoff area range is from 60 kHz to 200 kHz.

NOISE PERFORMANCE

From an analog design perspective, a larger gain results in larger noise; therefore, for a one-stage amplifier, minimal gain must be set to meet the output requirements. Either poor power or EMI design can result in noise spurs at certain areas, as shown in Figure 4.

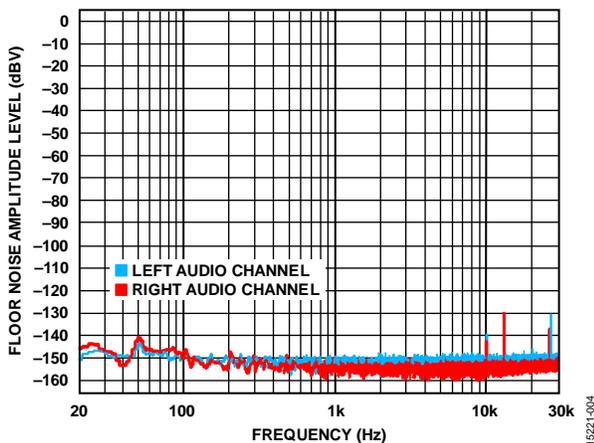


Figure 4. Floor Noise Amplitude Level vs. Frequency

GAIN CONFIGURATION

To achieve lower noise generated by the amplifier, calculate the proper gain setting with a resistor value. Taking the circuit shown in Figure 1 as an example, assume the load is R_L , V_L is the voltage load, and I_L (loads not shown in Figure 1) is the current load, therefore

$$V_L = \frac{V_{DAC} \times Gain \times R_L}{R_S + R_L} \tag{6}$$

where:

V_{DAC} is the voltage output from the DAC.

R_S is the output series resistance, shown in Figure 1.

R_L is the load resistance.

$$I_L = \frac{V_{DAC} \times Gain}{R_S + R_L} \tag{7}$$

For given R_L and V_{DAC} values, and the required V_L and I_L values, calculate and set the optimal gain, as well as the desired f_c , with the proper capacitor value according to the design requirement.

CROSSTALK

Crosstalk indicates the isolation between audio channels. Impedance between different ground nets of each channel contributes to most of the crosstalk. The layout principle can achieve low impedance connection between ground networks. One thing worth noting is that different kinds of ear jacks result in different GND connection impedances, which matters in crosstalk performance because ear jacks with a lower impedance connection helps to achieve better performance.

DYNAMIC RANGE (DNR)

As discussed in the Calculation Guidance and Design Parameters section, for small signal, noise (N) is the dominant factor that affects THD + N results. DNR is tested with almost no THD, only the noise condition. There is almost no THD in Figure 5; therefore, N is the main factor that affects DNR results. A lower noise floor results in improved DNR.

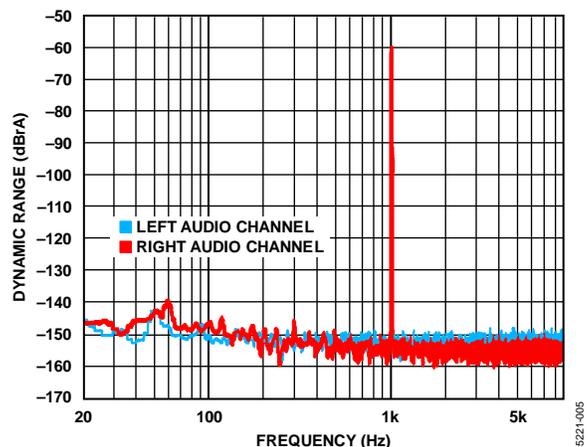


Figure 5. Dynamic Range vs. Frequency

FILTER DESIGN

Figure 1 shows a typical one-stage audio amplifier circuit design, using a simple first-order active filter, thereby achieving a limited filter effect.

Alternatively, the filter design can be refined with a second-order active filter design, such as a Butterworth, Chebyshev, Elliptic, or Bessel filter. Different types of filters hold different characteristics; therefore, a user must choose the specific filter type according to the specific requirement of the whole system. This section discusses the Bessel linear phase filter.

Amplifiers can easily result in phase drift, which means different signal frequencies lead to different time delays after passing through the amplifier, which is also known as group delay. Bessel filters can guarantee linear phase performance and achieve the same group delay towards different signal frequencies.

Figure 6 illustrates one example of a Bessel active filter schematic diagram. DAC_OUT+ and DAC_OUT- are the output signals from the DAC, which are also the positive and negative inputs of the Bessel filter.

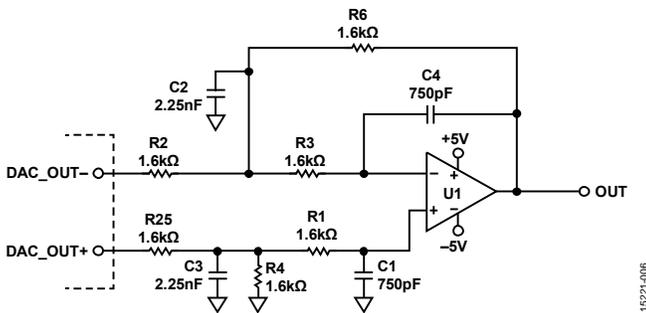


Figure 6. Schematic Diagram of a Bessel Active Filter

Figure 7 shows that the phase drift is in excellent linearity within the 20 Hz to 20 kHz, which is typically known as the human audible frequency range. The simulation of amplitude and phase vs. frequency results are shown in Figure 7.

Table 1 indicates the different phase drifts and linearity at various frequencies. The linearity curve is shown in Figure 8.

If the filter design, as shown in Figure 1, is changed to a second-order filter, the calculation of noise must change.

A one-stage amplifier high fidelity model requires system level design consideration, which includes headphone load, a DAC-compatible interface, audio power design, layout considerations, and system level tuning.

Table 1. Simulation Result of Filter Linearity

Parameter	Frequency (Hz)							Unit
	100	1000	5000	10,000	20,000	30,000	50,000	
Phase	0.130	1.298	6.492	12.984	25.947	38.794	63.245	Degrees
Linearity	1.299	1.298	1.298	1.298	1.297	1.293	1.265	m°/Hz

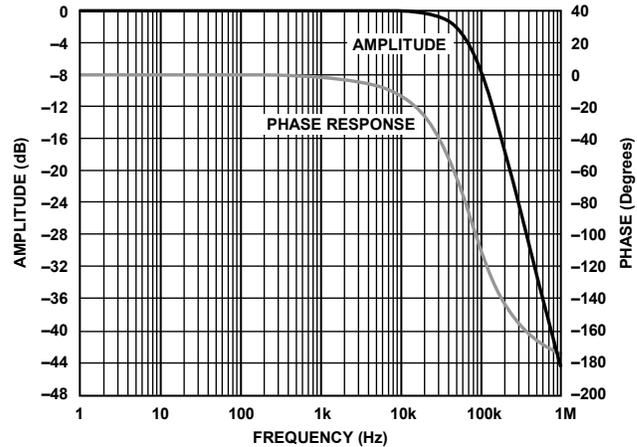


Figure 7. Amplitude and Phase vs. Frequency

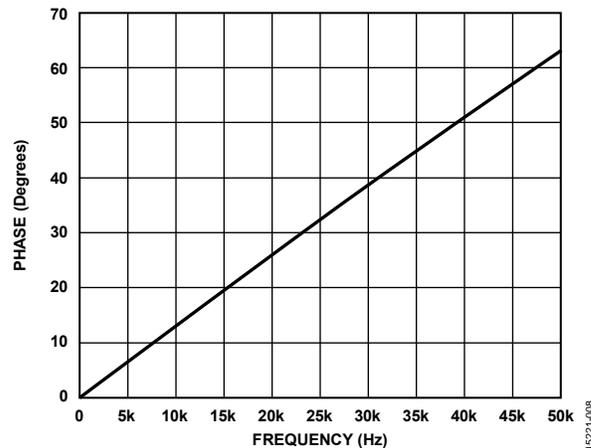


Figure 8. Phase vs. Frequency

For a more specific scenario design, compatibility of headphone parameters, such as frequency, impedance, sensitivity, cumulative spectral decay (CSD), and features, are also important for the entire audio system design. Audio designers can tune the analog components, like the amplifier, resistor, and capacitor, as well as the digital parameter setting like the digital filter and oversampling configuration, to achieve the final optimized performance.

To calculate the linearity listed in Table 1 and the slope shown in Figure 8, use the following equation:

$$\text{Linearity} = \text{Phase} \times 1000 \div \text{Frequency}$$