AN-1421
APPLICATION NOTE

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Paralleling the ADP1763 LDO Regulators for High Output Current Applications

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INTRODUCTION

Many high performance mixed-signal products, such as high speed analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), agile radio frequency (RF) transceivers, clocking, application specific integrated circuits (ASICs), and field programmable gate arrays (FPGAs) require ultralow noise, low dropout (LDO) linear regulators to provide clean supplies to maximize signal chain performance. With high demands of more integrated functionalities and lower power consumptions, those large scale mixed-signal integrated circuits (IC) feature a design with lower geometry process (for example, 28 nm or lower) to fit more transistors. This trend affects its power requirements as well. The core supply voltage keeps reducing, but with significantly increased load current (for example, >3 A), to adopt more analog or digital functionalities in recent years.

In particular applications, it is quite challenging to find an appropriate LDO regulator to meet the design target for both ultralow noise and high load current, because an LDO regulator may have very limited market availability or the user must pay a premium, if the device is even available. Therefore, sometimes it is beneficial to parallel LDO regulators for high current applications. Paralleling LDO regulators may provide many benefits over a single LDO regulator, including distributing the heat and power loss across multiple LDO regulator packages in high loads. Also, paralleling LDO regulators can improve dropout voltage and improve power supply rejection ratio (PSRR) performance because each LDO regulator operates in a lower current condition when compared to a single LDO regulator. Figure 1 shows a power diagram of high performance mixed-signal products. The two ADP1763 devices are paralleled to power the core voltage as shown in Figure 1.

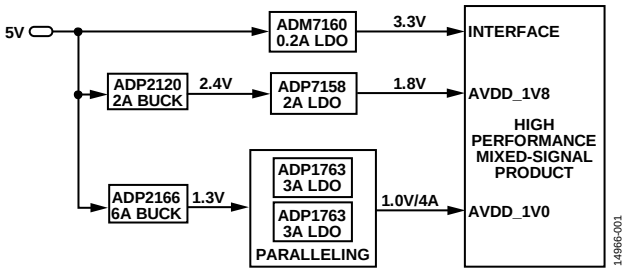

Figure 1. Power Diagram of Mixed-Signal Product

In this application note, two paralleling methods are introduced: passive and active. For passive paralleling, the two adjustable ADP1763 devices are paralleled together by the ballast resistors. For active paralleling, a low offset rail-to-rail amplifier, the ADA4051-1, adjusts the output voltage of the ADP1763 device to achieve current sharing by sensing the current difference between the two ADP1763 devices. The experimental test results show the advantages and disadvantages of the two methods.

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REVISION HISTORY

10/2016—Revision 0: Initial Version

CURRENT SHARING METHODS

Generally, the user cannot simply connect the two LDO regulators in parallel to achieve the current sharing because the output voltage between the LDO regulators can be mismatched due to tolerance errors; like different LDO reference voltages, mismatching feedback resistors, and mismatching printed circuit board (PCB) parasitics. The mismatching output voltage between LDO regulators can introduce significant load current unbalance. In the worst case, it can potentially cause one LDO to dominate most of the load so that it reaches the current-limit protection.

The ADP1763 is an LDO linear regulator that is designed to operate from a single input supply with an input voltage as low as 1.1 V without requiring an external bias supply and it provides up to 3 A of output current. The ADP1763 features 2 μV rms ultralow output noise from 100 Hz to 100 kHz. The ADP1763 ultralow output noise is achieved by keeping the LDO error amplifier in unity gain and setting the reference voltage qual to the output voltage. The advantage of unity-gain architecture is that the LDO output noise is independent with the output voltage setting. See Figure 2 for more details.

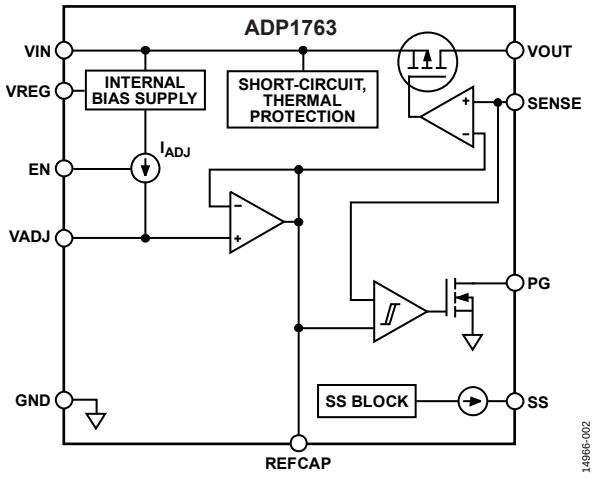

Figure 2. ADP1763 Internal Block Diagram

PASSIVE PARALLELING

A practical method for current sharing is to add identical ballast resistors (R_{B1} and R_{B2}) at the output of each regulator to improve the current sharing between multiple LDO regulators. To achieve better current sharing performance, large ballast resistance is preferred. However, the large ballast resistance degrades its load regulation and increases the dropout voltage. A careful design must consider the trade-off on the ballast resistance. Figure 3 shows two ADP1763 devices paralleled. To minimize the output errors, tie the REFCAP and the VADJ pins together to achieve the well matched voltage reference across different devices. Tie the SS and EN pins together to deliver the synchronized soft start behavior between the different devices. Tie the PG pins together if the application needs the power-good indicator feature.

When the REFCAP pins of the two ADP1763 devices connect together, the major output voltage errors come from the error amplifier offset voltage, which connects to an individual ADP1763 output. This error amplifier has a very low ±1.32 mV maximum offset voltage specification over the −40°C to +125°C temperature range. With only ±1.32 mV errors between the REFCAP pin and the VOUT pin, this offset voltage allows the use of small ballast resistors to achieve acceptable current sharing accuracy. In addition, the benefits of a small ballast resistor are low load regulation and low power loss.

To calculate the worst case, assume V_{O1} has the worst positive offset voltage, and V_{O2} has the worst negative offset voltage.

$$V_{O1} = V_{REFCAP} + V_{OFFSET}$$

$$V_{O2} = V_{REFCAP} - V_{OFFSET}$$

The total output current (I_O) = 5 A and $I_O = I_{O1} + I_{O2}$.

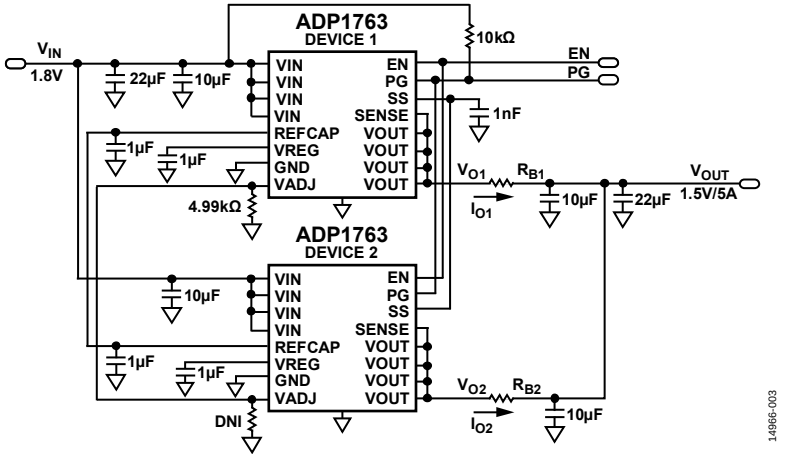

Figure 3. Passive Paralleling the Two ADP1763 Devices

The ballast resistor tolerance ($R_{S\text{-}TOL}$) is ±1%. To calculate the worst case, assume the ballast resistor on the V_{O1} voltage rail has a positive tolerance, and the V_{O2} voltage rail has a negative tolerance.

$$V_{O1} - I_{O1} \times R_B \times (1 - R_{S\text{-}TOL}) = V_{O2} - I_{O2} \times R_B \times (1 + R_{S\text{-}TOL})$$

When $R_{S\text{-}TOL}$ = 1%,

$$I_{O1} = \frac{I_O \times (1 + R_{S\text{-}TOL}) + \frac{V_{O1} - V_{O2}}{R_B}}{2}$$

$$I_{O2} = 5\ \text{A} - I_{O1}$$

$$CS_{ACCURACY} = \frac{I_{O2} - I_{O1}}{I_O} \times 100\%$$

where $CS_{ACCURACY}$ is the current sharing accuracy.

Figure 4 shows the relationship of current sharing accuracy and voltage droop vs. ballast resistance at a 5 A load. The current sharing accuracy improves with ballast resistance increasing. However, the penalty is a larger voltage droop. To achieve around 10% current sharing accuracy and minimal voltage droop, choose R_B = 5 mΩ.

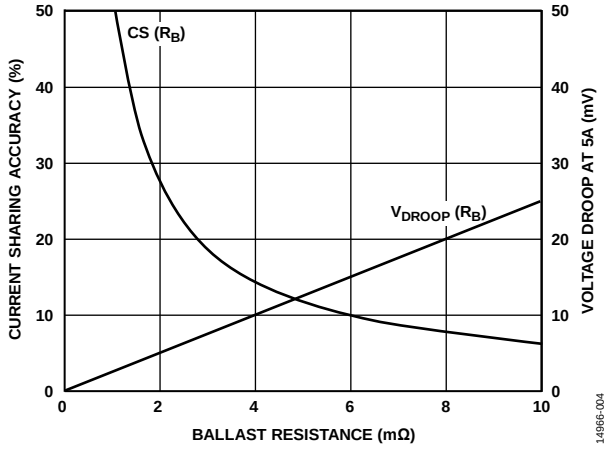

Figure 4. Current Sharing (CS) Accuracy and Voltage Droop vs. Ballast Resistance

Based on the calculation in Figure 4, the worst case current sharing accuracy is ±11.6% at a 5 A load. The maximum load current is 2.789 A, which is less than the 3 A rated current. Figure 5 shows the load regulation between the two channels using the passive current sharing method.

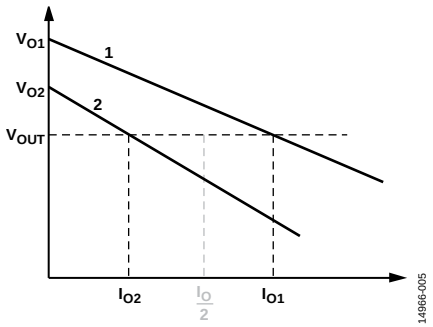

Figure 5. Passive Paralleling Load Regulation

ACTIVE PARALLELING

Compared with the passive current sharing method, the active current sharing method uses the active current sharing loop to achieve the current balance between the slave and the master LDO regulators. Figure 6 shows the active current sharing example for the two ADP1763 devices. It includes the two ADP1763 devices with the first ADP1763 as the master LDO, one output amplifier, the ADA4051-1, and two 10 mΩ current sensing resistors in the input of each LDO regulator. The amplifier, the ADA4051-1, senses the current difference and connects its output to the feedback node of the VADJ pin in the second ADP1763 device to adjust its output voltage to balance the current.

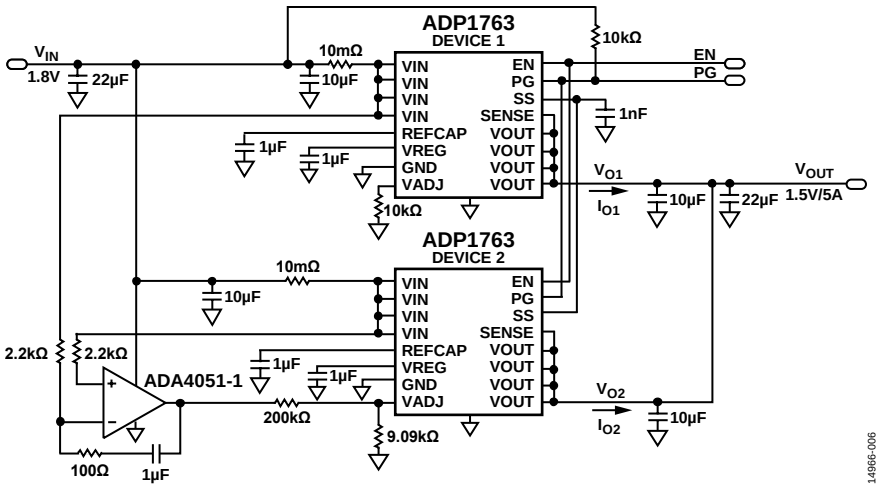

Figure 6. Active Paralleling the Two ADP1763 Devices

TEST RESULTS

To compare the two current sharing methods, the current sharing evaluation boards for the two ADP1763 devices are designed to verify the performance, as shown in Figure 7 and Figure 8.

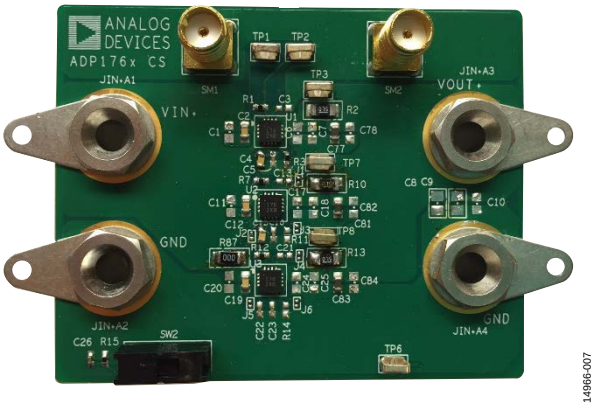

Figure 7. Passive Current Sharing Evaluation Board

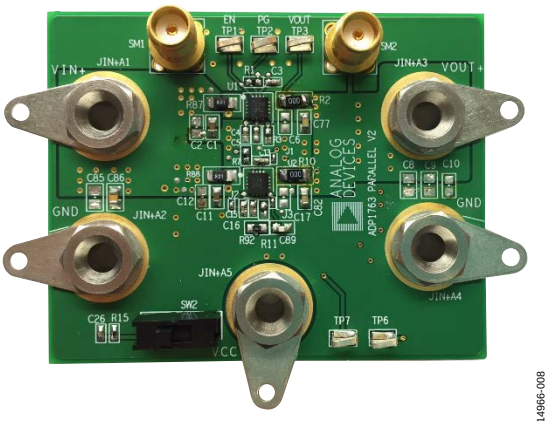

Figure 8. Active Current Sharing Evaulation Board

CURRENT SHARING ACCURACY

Figure 9 and Figure 10 depict the current sharing accuracy of the two evaluation boards. From the test results, the active current sharing accuracy is less than ±1% across a wide range of loads. The passive current sharing accuracy is about ±5% at full load, which is acceptable for most applications. The active current sharing method shows more improved current sharing results than the passive current sharing method, particularly at light load conditions due to the fixed offset error in the passive current sharing method.

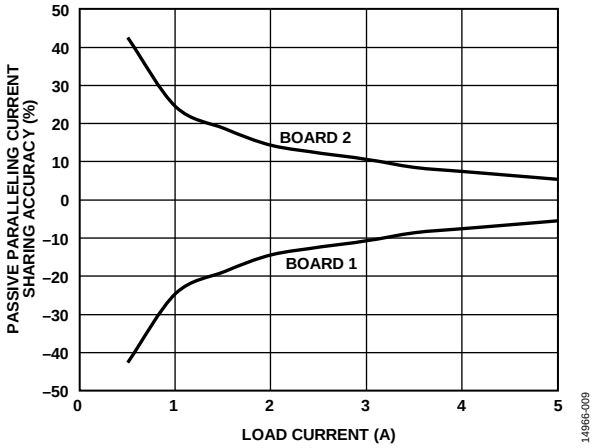

Figure 9. Passive Paralleling Current Sharing Accuracy vs. Load Current

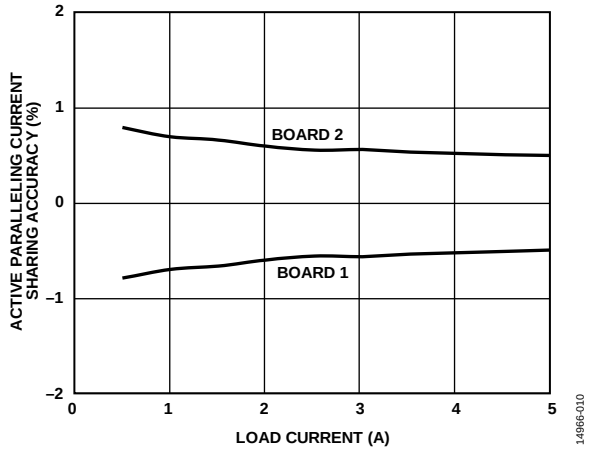

Figure 10. Active Paralleling Current Sharing Accuracy vs. Load Current

LOAD REGULATION

Because passive paralleling uses a ballast resistor at the output of each ADP1763, the output voltage droops with the load current increasing. From the test results shown in Figure 11, the load regulation of passive paralleling is about 1.3%, whereas Figure 12 shows the load regulation of active paralleling is about 0.5%, which is much lower than passive paralleling.

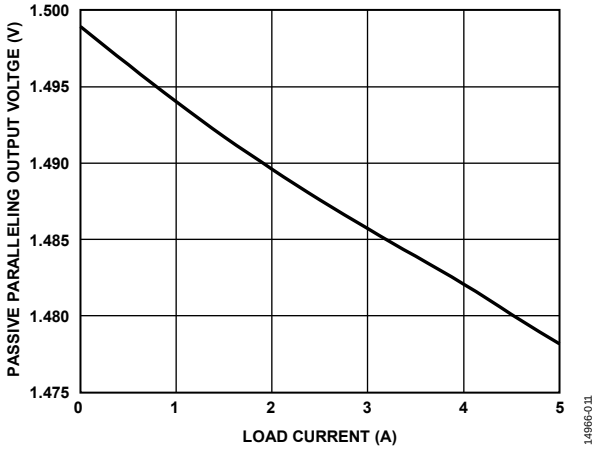

Figure 11. Passive Paralleling Output Voltage vs. Load Current

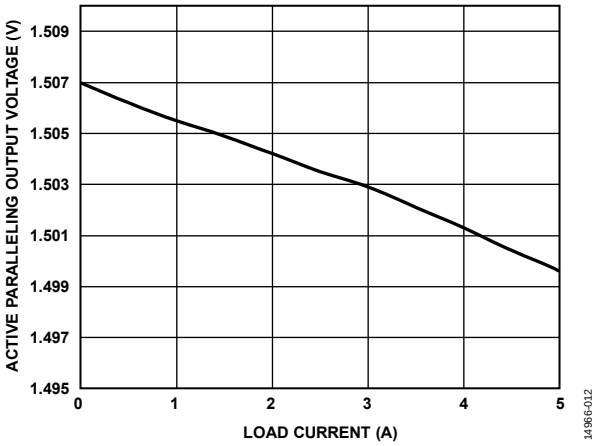

Figure 12. Active Paralleling Output Voltage vs. Load Current

SOFT START

Figure 13 and Figure 14 show the soft start waveform of passive and active paralleling at a full load condition. As shown in the waveforms of Figure 13 and Figure 14, the output voltage monotonic rises in either passive paralleling or active paralleling.

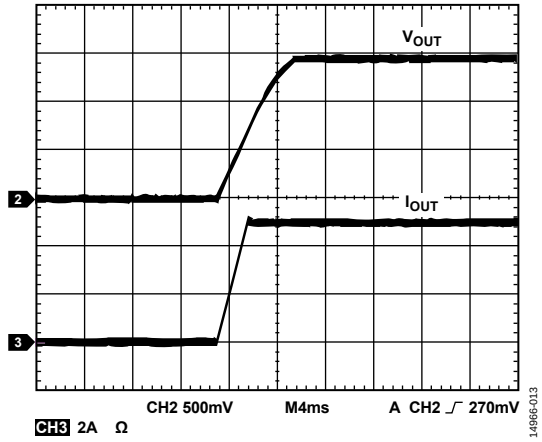

Figure 13. Soft Start of Passive Paralleling

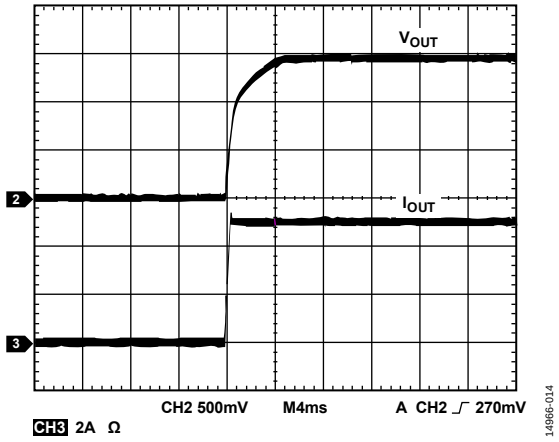

Figure 14. Soft Start of Active Paralleling

NOISE SPECTRAL DENSITY

Figure 15 and Figure 16 show the noise spectral density by passive paralleling and active paralleling, respectively, at a 5 A load. From the test results, the active paralleling and the passive paralleling noise spectral density performances are similar.

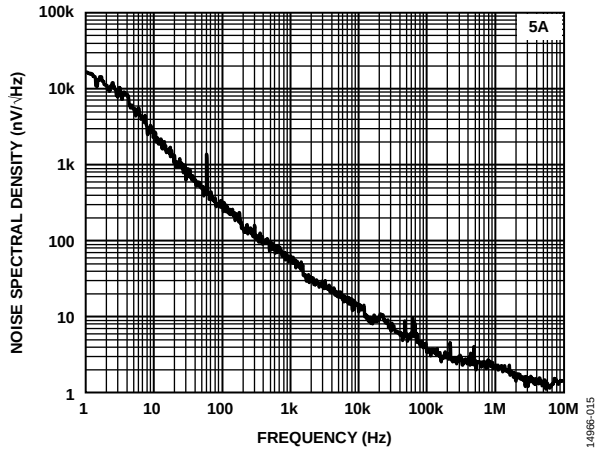

Figure 15. Noise Spectral Density (NSD) vs. Frequency at V_{IN} = 1.8 V, I_O = 5 A NSD of Passive Paralleling

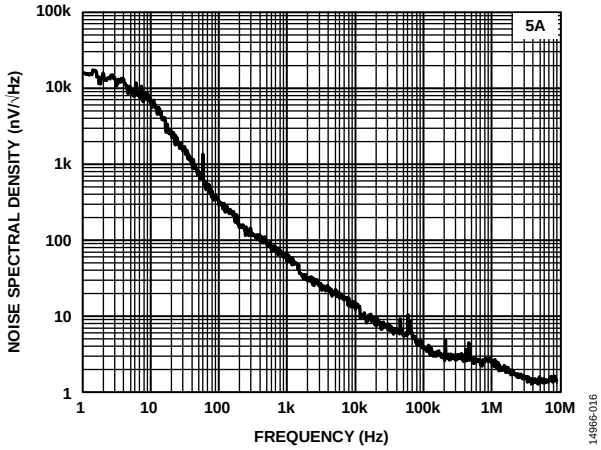

Figure 16. NSD vs. Frequency at V_{IN} = 1.8 V, I_O = 5 A NSD of Active Paralleling

THERMAL TEST RESULTS

Figure 17 and Figure 18 show the thermal test board results. As shown in Figure 17 and Figure 18, the ADP1763 devices are thermally balanced.

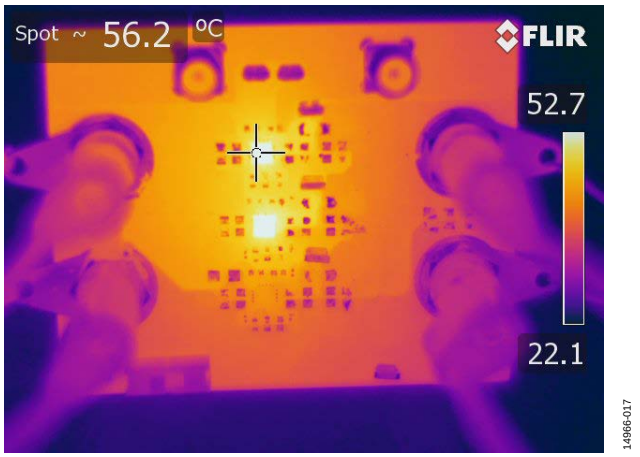

Figure 17. Thermal Test of Passive Paralleling

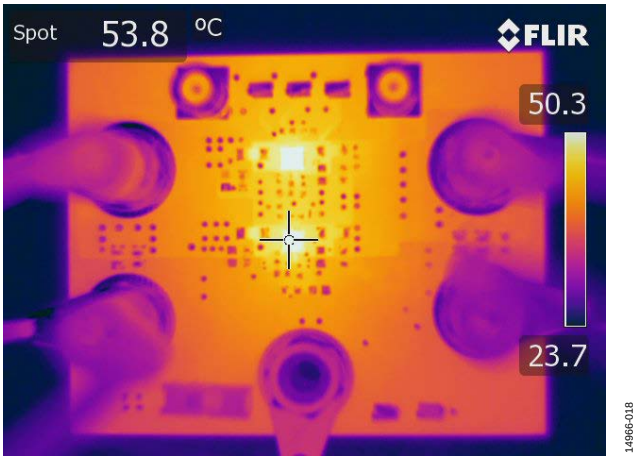

Figure 18. Thermal Test of Active Paralleling

CONCLUSION

This application note introduces two methods of paralleling LDO regulators using passive current sharing and active current sharing in high output current LDO applications. The design considerations and test results, including the current sharing accuracy, load regulation, soft start, noise spectral density, and thermal performance are demonstrated.