ANALOG DEVICES

AN-1416
APPLICATION NOTE

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Setup Example for Configuring the AD7616 for High Dynamic Range Applications

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INTRODUCTION

The AD7616 is a dual, simultaneous sampling, 16-channel, 16-bit successive approximation register (SAR), analog-to-digital converter (ADC). The AD7616 is ideally suited to protection and measurement applications in the energy distribution market. The AD7616 contains a host of features designed with protection and measurement applications in mind, such as an integrated programmable gain amplifier (PGA) with a low drift, 1 MΩ input impedance, highly flexible programmable sequencer, and the ability to perform oversampling up to 128×. This application note provides a detailed description of how to configure the AD7616 in one of its many modes of operation to achieve an increased dynamic range of more than 100 dB. This application note is intended as a quick start reference for the user to integrate the AD7616 into the application.

TABLE OF CONTENTS

REVISION HISTORY

6/2017—Revision 0: Initial Version

DYNAMIC RANGE REQUIREMENT

Depending on the application, the amplitudes of the input signals of interest can vary substantially. Relay protection applications, for example, generally have small scale signals relative to a fault condition; however, the user may wish to measure both the nominal and fault condition. This measurement requires an ADC with a large dynamic range to resolve these smaller input signals to the desired accuracy. The dynamic range required for such applications can be calculated as follows:

$$DR = 20 \times \log_{10} \frac{Signal_{MAX}}{Signal_{MIN}}$$

where:
DR is the dynamic range.
$Signal_{MAX}$ is the largest signal the ADC can resolve.
$Signal_{MIN}$ is the smallest signal the ADC can resolve.

Depending on the accuracy requirement of the application, the user may desire an accuracy greater than 16 bits. This requirement can be achieved with the AD7616 using the following methods:

1. Oversampling the analog input to achieve a signal-to-noise ratio (SNR) of up to 96 dB.
2. Dual gain sampling of a signal to increase the effective dynamic range.

Using the ±10 V input range of the AD7616, the user can typically achieve a 90.5 dB SNR without any oversampling. This SNR increases to a maximum of 96 dB with an oversampling ratio (OSR) of 64×. Similarly, the ±2.5 V range achieves an 87 dB SNR without oversampling, and a 93.9 dB SNR with an OSR of 64×.

Table 1. SNR Achievability with Oversampling

OSR	±2.5 V Range (dB)	±10 V Range (dB)
0	87	90.5
64	94	96

Consider an input signal from a sensor that is normally quite small in relation to the input range, but can overrange (for example, during startup or under a fault condition), as shown in Figure 1.

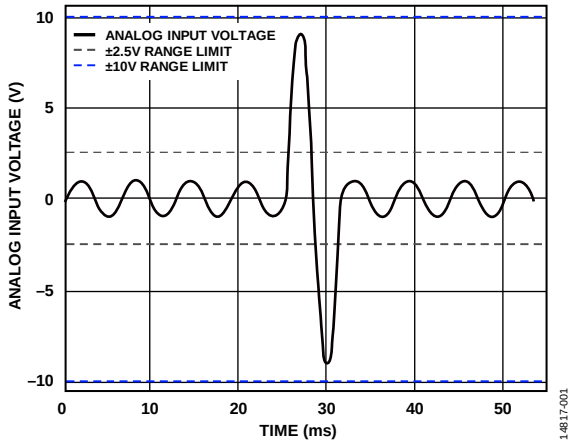

Figure 1. Out of Range Signal

By combining two AD7616 channels to sample the same input signal, it is possible to achieve a large dynamic range. The AD7616 has one PGA per channel, which can be configured to accept an input signal of ±2.5 V, ±5 V, or ±10 V. Using different gains while sampling the same signal is key to increasing the dynamic range.

Figure 2 shows a typical dual sampling setup using one channel on each of the ADCs of the AD7616. The AD7616 consists of two ADC cores and two 8:1 muxes for a total of 16 channels. For this example, the use of one channel on each multiplexer, which allows both channels to be sampled simultaneously, is shown in Figure 2.

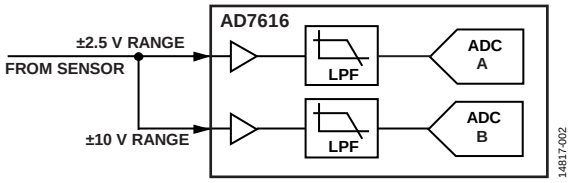

Figure 2. Dual Gain Sampling Setup

The connection shown in Figure 2 is typical for monitoring a single phase of a 3-phase power system and can be extended to monitor the other phases as needed. The configuration described in this application note assumes that the ADC channels are assigned as described in Table 2, where three phases are monitored.

Table 1 shows that oversampling can increase the SNR to 94 dB with an OSR of 64× in the ±2.5 V range. Oversampling at a more modest OSR of 4× with the same range, the smallest signal that is possible to be resolved is approximately ±88 µV. This can be calculated, knowing that the SNR for the ±2.5 V range at an OSR of 4× is 89 dB, as follows:

$$SNR = 20 \times \log_{10} (Largest\ Signal/Smallest\ Signal) = 89\ dB$$

where:
SNR is the signal-to-noise ratio.
Largest Signal is the maximum amplitude of the signal applied to the analog inputs.
Smallest Signal is the amplitude of the smallest resolvable signal from the noise floor.

The largest signal is the input range; in this case, ±2.5 V. Using this input range value, the equation can be rearranged and solved to determine the smallest signal that can be resolved by the ADC. This yields a result of ±88 µV.

By sampling using both the ±10 V and ±2.5 V input ranges, it is possible to achieve a dynamic range of up to

$$DR = 20 \times \log_{10} \frac{\pm 10\ \text{V}}{\pm 88\ \mu\text{V}} \cong 101\ \text{dB}$$

where *DR* is the dynamic range.

Table 2. ADC Channel Configuration

Phase	Channel	Range for ADC A (V)	Range for ADC B (V)
A	V0A/V0B	±2.5	±10
B	V1A/V1B	±2.5	±10
C	V2A/V2B	±2.5	±10

PIN CONFIGURATION

The AD7616 can be configured to operate in either hardware or software mode. Hardware mode uses pin control to configure options such as the sequencer, analog input range, and oversampling ratio. Software mode involves programming the on-board registers via either the parallel interface or the serial interface, and unlocks more of the feature set of the device. This setup example uses software mode, programmed via the parallel interface. Using the serial interface to configure the device is similar to programming the device using the parallel interface. For full details, see the AD7616 data sheet.

Before programming the on-board registers, configure the control pins as shown in Table 3 and Figure 3 prior to power-up, for this example. Hardware control pin values are latched by the device upon release of reset or after a full reset occurs. Any changes to the configuration also require a full reset.

Table 3. Hardware Pin Configuration

Pin Name	Setting	Description
HW_RNGSELx	GND	Configures the device in software mode.
SER/$\overline{\text{PAR}}$	GND	Selects the parallel interface when tied to ground.
SEQEN	GND	No function, tie to ground.
CHSELx	GND	No function, tie to ground.
REFSEL	GND/V_{CC}	Internal/external reference, as desired.

When the control pins are configured, the AD7616 can be powered on by supplying the appropriate voltage to the V_{CC} pin and the V_{DRIVE} pin. It is necessary to provide a full reset to the device after the supplies have stabilized. For full details, see the AD7616 data sheet.

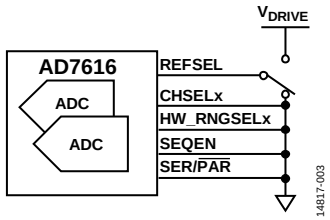

Figure 3. Hardware Control Pin Connections

PROGRAMMING THE AD7616

The AD7616 is highly configurable in software mode via the on-board registers. These registers can be accessed via either the parallel or the serial interface and are 16 bits wide. This application note uses the parallel interface for the example described. A flowchart showing the required register writes is shown in Figure 4. The following register write commands configure the AD7616 to dual sample three different signals by using the programmable sequencer.

First, write to the configuration register. The configuration register is used in software mode to configure many of the main functions of the ADC, including the sequencer, burst mode, oversampling, and CRC operation.

Write Command 0x8460 to the configuration register to enable the sequencer in burst mode. Burst mode requires a single CONVST pulse to initiate the conversion of every channel pair configured in the sequencer stack registers. Conversion results are then stored until the user is ready to read back the results. For full details, see the AD7616 data sheet.

The input range registers are configured next. Six channels are enabled for sampling as described in Table 2. Three channels are set to the ±2.5 V range and three channels are set to the ±10 V range. There are four input range registers; however, only two are required for this example: Register A1 and Register B1. Write Command 0x8815 to configure the input range of the V0A to V2A channels to the ±2.5 V range. Write Command 0x8C3F to configure the input range of the V0B to V2B channels to the ±10 V range.

Finally, write to the sequencer stack registers. The structure of the sequencer registers forms a 32-layer stack, in which each layer can contain two channels (any channel from ADC A and any channel from ADC B). The sequencer is programmed as shown in Table 4.

Table 4. Sequencer Programming

Layer	ADC A Channel	ADC B Channel	Code
1	V0A	V0B	0xC000
2	V1A	V1B	0xC211
3	V2A	V2B	0xC522

The last layer used in the stack, Layer 3 in this example, has the SSREN bit set to Logic 1. This defines the last layer of the stack. After the sequencer reaches the layer with the SSREN bit set to 1, the sequencer resets the stack pointer to the first layer of the stack. The sequence can then be repeated.

The AD7616 is now configured to sample three signals, as per the configuration shown in Figure 2. Write Command 0x0000 to the device to return it to read mode and begin sampling. Table 5 provides a summary of the registers programmed for this example.

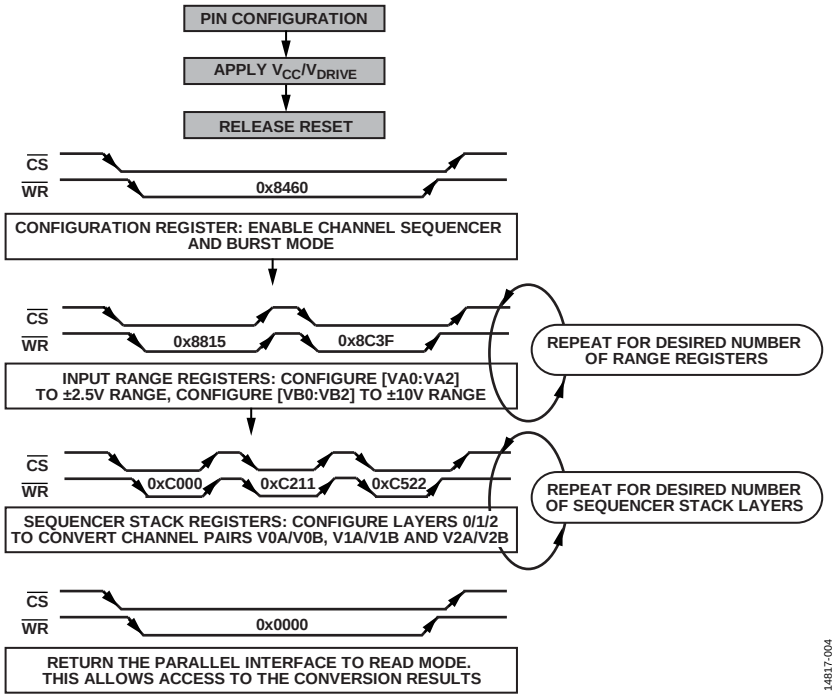

Figure 4. Register Configuration Flowchart

Table 5. Register Summary

Register	Command	Description
Configuration	0x8460	Enables sequencer and burst mode.
Input Range A1	0x8815	Configures the V0A to V2A channels to the ±2.5 V range.
Input Range B1	0x8C3F	Configures the V0B to V2B channels to the ±10 V range.
Sequencer Stack 1	0xC000	Defines V0A and V0B as the first channel pair in the sequencer stack.
Sequencer Stack 2	0xC211	Defines V1A and V1B as the second channel pair in the sequencer stack.
Sequencer Stack 3	0xC522	Defines V2A and V2B as the last channel pair in the sequencer stack. The SSREN bit is set to 1.
Conversion Results	0x0000	Returns the device to read mode to access conversion results.

CONVERSIONS

In burst mode, a single CONVST signal initiates the conversion of every channel programmed to the sequencer stack registers. The device internally generates the remaining CONVST signals required to complete the sequence. Figure 5 shows the operation of the device in this mode. Upon release of reset, the on-chip registers are programmed, as shown in Figure 4. After switching the device back to conversion read mode, a dummy conversion is required to latch the new configuration into the device. Thereafter, the user must supply a single CONVST pulse to initiate the conversion of the entire sequence. After the sequence finishes (indicated by a BUSY high to low transition), the user can read back the three channel pair conversion results, as shown in Figure 5.

READING CONVERSION RESULTS

In burst mode, the readback of conversions occurs after all of the channels in the sequence completes conversion, as shown in Figure 5. The cycle time (t_{CYCLE}) to complete conversions and readback of conversion results, with number of channel pairs, N, and oversampling ratio, x, is estimated by

$$t_{CYCLE} = (N \times x)(t_{ACQ} + t_{CONV}) - t_{ACQ} + 25\text{ ns} + t_{CS\_SETUP} + N(t_{RB}) + t_{QUIET}$$

where:
t_{ACQ} is the typical acquisition time.
t_{CONV} is the typical conversion time.
t_{CS_SETUP} is the BUSY falling edge to $\overline{CS}$ falling edge setup time.
t_{RB} is the time required to read back the conversion results using the parallel interface.
t_{QUIET} is the time required from the last $\overline{CS}$ rising edge to the CONVST rising edge.

Using the parallel interface for the readback of conversion results allows the user to maintain maximum throughput, even with the burst sequencer enabled. Substituting the appropriate numbers from the AD7616 data sheet into the t_{CYCLE} equation results in a cycle time of 11.945 µs to convert the three channel pairs with an OSR of 4×. This substitution achieves a throughput of 83 kSPS per channel.

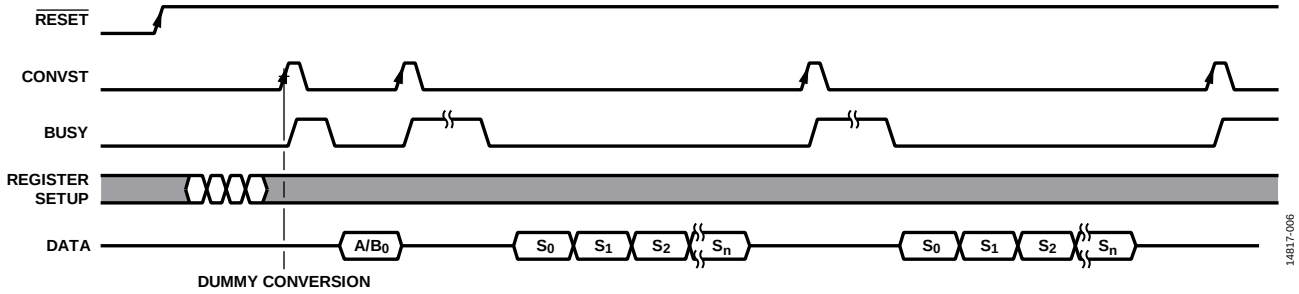

Figure 5. Burst Mode Operation

CONCLUSION

The user can detect overvoltage and overcurrent conditions on the input by monitoring the ADC A output, using the smaller ±2.5 V input range setting. With this method, the user can preserve dynamic range by using the full-scale amplitude range of the ±2.5 V range setting. The user can then switch to monitoring the larger ±10 V input range to capture the nature and magnitude of a fault condition. This method removes the requirement for the user to apply dynamic input range scaling before the ADC, and the channel density of the AD7616 makes dual sampling a cost effective option. This application note demonstrates that, by using a dual sampling setup with an OSR of 4×, it is possible to increase the dynamic range of the AD7616 to 101 dB. Sampling three channels, with oversampling enabled, it is possible to maintain a throughput of greater than 83 kSPS per channel. In practical terms, for a 60 Hz input signal, the user can gather more than 1300 samples per line cycle using the method described in this application note.