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APPLICATION NOTE

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Modular Data Acquisition (DAQ) Footprint Using the AD7768/AD7768-4

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INTRODUCTION

A common trend in analog input/output module design is increased channel count in a smaller form factor. This trend is driven by the need to reduce cost and testing time by increasing the number of measurements achievable from a single module or a PCI extension for instrumentation (PXI) card slot. The increase in channel density contributes to an increase in thermal dissipation, which is a common issue for designers in modular applications. To design within the thermal budget requirements of high density data acquisition modules, customers must consider trade-offs for speed, bandwidth, and performance.

The AD7768/AD7768-4 are 8-channel and 4-channel, 24-bit simultaneous sampling analog-to-digital converters (ADCs). Selectable power modes and digital filter options can reconfigure the AD7768/AD7768-4 to suit a wide range of applications, such as industrial input/output modules, instrumentation, audio testing, control loops, and condition monitoring.

An external driver amplifier must be used to drive the input to the AD7768/AD7768-4. Drive requirements for the analog front end scale with the front-end sampling rate. Selectable precharge buffers on the AD7768/AD7768-4 reduce the burden on front-end driver amplifiers, which can allow lower power amplifiers to drive analog inputs with high sampling rates.

This application note outlines how to achieve −126.6 dB of total harmonic distortion (THD) at subsystem power levels as low as 19.5 mW per channel. This application note also compares combinations of high performance driver amplifiers and low power amplifiers with and without the assistance of the precharge buffers. These amplifiers are selected based on the suitability to drive the AD7768/AD7768-4 in particular power modes for a fair and valid comparison. For example, the higher bandwidth amplifiers selected to drive the AD7768/AD7768-4 in fast power mode work equally well in median or low power mode, but may burn more power than necessary depending on which system is being used. The appropriate combinations of driver amplifiers and power modes evaluated in this application note allow the design of a single DAQ platform to achieve the highest performance within specific bands of thermal or power constraints. Some of the trade-offs system designers encounter are discussed.

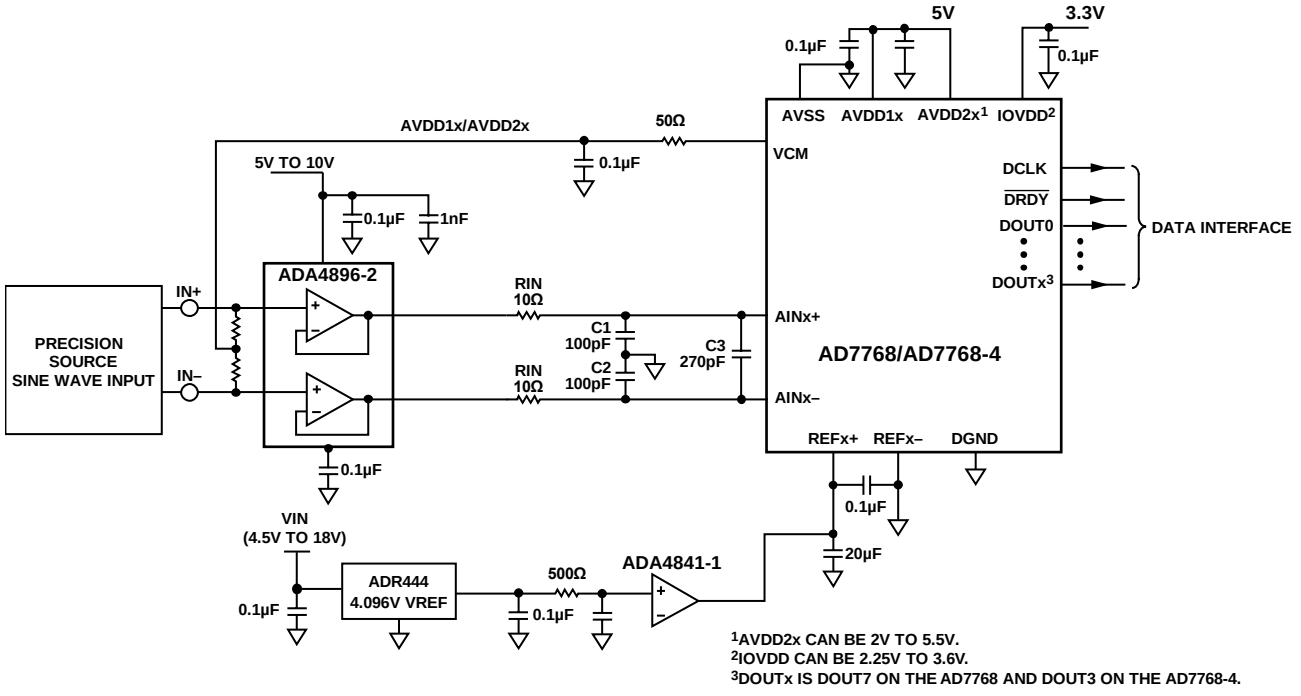

Figure 1. Typical Connection Diagram for the AD7768/AD7768-4 in Fast Power Mode, with the ADA4896-2 as the Driver Amplifier

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REVISION HISTORY

12/2016—Revision 0: Initial Version

CIRCUIT DESCRIPTION

The amplifier testing for the AD7768/AD7768-4 was conducted using the EVAL-AD7768FMCZ evaluation platform, the EVAL-AD7768-4FMCZ evaluation platform, and various amplifier mezzanine cards (AMCs). The amplifiers populated on each AMC are listed in the Amplifier Configuration section. The EVAL-AD7768FMCZ and the EVAL-AD7768-4FMCZ evaluation platforms schematics, available at www.analog.com/eval-ad7768 and www.analog.com/eval-ad7768-4, respectively, can be configured to use an AMC (on one channel only) as the driver amplifier input. See the EVAL-AD7768FMCZ and EVAL-AD7768-4FMCZ for more details. The AMCs available are populated with various amplifiers and designed specifically to work with Analog Devices, Inc., ADCs. The EVAL-SDP-H1 is connected to the EVAL-AD7768FMCZ and the EVAL-AD7768-4FMCZ evaluation platforms to interface with the evaluation software, which is supplied with the evaluation hardware. A precision audio source was used for ac analysis.

The following amplifiers selected for testing have been identified to complement each of the different power modes on the AD7768/AD7768-4:

- In low power mode: ADA4805-2, ADA4500-2, ADA4841-2, and ADA4940-1.
- In median mode: ADA4805-2, ADA4807-2, ADA4500-2 and ADA4940-1.
- In fast power mode: ADA4807-2, ADA4896-2, ADA4899-1 and ADA4940-1.

Table 1 shows the performance and power specifications for the selected amplifiers. Some of these amplifiers are available in different package sizes and options.

Table 1. Amplifier Specifications

Amplifier	Features	Bandwidth (BW) (MHz)	Slew (V/µs)	Voltage Noise Density (nV/√Hz)	Current Noise Density (pA/√Hz)	Offset Voltage (µV maximum)	Offset Drift (µV/C)	Supply (V)	Power per Amplifier (mA)
ADA4899-1	Unity gain, ultralow distortion	600	310	1	2.6	230	5 typical	5 to 12	16
ADA4896-2	Low drift, rail to rail output (RRO)	230	120	1	2.8	500	0.2 typical	±3 to ±5	3
ADA4807-2	Rail to rail input/ output (RRIO), low drift	180	225	3.1	0.7	125	0.7 typical	±3 to ±5	1
ADA4805-2	RRO, low drift	105	190	5.2	0.7	125	1.5 maximum	±3 to ±5	0.625
ADA4940-1	RRO, differential amplifier	260	95	3.9	0.81	350	1.2 typical	3 to 7	1.25 total[1]
ADA4841-2	RRIO low noise and distortion	80	13	2.1	1.4	300	1 typical	2.7 to 12	1.2
ADA4500-2	RRIO, zero input crossover distortion	10	8.7	14.5	<0.0005	700	5.5 maximum	2.7 to 5.5	1.8

[1] Total power for a single channel.

SELECTING A POWER MODE

The AD7768/AD7768-4 have three selectable power modes: low, median, and fast. These power modes select an operating point for the AD7768/AD7768-4 in which the optimum bandwidth and power consumption can be chosen while maintaining the same dynamic range.

The power mode selected can be used in conjunction with the master clock divider (MCLK_DIV) to set this operating point correctly. MCLK_DIV determines the frequency the modulator runs at. The modulator output is then decimated to give the final output data rate (ODR). The recommended modulator frequency (f_{MOD}) ranges are shown in Table 2.

Table 2. Recommended f_{MOD} Ranges

Power Mode	Typical MCLK_DIV	Recommended f_{MOD} (MHz)
Low	MCLK/32	0.036 to 1.024
Median	MCLK/8	1.024 to 4.096
Fast	MCLK/4	4.096 to 8.192

Table 3 shows the power consumption for each power mode with a 32.768 MHz master clock applied, analog input precharge buffers on, at nominal supplies, using a wideband filter and a decimation rate of 32. Table 3 shows that the power consumption scales with speed and bandwidth.

ANALOG INPUT STRUCTURE

Figure 2 shows the analog input structure of the AD7768/AD7768-4. The analog input precharge buffers can be enabled on a per channel basis. When enabled, the analog input precharge buffers provide the charge to the sampling capacitors for the initial sampling period and charge the bulk of the current required to settle the sampling capacitors. The remaining charge is driven by the external amplifier, which charges the final finer settling of the sampling capacitors to achieve precision results.

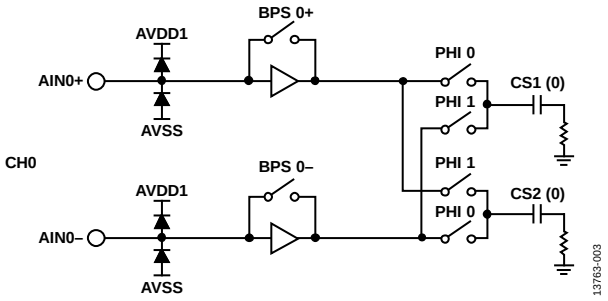

Figure 2. Analog Input Structure

The precharge buffers reduce the input current sourced from the amplifier from 320 µA to ~25 µA for a 5 V input at the fastest sampling rate. See the AD7768/AD7768-4 data sheet for more information about the AD7768/AD7768-4 analog input structure.

Figure 3 shows the ADA4807-2 AMC connected to the AD7768/AD7768-4 evaluation board.

Table 3. Power Modes for the AD7768/AD7768-4

Power Mode	Maximum Speed (kSPS)	Wideband BW (kHz)	Wideband Power (mW/Channel)	Sinc BW (kHz)	Sinc Power (mW/Channel)
Fast	256	110.8	52	52.2	41
Median	128	55.4	28	26.1	22
Low	32	13.8	9.4	6.5	8.2

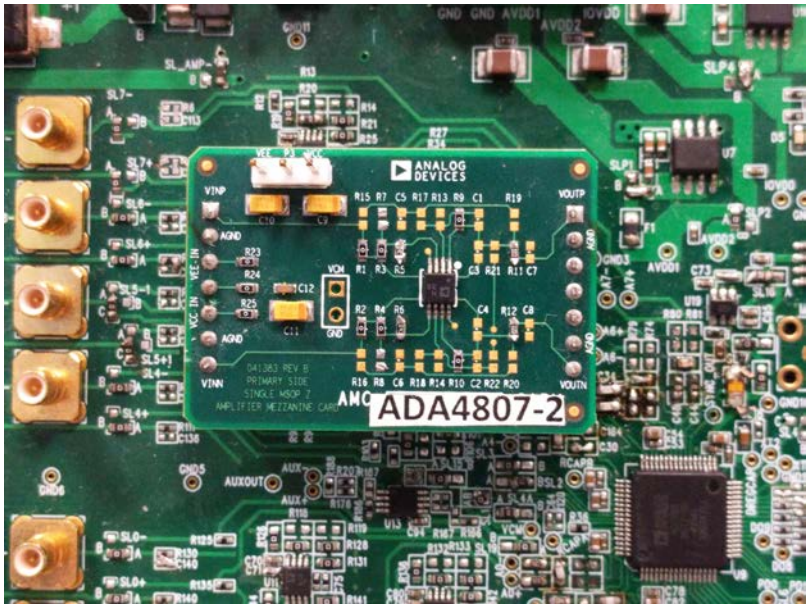

Figure 3. The ADA4807-2 AMC Setup on the EVAL-AD7768FMCZ

TESTING METHOD

The AD7768/AD7768-4 have a wideband digital filter used for this amplifier test. The wideband filter has a brick wall filter response with a cutoff frequency of 0.433 × ODR. The excellent pass-band ripple of ±0.005 dB allows excellent frequency domain measurements to determine the performance of drive amplifiers vs. input frequency. The sinc5 digital filter has a bandwidth of 0.2 × ODR and 3 dB improvement for dynamic range, but is not considered for these comparative tests.

There is a resistor/capacitor (RC) network between the amplifier output and the ADC input. Figure 4 shows a typical RC network used for the AD7768/AD7768-4 for most amplifier pairings. The RC network performs a variety of tasks. C1 and C2 are charge reservoirs to the ADC, providing the ADC with fast charge current to the sampling capacitors.

Capacitor C3 removes common-mode errors between the AINx+ and AINx− inputs. These capacitors, in combination with RIN, form a low-pass filter to filter out glitches related to the input switching. The input resistance also stabilizes the amplifier when driving large capacitor loads and prevents the amplifier from oscillating.

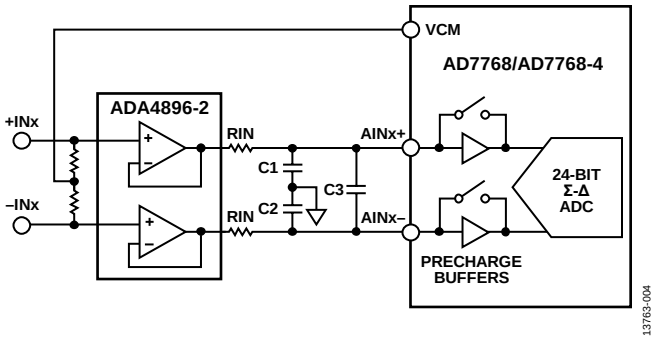

Figure 4. Typical Input Structure for an RC Network

The specific details of each of the RC antialias networks are covered in the Amplifier Configuration section. The targeted cut off frequencies (f_C) are 6 MHz, 12 MHz, and 24 MHz for low, median, and fast power modes, respectively. Standard resistor and capacitor values were chosen to give approximately the same f_C in each power mode

Table 4 shows the combinations of RIN, C1 and C2, and C3, which were selected to collect data in fast power mode. Faster and higher power amplifiers settle glitches on the ADC input quickly. Lower power amplifiers require larger RIN values to prevent oscillations due to changes on the input. The switching effects of the modulator are more apparent in fast power mode and, in particular, for the lower power amplifiers. These amplifiers may need larger capacitor values at the input of the AD7768/AD7768-4 to settle the fast transients caused by the modulator switching.

The ADA4807-2 requires larger capacitors, as shown in Table 4. The ADA4807-2 requires at least a 22 Ω RIN resistor, and a larger capacitance at the input. As a result, the ADA4807-2 has an RC cutoff at 11.6 MHz for fast power mode operation. The other amplifiers in Table 4 operate with the RC cutoff at approximately 24 MHz. The input RC of the ADA4807-2 is limited because the amplifier needs at least a 22 Ω RIN resistor, although the capacitors used must also be larger than a 24 MHz f_C allows.

Table 4. Example RC Antialias Filter Network in Fast Power Mode

Amplifier	RIN (Ω)	C1, C2 (pF)	C3 (pF)
ADA4899-1	5.1	270	680
ADA4940-1	82	68	Not inserted
ADA4896-2	10	100	270
ADA4807-2	22	82	270

RESULTS

LOW POWER MODE

Low power mode offers a 32 kSPS ODR and 12.8 kHz of bandwidth when using the wideband digital filter with a 32.768 MHz clock. Table 5 shows the signal-to-noise ratio (SNR), THD, and signal-to-noise-and-distortion ratio (SINAD) for the low power mode for the selected amplifiers. The input applied is a 1 kHz sine wave signal at −0.5 dB from a full-scale input with precharge buffers enabled and disabled.

Table 5 displays the performance and power consumption of each amplifier tested, sorted in terms of efficiency. Power (mW) is the power consumption of the drive amplifier on a single differential channel. The precharge (mW) power consumption is the power of two precharge buffers enabled on a differential channel for the specific sampling rate. The total (mW) is the power of the drive amplifier and the precharge buffer if enabled.

The ADA4805-2 with the precharge buffers disabled is the most efficient solution with 6.5 mW of power dissipated to achieve 106.5 dB SINAD. The ADA4841-2 has the highest performance with 106.9 dB SINAD, requiring 13.5 mW per channel. For the same power consumed, the ADA4841-2 shows almost −9 dB improved THD compared to the ADA4940-1. In general, these low power amplifiers from Analog Devices can easily drive the AD7768/AD7768-4 in low power mode. The ADA4805-2 and ADA4841-2 cases described previously highlight the trade-off DAQ system designers are faced with— the balance between power consumption and system performance. This trade-off is evident for all of the power modes, as shown in Table 5, Table 6, and Table 7.

The recommended amplifier pairing for the low power mode is the ADA4805-2 with precharge buffers disabled. For the power it consumes, such a combination of amplifier and ADC meets thermal restrictions in the DAQ system design. The total power consumed for the amplifier and the AD7768/AD7768-4 is only 15.875 mW per channel.

Table 5. Low Power Mode Performance vs. Power

Amplifier	Precharge Buffer	Power (mW)	Precharge (mW)	Total (mW)	SNR (dB)	THD (dB)	SINAD (dB)
ADA4805-2	Disabled	6.50	Not applicable	6.5	106.6	−126.6	106.5
ADA4841-2	Disabled	13.45	Not applicable	13.5	107.0	−129.7	106.9
ADA4940-1	Disabled	13.53	Not applicable	13.5	107.0	−121.0	106.8
ADA4841-2	Enabled	13.38	1.31	14.7	106.9	−131.1	106.8
ADA4940-1	Enabled	13.56	1.31	14.9	106.5	−122.3	106.3
ADA4500-2	Disabled	15.61	Not applicable	15.6	106.7	−112.1	105.8
ADA4500-2	Enabled	15.534	1.31	16.8	106.6	−110.1	105.2

MEDIAN POWER MODE

Median power mode offers 128 kSPS ODR with a 32.768 MHz clock and 51.2 kHz of bandwidth when using the wideband filter. The input applied is a 1 kHz sine wave signal at −0.5 dB from full scale. Table 6 is sorted in terms of efficiency.

The ADA4940-1, with precharge disabled, has the highest performance with 106.1 dB SINAD, requiring 13.9 mW per channel. These results are taken with a single 5 V supply to the amplifier. Thus, the DAQ system of the ADC and amplifier can run from the same rail, minimizing the design size and cost.

The benefits of the precharge buffers are shown in the THD results in Table 6. For example, the ADA4500-2 has a −17.5 dB improvement in THD with precharge buffers enabled vs. disabled. The ADA4805-2, with precharge buffers disabled, is the most efficient solution with 6.9 mW power dissipated. However, the performance is diminished in median power mode vs. in low power mode. One solution to increase performance is to increase the headroom of the amplifier from 6 V to 10 V. The results shown in Table 6 are for a 6 V supply to the ADA4805-2. For all supply levels, see Table 9. The increased headroom, coupled with the precharge buffers enabled, yields −119.4 dB of THD and 105.2 dB of SINAD, although at the expense of more power consumption.

In general, when using the precharge buffers with amplifiers that have enough power and bandwidth, the precharge buffers only offer small improvements in performance. The real benefit of the precharge buffers is shown when low power, low bandwidth amplifiers perform in a power mode they otherwise struggle to perform in.

The ADA4940-1 with precharge buffers disabled is the recommended amplifier for median power mode. The total power consumed in this case for both the ADA4940-1 and AD7768/AD7768-4 is just 41.4 mW per channel.

FAST POWER MODE

Fast power mode offers 256 kSPS ODR with a 32.768 MHz clock and 102.4 kHz of bandwidth when using the wideband filter. Table 7 is sorted in terms of efficiency and displays the performance and power consumption of each amplifier tested, with and without precharge assistance.

The AD7768/AD7768-4 in fast power mode achieves the greatest benefits of the precharge buffers. The precharge buffers enable high performance, even with the high modulator rates in fast power mode. The benefit of the precharge buffers is an increase in THD performance in all amplifiers. The ADA4896-2 shows the most improvement in THD performance when the precharge buffers are enabled. Using just 45.7 mW of power, the ADA4896-2 and AD7768/AD7768-4 combination achieves −130 dB of THD when running the ADA4896-2 on a single 6 V supply.

The ADA4940-1 with precharge buffers disabled is the most efficient solution with 14.4 mW of power dissipation, although performance must be sacrificed slightly to achieve this result. The recommended amplifier for power savings in fast power mode is the ADA4940-1. The total power consumed for the ADA4940-1 and the AD7768/AD7768-4 is 65.9 mW per channel.

Overall, when designing a general-purpose configurable DAQ system, the ADA4896-2 shows the best performance across all three power modes. However, if the power consumption of the whole DAQ system is limited, some of the lower power amplifiers shown in Table 5 and Table 6 can offer a more efficient solution for low and median power modes, respectively.

Table 6. Median Power Mode Performance vs. Power

Amplifier	Precharge Buffer	Power (mW)	Precharge (mW)	Total (mW)	SNR (dB)	THD (dB)	SINAD (dB)
ADA4805-2	Disabled	6.91	Not applicable	6.9	105.3	−104.3	102.0
ADA4805-2	Enabled	6.87	4.75	11.6	104.6	−107.2	102.8
ADA4940-1	Disabled	13.86	Not applicable	13.9	106.3	−120.7	106.1
ADA4500-2	Disabled	15.76	Not applicable	15.8	105.3	−94.0	94.2
ADA4940-1	Enabled	13.37	4.75	18.2	106.0	−121.6	105.8
ADA4500-2	Enabled	15.48	4.75	20.2	106.6	−111.5	105.5
ADA4807-2	Disabled	28.01	Not applicable	28.0	105.9	−117.9	105.5
ADA4807-2	Enabled	27.67	4.75	32.4	105.5	−117.9	105.2

Table 7. Fast Power Mode Performance vs. Power

Amplifier	Precharge Buffer	Power (mW)	Precharge (mW)	Total (mW)	SNR (dB)	THD (dB)	SINAD (dB)
ADA4940-1	Disabled	14.36	Not applicable	14.4	105.4	−114.5	105.0
ADA4940-1	Enabled	13.4	9.3	22.7	105.2	−120.4	105.1
ADA4896-2	Disabled	36.94	Not applicable	36.9	106.7	−118.0	106.5
ADA4896-2	Enabled	36.35	9.3	45.7	106.5	−130	106.4
ADA4807-2	Disabled	65.89	Not applicable	65.9	105.7	−98.2	97.9
ADA4807-2	Enabled	64.9	9.3	74.2	105.7	−112.7	105.0
ADA4899-1	Disabled	378.12	Not applicable	378.1	106.8	−117.9	106.5
ADA4899-1	Enabled	377.16	9.3	386.5	106.8	−120.9	106.6

SINGLE DAQ FOOTPRINT

The results in Table 5 show the ADA4805-2 is the most power efficient front-end combination tested with the AD7768/AD7768-4. The ADA4805-2 can help to meet power requirements while also meeting data sheet specifications. The combination of power scaling and precharge buffers enables the DAQ footprint to achieve minimum power consumption. Figure 5 shows an example of a low power DAQ footprint.

Table 8 shows the total power dissipation for the AD7768/AD7768-4 single DAQ footprint.

The ADC power specifications in Table 8 are for 5 V AVDD1x, 2.5 V AVDD2x, IOVDD, 32.768 MHz MCLK, and a wideband filter, decimated by 32.

Total driver requirements for the low power and median power modes in Table 8 are for an 8-channel ADC with both 6 V and 10 V supplies.

Reference and reference buffers consumption are for the ADR444 and the ADA4841-1 operating on a 6 V supply rail.

Figure 5 shows the minimum form factor for eight channels of AD7768/AD7768-4. The form factor includes the AD7768/AD7768-4, 8 × ADA4805-2, ADR444, ADA4841-1, and 3 × ADP7118 low dropout (LDO) regulators. The 8-channel acquisition system can be achieved on 49.4 mm × 64.1 mm of printed circuit board (PCB) with a total power dissipation of 148.6 mW. A similarly sized footprint can be used in a higher power DAQ module where greater bandwidth is required.

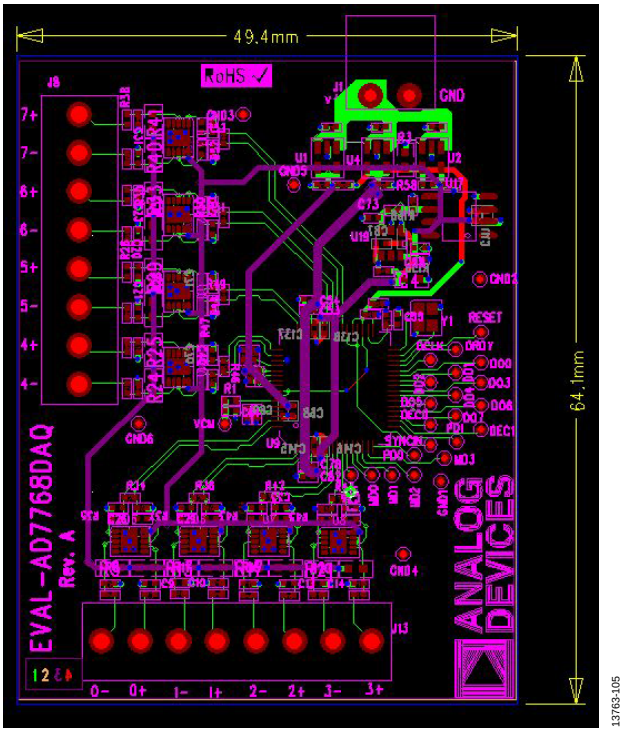

Figure 5. Example DAQ Footprint for the AD7768/AD7768-4 and the ADA4805-2

Table 8. Total Power Dissipation for Single DAQ Footprint

Power Mode	8-Channel ADC (mW)	Total Drive Requirements (mW)	Reference Buffer (mW)	Total Power (mW)	Power per Channel (mW)
Low Power (6 V Amplifier Supply, Precharge Buffers Disabled)	75	52	29.1	156.1	19.5
Low Power (10 V Amplifier Supply, Precharge Buffers Disabled)	75	99.8	29.1	203.9	25.5
Median Power (10 V Amp Supply, Precharge Buffers Enabled)	260	106.5	29.1	395.6	49.4

AMPLIFIER CONFIGURATION

Figure 6 shows a typical amplifier configuration, with the exception of the ADA4940-1, which is a fully differential amplifier. The ADA4899-1 requires a 25 Ω resistor on the noninverting input, for stability purposes, when operating with a gain of 1 (not shown in Figure 6).

CONFIGURATION OF THE AD7768/AD7768-4

The AD7768/AD7768-4 was set up as follows: IOVDD = 3.3 V, AVDD1x and AVDD2x = 5 V, MCLK = 32.768 MHz, V_{REF} = 4.096 V, wideband filter, precharge reference buffers disabled, analog input precharge buffers enabled/disabled, all channels enabled, chopping frequency (f_{CHOP}) = f_{MOD}, decimated by 32.

The evaluation boards used were the EVAL-AD7768FMCZ and the EVAL-AD7768-4FMCZ.

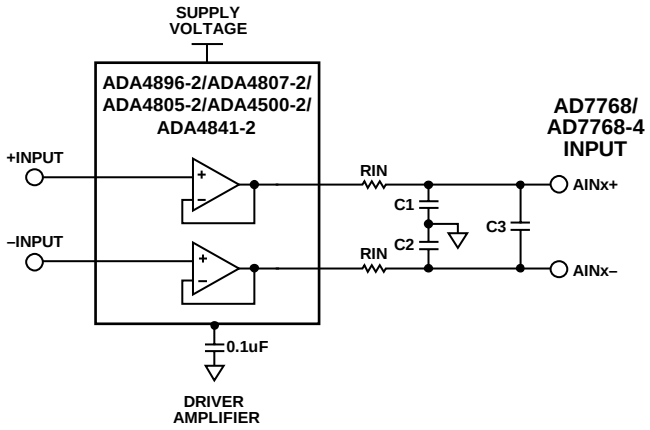

Figure 6. Typical Drive Amplifier Configuration

Table 9. Configuration of Amplifiers for Each Power Mode

Amplifier	Power Mode	RIN (Ω)	C1, C2 (pF)	C3 (pF)	f_C (MHz)	Supply Voltage (V)
ADA4899-1	Fast	5.1	270	680	19.1	−4 and +8
ADA4896-2	Fast	10	100	270	24.9	0 and 8
ADA4807-2	Fast	22	82	270	11.6	0 and 10
	Median	22	82	270	11.6	0 and 6
ADA4940-1	Fast	82	68	Do not insert	28.5	0 and 5
	Median	33	56	180	11.6	0 and 5
	Low	33	120	330	6.2	0 and 5
ADA4805-2	Median	33	56	180	11.6	0 and 6
	Low	33	120	330	6.2	0 and 6
ADA4500-2	Median	15	120	390	11.8	0 and 5
	Low	15	270	680	6.5	0 and 5
ADA4841-2	Low	33	120	330	6.2	0 and 6

CONCLUSION

This application note simplifies the amplifier selection process in a DAQ system design based on the AD7768/AD7768-4, with consideration for system bandwidth, performance requirements, and power constraints. The AD7768/AD7768-4 are suitable for acquisition of both ac and dc signals and are highly customizable to suit bandwidths from dc up to 110 kHz. As a result, the AD7768/AD7768-4 are suitable for a wide variety of applications. By changing the selected power mode and decimation rate, a system designer can match the required operating point for both power consumption and noise performance. For systems that are required to be adaptable, the power mode and decimation rates are software configurable. The information presented throughout this application note serves as a starting point to begin optimizing a DAQ design that can fulfill those key design challenges.

A more complex front-end filter can potentially improve the results for a specific bandwidth, because all noise figures given are not band limited. The switching input structure of the AD7768/AD7768-4 requires high bandwidth amplifiers, particularly in fast power mode. These driver amplifiers are required to settle the effect of fast switching transients before the next modulator sample takes place. The precharge input buffers can help in some instances to allow lower power amplifiers to be used. In general, enabling the precharge buffers improves THD.

The solutions discussed can be chosen for system power requirements, performance requirements, or single-supply operation.

The optimum driver amplifiers for each of these requirements of power, performance, and supply are as follows:

- The ADA4805-2 is suited for low power, particularly in low power mode.
- The ADA4940-1 is suited for single-supply operation, which is also the recommended fully differential amplifier to drive the AD7768/AD7768-4.
- For optimum performance in fast power mode, the ADA4896-2 performs best, although not consuming the same power as the ADA4899-1. The ADA4896-2 is also suitable for a general-purpose DAQ module, which can be configured for all three power modes.