AN-1366
APPLICATION NOTE

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Using the ADP5070/ADP5071 to Create Positive and Negative Voltage Rails when $V_{OUT} < V_{IN}$

by Kevin Tompsett

INTRODUCTION

The ADP5070/ADP5071 are dual high performance dc-to-dc regulators that generate independently regulated positive and negative rails. Their input range of 2.85 V to 15 V supports a wide variety of applications. Start-up sequencing, precision enable, the ability to synchronize switching frequency, and a pin-selectable power switch slew rate to reduce switching noise make the ADP5070/ADP5071 very flexible power parts. The ADP5070/ADP5071 data sheets give detailed descriptions of how to design the positive rail in the boost topology and the negative rail as an inverting buck boost. However, sometimes it is necessary to generate a positive voltage from an input that is less than the output voltage. Fortunately, the positive rail can easily be configured in the single-ended primary inductance converter (SEPIC) topology, which can generate an output voltage that is less than, equal to, or greater than the input for maximum flexibility. This application note provides appropriate design formulas and considerations for designing the ADP5070/ADP5071 in a SEPIC configuration.

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REVISION HISTORY

7/15—Revision 0: Initial Version

DESCRIPTION OF THE SEPIC TOPOLOGY

The SEPIC is one of the least understood yet commonly used dc-to-dc converter topologies. For a SEPIC, the Q1 and Q2 switches operate in opposite phase from one another. Figure 1 shows the current flow diagram for the two different switch states.

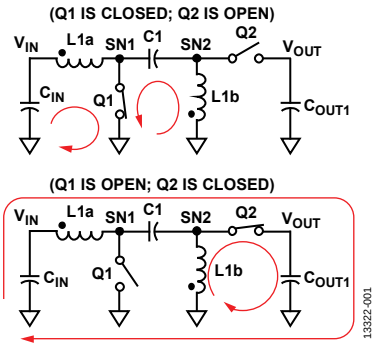

Figure 1. Current Flow in a SEPIC Converter

It is not immediately obvious, but the transfer capacitor (C1) voltage is constant at approximately V_{IN} with a small ripple. Figure 2 shows the idealized waveforms for a SEPIC. When Q1 is on, the voltage at SN2 is equal to $-V_{IN}$. Thus, during the time that Q1 is on (Q2 is off), the voltage across both L1a and L1b is V_{IN}, and when Q1 is off (Q2 is on), the voltage across both L1a and L1b is negative V_{OUT}. Calculate the equilibrium dc conversion ratio by using Equation 1 and applying the principles of inductor volt-second balance. D is the duty cycle of the converter (the fraction of the switching cycle that Q1 is on).

$$\frac{V_{OUT\_SEPIC}}{V_{IN}} = \frac{D}{(1-D)} \quad (1)$$

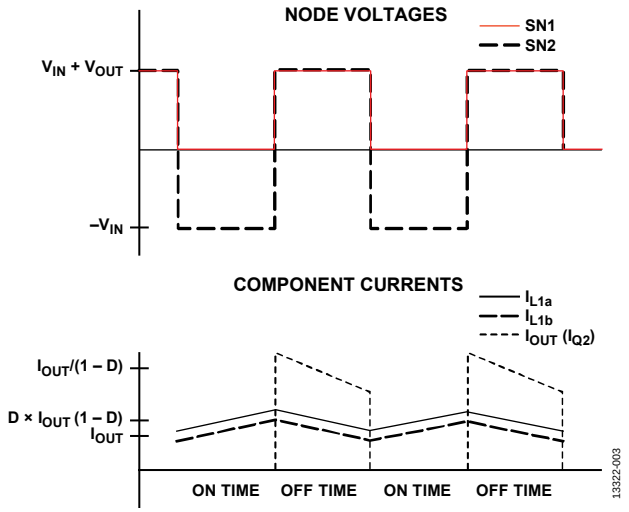

Figure 2. Idealized SEPIC Waveforms

Q2 is replaced by a diode because these supplies are generally lower power analog supplies where an asynchronous controller is appropriate.

L1a and L1b are coupled, which reduces current ripple in the inductors by a factor of 2 (see the Ćuk-Middlebrook paper cited in the References section), significantly reduces the complexity of the small signal model, and enables higher bandwidth by eliminating the SEPIC resonances calculated by Equation 2.

$$f_{SEPIC\_RESONANCE} = \frac{1}{2\pi\sqrt{(L1a + L1b)\,C1}} \quad (2)$$

LIMITS TO THE COUPLING COEFFICIENT

Even though coupling the inductors has distinct advantages, it is undesirable for the coupling to be so tight that significant energy transfer results through the core. To avoid this situation, the designer must ensure that the magnitude of the complex impedance of C1 is less than a tenth that of the impedance of the leakage inductance (L_{LKG}) plus the dc resistance (DCR) of a single winding.

Equation 3 designates this inequality. The leakage inductance of L_1 (L_{LKG}) is calculated by Equation 4 and the coupling coefficient (K) generally found on coupled inductor data sheets. L_M is the measured self inductance that appears in the ADP5070/ADP5071 data sheet.

$$|Z_{C1}| = \sqrt{ESR_{C1}{}^2 + \left(\frac{1}{2\pi C_{C1} f_{SW}}\right)^2} \le \frac{|Z_{L_{LKG\_L1}}|}{10} = \frac{\sqrt{DCR_{L1}{}^2 + 2\pi L_{L_{LKG\_L1}}}}{10} \quad (3)$$

$$L_{LKG} = L_M(1 - K)/K \quad (4)$$

SMALL SIGNAL ANALYSIS AND LOOP COMPENSATION

A complete small signal analysis of the SEPIC is beyond the scope of this application note; however, the equations provided in this application note allow the designer to compensate the design correctly. The ADP5070/ADP5071 design tool uses a more complete model, which is more accurate than the one provided in this application note but much more complicated.

In their paper, Ćuk and Middlebrook (see the References section) show that a coupled inductor, from both a small signal and a large signal perspective, behaves like an inductor with twice its single winding inductance value and without the SEPIC resonances. Therefore, analysis in this application note uses the effective inductance, that is, twice the single winding inductance value that appears on coupled inductor data sheets.

The first step in compensating a SEPIC is to choose an achievable target crossover frequency. Like most boost and buck boost topologies, the SEPIC has a right half plane zero (RHP) calculated by Equation 5. A RHP has the dual effect of adding gain, like a zero, and subtracting phase, like a pole. Therefore, the converter must be compensated for a crossover frequency that is a maximum of one fifth the frequency of the RHP (f_{RHP}).

The SEPIC has an additional resonance caused by the leakage inductance (L_{LKG}) and transfer capacitance (C1) that occur at f_{RES}. This resonance is generally well damped by the DCR of the inductors, but it can introduce significant phase lag. Therefore, it is good practice to cross over at least a decade before it. In addition, a current mode controller with standard Type II compensation is used; thus, the maximum achievable crossover frequency is approximately one tenth the switching frequency. Therefore, choose target f_C as the minimum of these three constraints, as shown in Equation 7.

$$f_{RHP} = \frac{R_{LOAD}\ D_{Q2}^{1.5}}{L \times D_{Q1}} \quad (5)$$

$$f_{RES} = \frac{1}{2\pi\sqrt{L_{LKG}C1}} \quad (6)$$

$$f_C = Minimum\left(\frac{f_{RHP}}{5}, \frac{f_{RES}}{10}, \frac{f_{SW}}{10}\right) \quad (7)$$

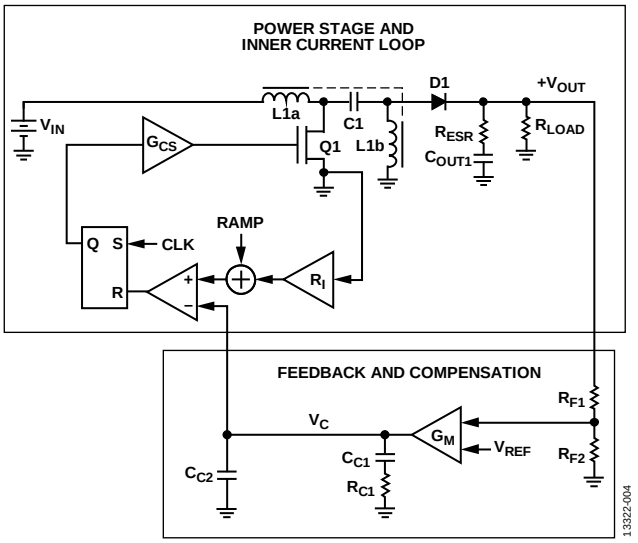

Figure 3. Block Diagram Showing Power Stage and Compensation Components

The compensation values in Figure 3 are calculated by Equation 8. Because it is assumed that ceramic output capacitors are used, select 10 pF as C_{C2}.

$$C_{C2} = -C_{C2} + \sqrt{\frac{V_{REF}^2 G_M^2 A_C^2}{4\pi^2 V_{OUT}^2}\left(\frac{1}{f_P^2} + \frac{1}{f_C^2}\right) - C_{C2}^2\left(\frac{1}{2} + \frac{f_C^2}{f_P^2}\right)} \quad (8)$$

$$R_{C1} = \frac{1}{2\pi f_P C_{C1}} \quad (9)$$

where f_P is the approximate dominant pole for the current mode converter.

$$f_P = \frac{(1 + D_{ON})}{(C_{OUT1})R_{LOAD}} \quad (10)$$

A_C is the magnitude of the open loop converter gain at the crossover frequency f_C:

$$A_C = \frac{F_M}{2D_{ON}D_{OFF}\left(1 + \frac{F_M V_{OUT}(1 + D_{ON})}{D_{ON}D_{OFF}^2 R_{LOAD}}\right)} \frac{\sqrt{1 + \left(\frac{f_C}{f_{RHP}}\right)^2}}{\sqrt{1 + \left(\frac{f_C}{f_P}\right)^2}} \quad (11)$$

M_C and F_M are terms derived from a thesis by Ridley (see the References section) on current mode control.

$$M_C = 1 + \frac{V_{RAMP\_SLOPE} L1}{V_{IN}} \quad (12)$$

$$F_M = \frac{L1 f_{SW} A_{CS}}{4 M_C V_{IN}} \quad (13)$$

where:

V_{RAMP_SLOPE} and A_{CS} are fixed constants within the chip.
V_{RAMP_SLOPE} = 300000 (ADP5070)
V_{RAMP_SLOPE} = 600000 (ADP5071)
A_{CS} = 0.1538 (ADP5070)
A_{CS} = 0.072 (ADP5071)

POWER COMPONENT STRESS

As is often the case, a 30% ripple in the inductors generally results in a reasonable value (see Equation 15). However, with large step-down ratios, it is more optimal to increase this ripple percentage in the input inductor to 50% or 60%.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \text{ (into each inductor, L1a and L2a)} \quad (14)$$

$$\Delta I_L = 0.3 I_{IN} \quad (15)$$

$$I_{PKL1a} = I_{IN} + \frac{\Delta I_L}{2} \quad (16)$$

$$I_{PKL1b} = I_{OUT} + \frac{\Delta I_L}{2} \quad (17)$$

$$L1 = \frac{V_{IN} \times V_{OUT}}{(V_{IN} + V_{OUT}) f_{SW} \Delta I_L} \quad (18)$$

Figure 4 shows the currents in the FET switch (Q1) and Q2. It also shows the dc components of the switch current. The peak currents depend on the ripple chosen in Equation 15.

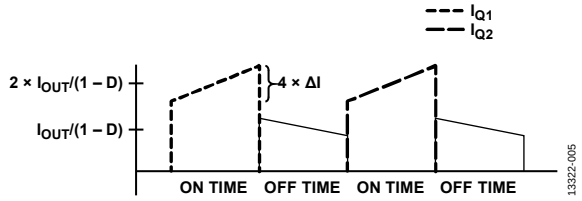

Figure 4. Idealized SEPIC Waveforms

Calculating the switching loss in the primary switch Q1 is beyond the scope of this application note. Note that in many cases, the switching loss can be large because the voltage swing the switch sees is large (~V_{IN} + V_{OUT}) and so are the currents (see Figure 4).

The peak-to-peak output voltage ripple on the output is (ΔV_{RIPPLE_SEPIC}) and is approximated by

$$\Delta V_{RIPPLE\_SEPIC} \approx \frac{I_{OUT} D_{ON}}{f_{SW} C_{OUT1}} + ESR_{C_{OUT1}} \times I_{OUT}(1 - D_{ON}) \quad (19)$$

The value of the current through the capacitor ($I_{RMS\_C_{OUT}\_SEPIC}$) is

$$I_{RMS\_C_{OUT}\_SEPIC} = \frac{I_{OUT} D_{ON}}{(1 - D_{ON})} \sqrt{1 + \left(\frac{1}{3}\right)\left(\frac{\Delta I_L (1 - D_{ON})}{2 I_{OUT}}\right)^2} \quad (20)$$

Choose the ripple on C1 for around 5% of V_{IN}.

$$V_{RIPPLE\_C1} = \frac{(1 - D_{ON}) I_{IN}}{f_{SW} C1} + I_{IN} ESR_{C1} \quad (21)$$

$$V_{RIPPLE\_Cx} = \frac{(1 - D_{ON}) I_{IN}}{f_{SW} C1} + I_{IN} ESR_{C1} \quad (22)$$

It is important to consider I_{RMS} ratings when choosing C1 because the current through it is large.

Because Q2 is a diode, there are several considerations to make when choosing a component. The V_{DS_MAX} must be rated to at least V_{IN} + V_{OUT}. The continuous current must be at least 1/3 the peak current to be seen. As expected, the average current through the diode is I_{OUT}. In addition, the package must be able to handle I_{OUT} in the thermal environment of the application.

OUTPUT FILTER

As dual rail converters, the ADP5070/ADP5071 are typically used for analog power supplies, which often require very low output ripple. The output current of a SEPIC is discontinuous, unlike the input current of a buck converter. This results in a step change in the current into the output capacitors. These switching spikes are not well attenuated even by ceramic capacitors because of their inductance. The ADP5070/ADP5071 have a pin-selectable slew rate. This helps reduce the appearance of switch spikes by slowing down the switch transition. However, it is often necessary to put a small, damped output pi filter on the output of the SEPIC winding.

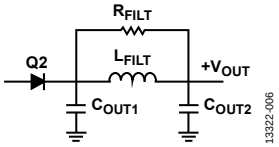

Figure 5. Schematic of the Output Filter

Although this filter affects the small signal model, this issue is not fully discussed in this application note. As long as the damping resistor is chosen according to Equation 23 and Equation 24, and the converter is designed to crossover at a tenth of ω_o or less, no instability is caused by the pi filter.

Choose C_{OUT1} to be around 2% of the output ripple and C_{OUT2} to be at least the value of C_{OUT1}. A good value for L_{FILT} is generally 1 µH; set Q_o to 1.

$$\omega_o = \sqrt{\frac{2(C_{OUT1} + C_{OUT2})}{(L_{FILT} \times C_{OUT1} \times C_{OUT2})}} \quad (23)$$

$$R_{FILT} = \frac{\left(R_{LOAD} L_{FILT}(C_{OUT1} + C_{OUT2}) - \frac{L_{FILT}}{Q_O \omega_O}\right)}{\frac{R_{LOAD}(C_{OUT1} + C_{OUT2})}{Q_O \omega_O} - L_{FILT} C_{OUT1}} \quad (24)$$

$$I_{RMS\_C1} = \sqrt{\frac{(1 - D_{ON})}{3}\left(I_{PKL1a}{}^2 + I_{PKL1a}\left(I_{IN} - \frac{\Delta I_L}{2}\right) + \left(I_{IN} - \frac{\Delta I_L}{2}\right)^2\right) + \left(\frac{D_{ON}}{3}\right)\left(I_{PKL1b}{}^2 + I_{PKL1b}\left(I_{OUT} - \frac{\Delta I_L}{2}\right) + \left(I_{OUT} - \frac{\Delta I_L}{2}\right)^2\right)} \quad (25)$$

ADP5070/ADP5071 DESIGN TOOL

The ADP5070/ADP5071 ADIsimPower™ design tool is a fully integrated Microsoft Excel®-based designer for the ADP5070/ADP5071 devices. For the positive output, the tool automatically chooses a boost or a SEPIC topology. The negative rail always uses the inverting buck boost topology. Once the user has enabled macros (which may require a change of the security settings in Excel), the **Basic Setings** dialog box appears. It can also be found by clicking the **Find Solution** button. In the dialog box, enter the voltages and currents required for the design and choose whether to optimize for cost, loss, or size.

If the **View Solution** button is clicked, the design tool outputs a complete, optimized design. This includes a costed bill of materials (BOM) with compensation values, an accurate, tested efficiency plot across load, a plot of power loss across load, a full load Bode plot, performance parameters, component stresses, and power dissipation for every component. In addition, the **Build Your Design** tab provides the same BOM, but with the components arranged to fit on the blank demo board listed in the BOM and any extra components required to configure the demo board.

Additional customization tools are available in the **Advanced Settings** dialog box. Here, the user can select parameter specifications for output voltage ripple, current, transient response, optional output filter usage, an external undervoltage lockout (UVLO), and more. A more in-depth description of the functionality of these options is provided in the **Program Details** dialog box, available by clicking the **Program Details** button found on the **Basic Settings** dialog box.

Among the most powerful features of this tool are the component buttons found on the **User Interface** tab. This functionality gives the user the ability to change each component individually to fully customize the design.

Each of the components in the drop down list has been preselected from a database of thousands of components to produce a functional design and is sorted according to the optimization chosen in the **Basic Settings** dialog box. The components must be selected in order from top to bottom because there are dependencies between the different components.

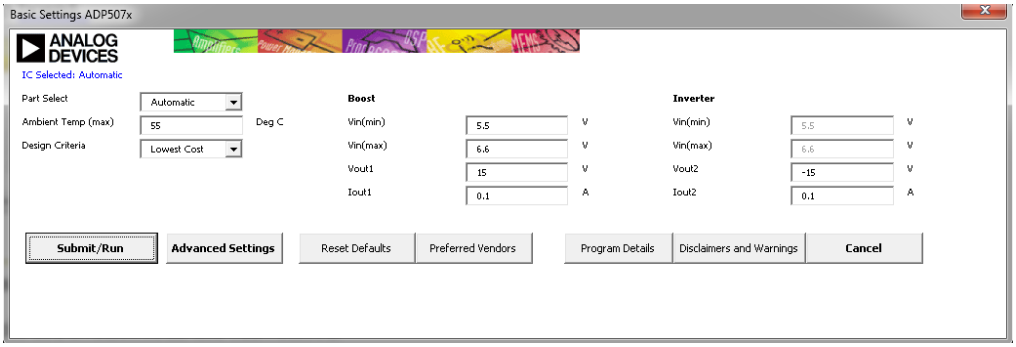

Figure 6. Basic Settings Dialog Box

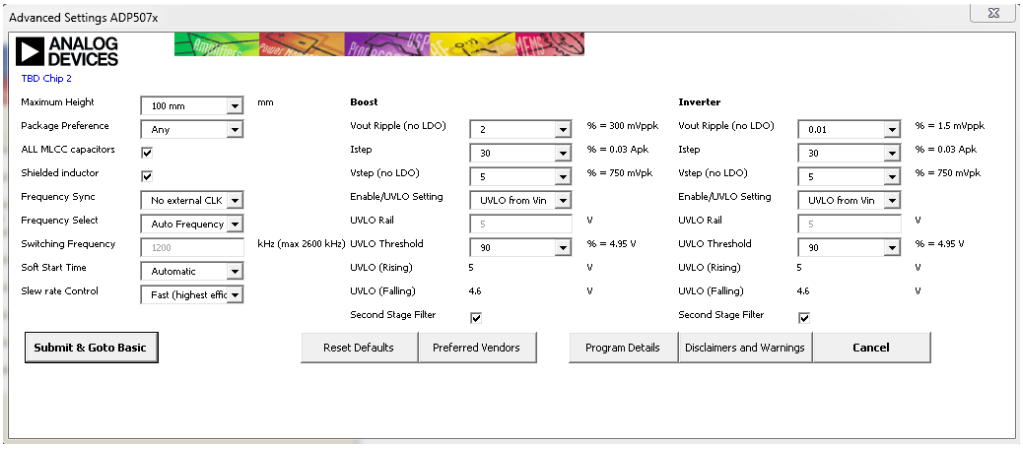

Figure 7. Advanced Settings Dialog Box

CONCLUSION

In conclusion, the ADP5070/ADP5071 devices provide an inexpensive and robust way to create dual rails using only one controller. The ADIsimPower design tool allows complete customization of the design and can be relied on to create robust dual rail designs quickly.

REFERENCES

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Ridley, Dr. Ray. *A New Continuous-Time Model for Current-Mode Control.* Bradenton, FL: Ridley Engineering, 1990.