

Noise Reduction Network for Adjustable Low Dropout Regulators

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INTRODUCTION

Noise is a parameter that is extremely important to designers of high performance analog circuits. This is especially true for high speed clocks, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), voltage controlled oscillators (VCOs), and phase-locked loops (PLLs). The key to reducing the output voltage noise is keeping the ac closed-loop gain close to unity without compromising the ac performance and dc closed-loop gain.

This application note describes how to use a simple RC network to reduce the output noise of an adjustable low dropout regulator (LDO). Experimental data for several LDOs is presented and demonstrates the efficacy of this simple circuit technique. Although noise reduction (NR) is the primary focus of this application note, test data documenting the effect on power supply rejection ratio (PSRR) and transient load response is also shown.

Figure 1 shows a simplified block diagram of a typical adjustable LDO. The output voltage, V_{OUT} , is a function of the reference voltage, V_R , and the dc closed-loop gain of the error amplifier. To derive the output voltage, the reference voltage is multiplied by the dc closed-loop gain. The equation is

$$V_{OUT} = V_R \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where $\left(1 + \frac{R1}{R2}\right)$ is the dc closed-loop gain.

The error amplifier noise, V_N , is also multiplied by the same factor, resulting in an output noise that increases in proportion to the programmed output voltage.

When output voltages are less than a factor of two times the reference voltage, there is only a modest increase in the output noise. This modest increase, however, can be unacceptable for many sensitive applications.

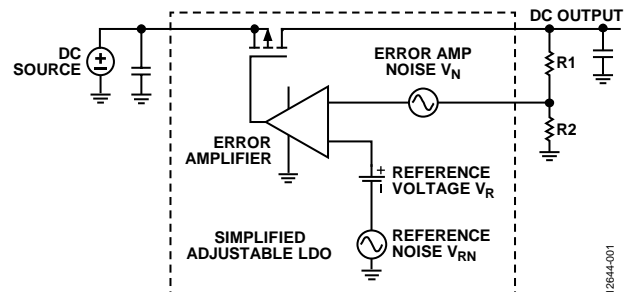


Figure 1. Simplified Adjustable LDO Block Diagram with Internal Noise Source Shown

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REVISION HISTORY

10/14—Revision 0: Initial Version

NOISE IN LDOs

The major sources of intrinsic noise in LDOs are the internal reference voltage and the error amplifier.

Modern LDOs operate with internal bias currents of a few hundred nanoamperes to achieve quiescent currents of 15 μ A or less. These low bias currents require the use of large value bias resistors, up to 1 G Ω in value. Operating at low bias currents results in a noisier error amplifier and noisier reference voltage circuits in comparison to their discrete counterparts.

A typical LDO uses a resistive voltage divider to set the output voltage. Therefore, the ac closed-loop gain is equal to the dc closed-loop gain plus one. The noise gain of the error amplifier is also equal to the ac closed-loop gain.

REDUCING LDO NOISE

There are two major methods for reducing the noise of an LDO.

- Filter the reference
- Reduce the noise gain of the error amplifier

Some LDOs allow the use of an external capacitor to filter the reference. In fact, many ultralow noise LDOs require the use of an external noise reduction capacitor, usually denoted as C_{BYP} in the application schematic, to achieve their low noise specifications. The drawback of only filtering the reference is that the error amplifier noise and any residual reference noise are amplified by the closed-loop gain, resulting in noise that is proportional to the output voltage.

Figure 2 shows the noise spectral density of the ADP125 set to output voltages of 500 mV, 1 V, 2.5 V, and 4 V. The results indicate that the noise increases as the output voltage is increased, which is typical behavior of LDOs with a C_{BYP} capacitor.

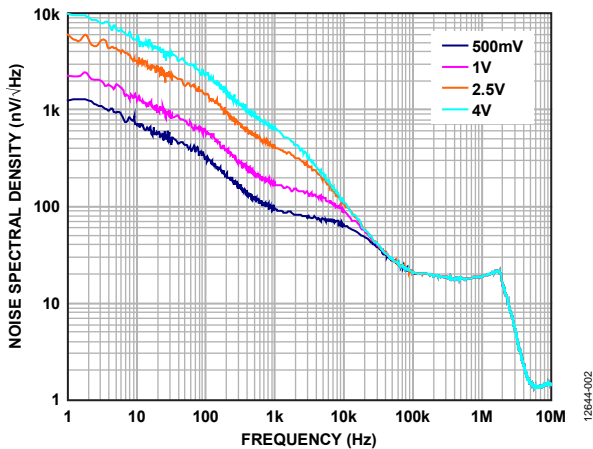


Figure 2. ADP125 Noise Spectral Density for Different Output Voltages

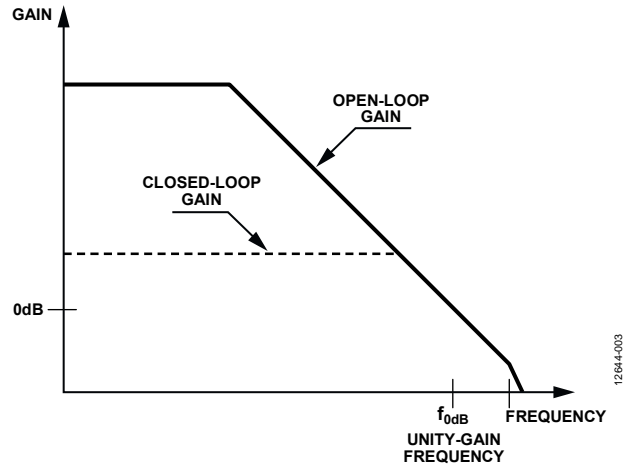


Figure 3. LDO Closed-Loop and Open-Loop Gain Frequency Response

Reducing the noise gain of the error amplifier can result in an LDO whose output noise does not significantly increase with output voltage. Unfortunately, reducing the output noise is generally not possible for fixed output LDOs because there is no access to the feedback node. Fortunately, the feedback node is readily accessible in adjustable output LDOs.

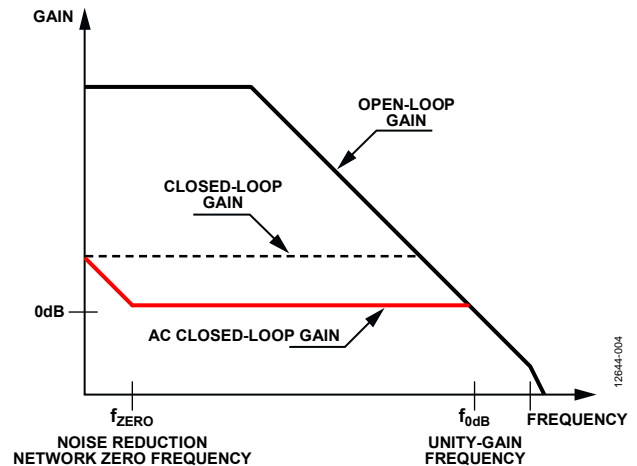


Figure 4. AC Closed-Loop Frequency Response with Noise Reduction Network

Figure 4 compares the ac closed-loop gain of a properly designed noise reduction network with the unmodified closed-loop gain. The ac gain is close to unity for much of the bandwidth of the LDO. As a result, the noise of the reference and error amplifier are amplified to a lesser degree.

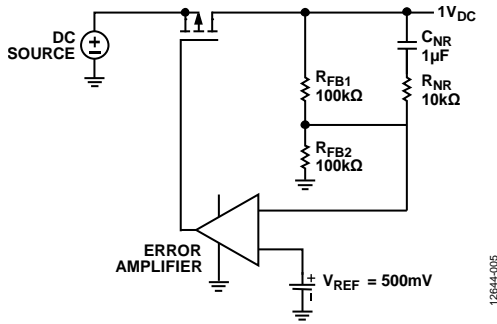


Figure 5. Reducing Noise Gain in an Adjustable LDO

Figure 5 shows a 1 V output adjustable LDO where R_{FB1} and R_{FB2} set the output voltage. Reducing the noise gain of the error amplifier is accomplished with R_{NR} and C_{NR} . Some LDOs have a low phase margin or are not stable at unity gain; therefore, R_{NR} is arbitrarily chosen to set the high frequency gain of the amplifier to approximately 1.1. The value of R_{NR} can be adjusted as needed to ensure that the LDO is stable, although the noise reduction becomes lessened. The value of C_{NR} was chosen to set the low frequency zero of the noise reduction network (which consists of C_{NR} , R_{FB1} , and R_{NR}) below 10 Hz, which ensures that the noise in the $1/f$ region is adequately reduced.

EXAMPLES OF LDO NOISE

Figure 6 to Figure 9 show the output voltage noise of several adjustable LDOs, with and without the noise reduction network. The effect of the noise reduction network on the noise spectral density is evident. In all cases, there is a significant reduction in noise performance between 20 Hz and 10 kHz and even up to 50 kHz for some LDOs.

The noise spectral density of the adjustable LDOs in unity gain is also plotted on the same graphs for comparison. Above the zero created by R_{FB1} and C_{NR} , it is clear that the noise characteristic of the adjustable LDOs with the noise reduction network is almost identical to the LDO in unity gain.

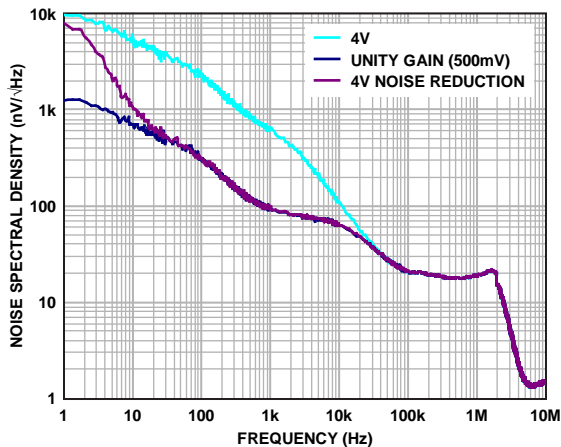


Figure 6. Noise Spectral Density of the ADP125 Adjustable LDO

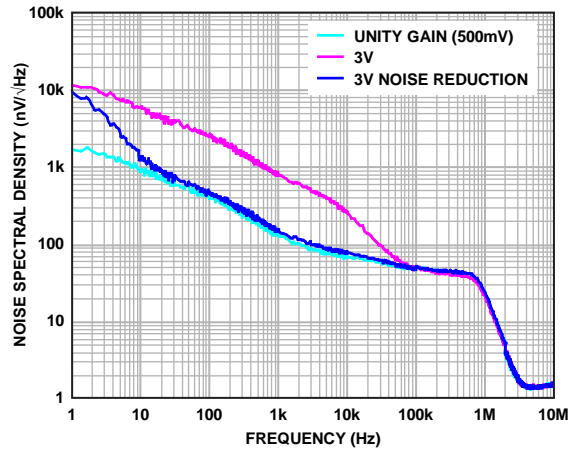


Figure 7. Noise Spectral Density of the ADP171 Adjustable LDO

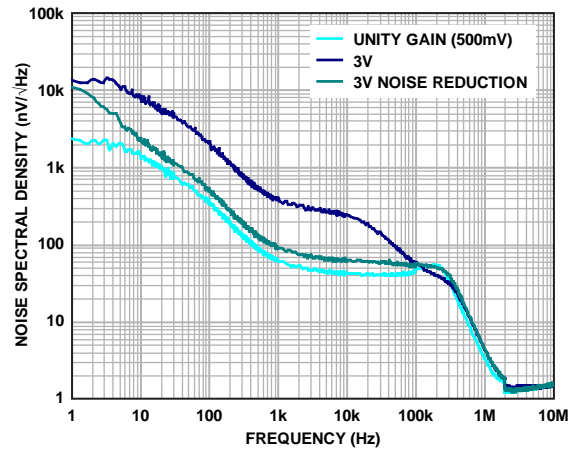


Figure 8. Noise Spectral Density of the ADP1741/ADP1753/ADP1755 Adjustable LDOs

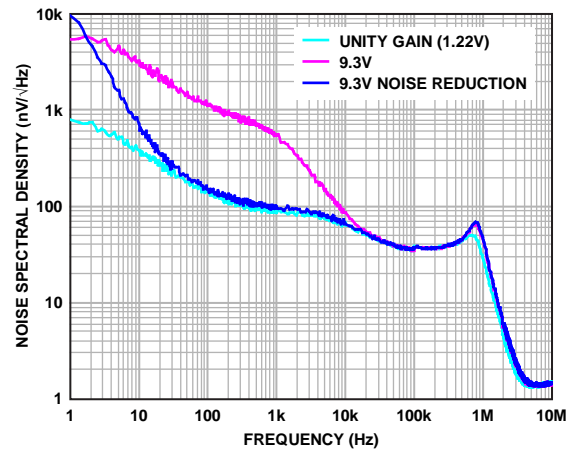


Figure 9. Noise Spectral Density of the ADP7102/ADP7104/ADP7105 Adjustable LDOs

Note that the noise spectral density curves, with and without the noise reduction network, converge above 20 kHz. This is because the closed-loop gain of the error amplifier meets the open-loop characteristic of the amplifier, and no further reduction in noise gain is possible.

NOISE REDUCTION NETWORK

DESIGN EXAMPLE OF USING THE NOISE REDUCTION NETWORK WITH THE ADP7142

Assuming the noise of the ADP7142 is approximately 11 μV , determine the noise of the ADP7142 used in adjustable mode with the following formula:

$$\text{Noise} = 11 \mu\text{V} \times (R_{PAR} + R_{FB2})/R_{FB2} \quad (2)$$

where R_{PAR} is a parallel combination of R_{FB1} and R_{NR} .

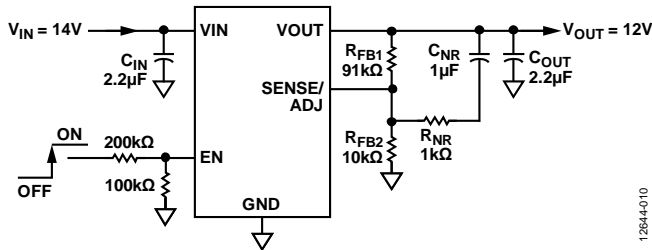


Figure 10. Noise Reduction Modification

Based on the component values shown in Figure 10, the ADP7142 circuit has the following characteristics:

- DC gain of 10 (20 dB)
- 3 dB roll-off frequency of 1.75 Hz
- High frequency ac gain of 1.099 (0.82 dB)
- Theoretical noise reduction factor of 9.1 (19.2 dB)
- Measured rms noise of the adjustable LDO without noise reduction of 70 μV rms
- Measured rms noise of the adjustable LDO with noise reduction of 12 μV rms
- Measured noise reduction of about 15.3 dB

Note that the measured noise reduction is less than the theoretical noise reduction. Figure 11 shows the noise spectral density of an adjustable ADP7142 set to 6 V and 12 V, with and without the noise reduction network. The output noise with the noise reduction network is approximately the same for both voltages, especially for frequencies above 100 Hz.

The noise of the 6 V and 12 V outputs, without the noise reduction network, can differ by a factor that ranges from 2 kHz to approximately 20 kHz. If the noise is above 40 kHz, the closed-loop gain of the error amplifier is limited by its open-loop gain characteristic. Therefore, the noise contribution from

20 kHz to 100 kHz is less than what is expected when the error amplifier has an infinite bandwidth. The noise is also less than what is expected based on the dc gain, which is 70 μV rms vs. 110 μV rms. There is also an improvement in PSRR over the same frequency range (see the Improving PSRR section for more information).

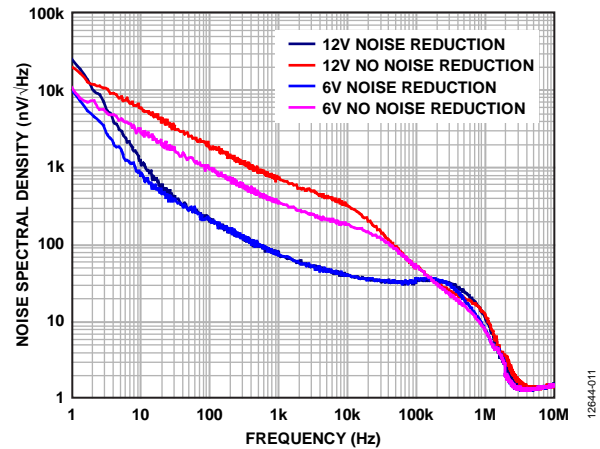


Figure 11. ADP7142 6 V and 12 V Output Voltage with and Without Noise Reduction Network

LDO PSRR

PSRR is a measure of how well a circuit suppresses or rejects extraneous signals (such as noise and ripple) appearing at the power supply input, which keeps these unwanted signals from corrupting the output of the circuit. The PSRR of a circuit is

$$\text{PSRR} = 20 \times \log \left(\frac{V_{E_{IN}}}{V_{E_{OUT}}} \right) \quad (3)$$

where $V_{E_{IN}}$ and $V_{E_{OUT}}$ are the extraneous signals appearing at the input and output, respectively.

For most circuits, such as ADCs, DACs, and amplifiers, this PSRR applies to the pins that supply power to the inner workings of the circuit. However, an LDO input power pin supplies power to the internal circuitry and the load current of the regulated output voltage.

IMPROVING PSRR

Another benefit of using a noise reduction network to reduce the output noise of an adjustable LDO is that the low frequency PSRR of the LDO is also improved. In Figure 5, R_{FB1} , R_{NR} , and C_{NR} form a lead lag network with a zero at approximately $1/(R_{FB1} \times C_{NR})$. It also has a pole at approximately $1/(R_{NR} \times C_{NR})$. The lead lag network acts as a feedforward function in the feedback loop, which improves the PSRR of the LDO. For frequencies below the point where the LDO closed-loop gain and open-loop gain converge, the amount of PSRR improvement, in dB, is approximately

$$20 \times \log \left(1 + \frac{R_{FB1}}{R_{NR}} \right)$$

Figure 12 to Figure 15 show the effect of the noise reduction network on the PSRR of several adjustable LDOs. The PSRR improvement for frequencies that range from 10 Hz to about 20 kHz is between 15 dB and 20 dB. For example, Figure 15 compares the PSRR of a 9 V adjustable LDO, one with the noise reduction network and one without the noise reduction network. For this example, $R_{FB1} = 64 \text{ k}\Omega$, $R_{FB2} = 10 \text{ k}\Omega$, $R_{NR} = 10 \text{ k}\Omega$, and $C_{NR} = 1 \mu\text{F}$. The zero created by R_{FB1} and C_{NR} is about 2.5 Hz and is evident by the improvement in the PSRR that is above 10 Hz. The overall PSRR improvement is about 17 dB, when the frequency ranges from 100 Hz to 1 kHz. The PSRR improvement decreases until about 20 kHz, which is when the LDO open-loop gain and closed-loop gain converge.

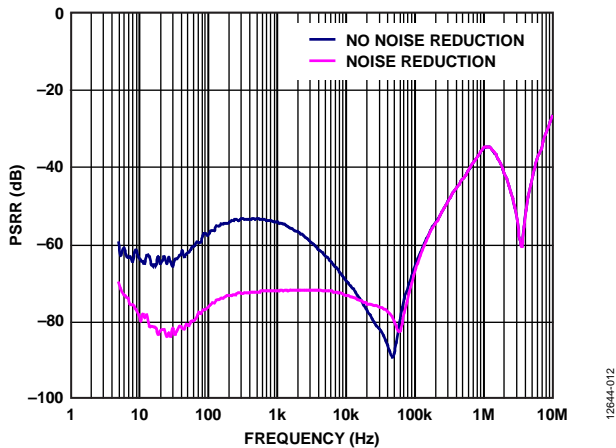


Figure 12. PSRR of the ADP125 Adjustable LDO With and Without a Noise Reduction Network

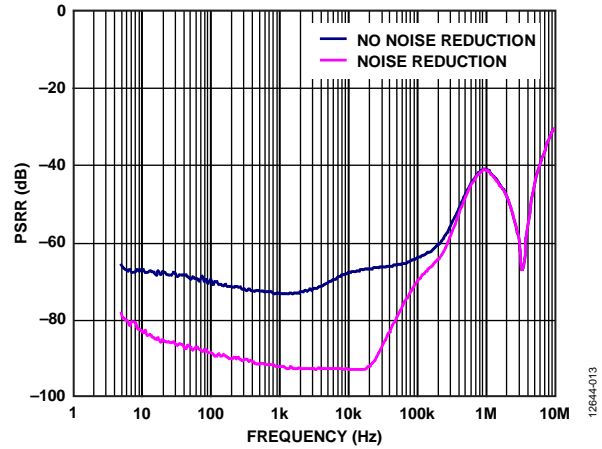


Figure 13. PSRR of the ADP171 Adjustable LDO With and Without a Noise Reduction Network

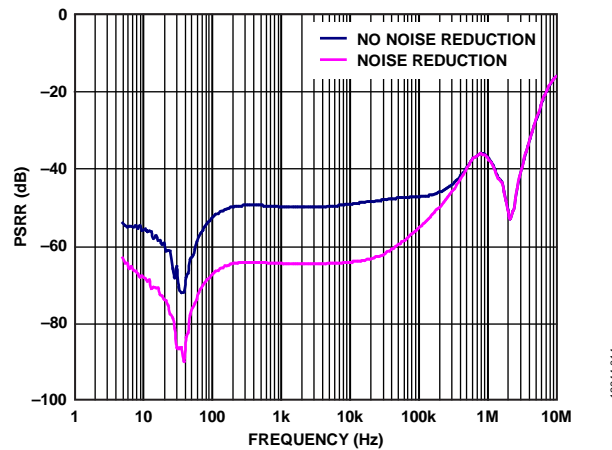


Figure 14. PSRR of the ADP1741/ADP1753/ADP1755 Adjustable LDO With and Without a Noise Reduction Network

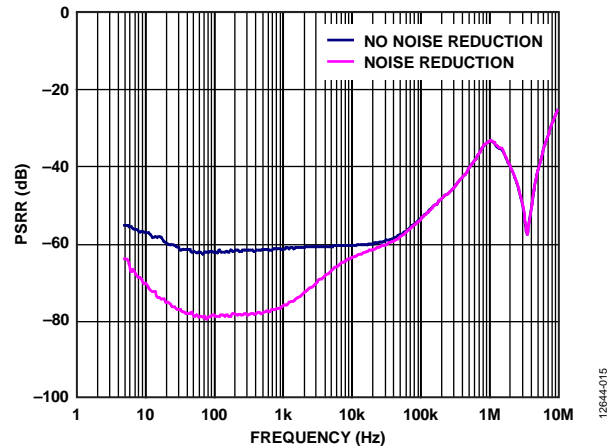


Figure 15. PSRR of ADP7102/ADP7104 Adjustable LDO With and Without a Noise Reduction Network

TRANSIENT LOAD IMPROVEMENT

The noise reduction network can also improve the transient load response of the LDO. Because R_{FB1} , R_{NR} , and C_{NR} (see Figure 5) perform a feedforward function in the feedback loop of the LDO, high frequency components of the transient load are fed to the error amplifier without attenuation. This allows the error amplifier to respond to the transient load quickly. Figure 16 and Figure 17 show the transient load response of an ADP125, with and without the noise reduction network. Figure 17 illustrates that the LDO with the noise reduction network can respond to the transient load in less than 50 μ s as compared to 500 μ s for the LDO without the noise reduction network.

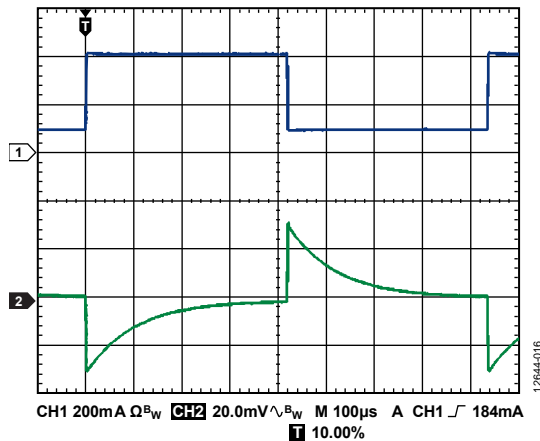


Figure 16. Transient Load Response of an ADP125 Adjustable LDO Without a Noise Reduction Network

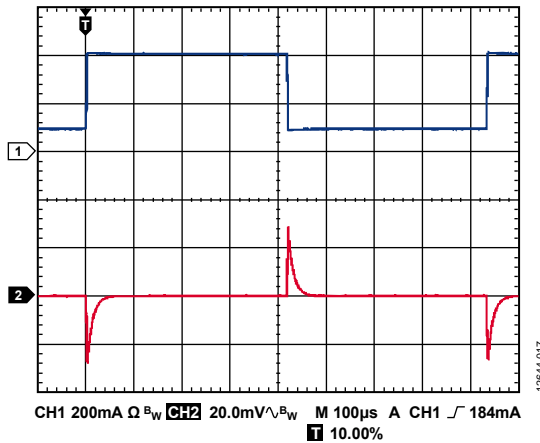


Figure 17. Transient Load Response of an ADP125 Adjustable LDO with a Noise Reduction Network

EFFECT ON START-UP TIME

One drawback to the use of the noise reduction network is that it significantly increases the start-up time of the LDO. Figure 18 to Figure 20 show the start-up time of an ADP125, with and without the noise reduction network. The normal start-up time

is about 600 μ s. Adding a noise reduction network with $C_{NR} = 10$ nF increases the start-up time to 6 ms. With $C_{NR} = 1$ μ F, the start-up time is 600 ms. The increase in the start-up time is not an issue for applications that do not switch the LDO off and on after the circuit is fully powered.

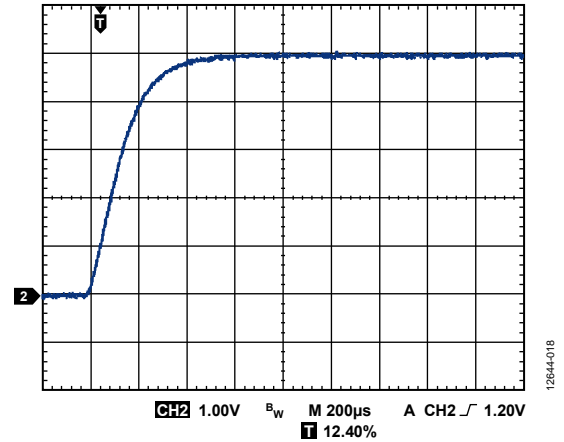


Figure 18. Start-Up Time of the ADP125 Adjustable LDO

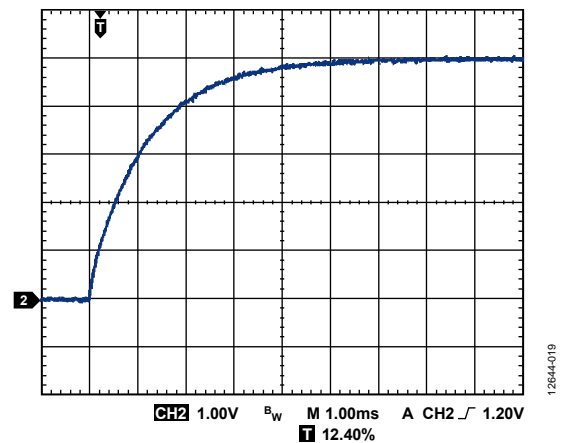


Figure 19. Start-Up Time of the ADP125 Adjustable LDO with a Noise Reduction Network, $C_{NR} = 10$ nF

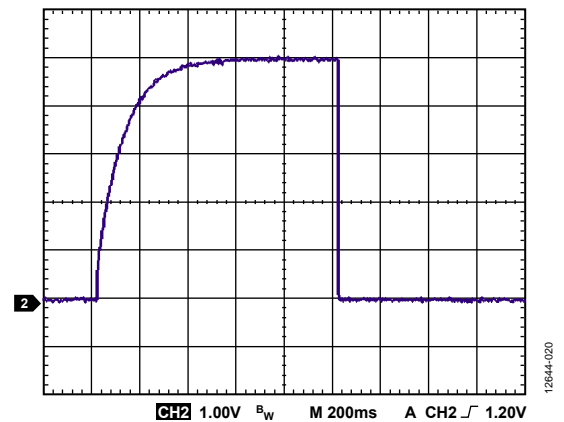


Figure 20. Start-Up Time of the ADP125 Adjustable LDO with a Noise Reduction Network, $C_{NR} = 1$ μ F

SUMMARY

In general, the noise, the PSRR, and the transient load performance of an adjustable LDO can be greatly improved with the addition of a simple RC network. Noise sensitive applications, such as high speed clocks, ADCs, DACs, VCOs, and PLLs, can benefit from the use of adjustable LDOs with an added noise reduction network.

This technique only works for adjustable output voltage LDOs with architectures similar to the one shown in Figure 5. A defining characteristic of this architecture is that the output noise scales with the output voltage. This is evident in Figure 5 because both the reference voltage and the error amplifier noise are increased by the ratio of approximately R1:R2.

Older adjustable LDOs, such as the [ADP123](#), [ADP125](#), [ADP171](#), [ADP223](#), [ADP323](#), [ADP1741](#), [ADP1753](#), [ADP1755](#), [ADP7102](#), [ADP7104](#) and [ADP7105](#), share this general architecture and benefit greatly from the use of a noise reduction network.

Newer LDOs, such as the [ADP7118](#), [ADP7142](#), [ADP7182](#), [ADM7170](#), [ADM7171](#), and [ADM7172](#), share a similar

architecture when used in adjustable mode. However, these LDOs set the error amplifier in unity gain and make the reference voltage equal to the output voltage, which ensures that the output noise is nearly independent of output voltage. When using these LDOs in adjustable mode, it is best to select a fixed output voltage version that is somewhat less than the desired voltage to ensure that the dc gain of the error amplifier is kept as close to unity as possible.

Ultralow noise LDOs, such as the [ADM7150](#), [ADM7151](#), [ADM7154](#), and [ADM7155](#), do not benefit from the use of a noise reduction network. Their architecture places the LDO error amplifier in the unity gain, which means that the reference voltage is equal to the output voltage, much like the newer LDOs mentioned previously. The error amplifier in these designs has very low noise and an internal filter with a pole well below 1 Hz heavily filters the reference voltage. The combination of these two design elements virtually eliminates noise at the output of the LDO.