

Rolling Data Buffer on the **ADF7024**

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INTRODUCTION

When the **ADF7024** receives a packet, it stores the data in a linear sequence in the packet RAM. Prior to transmission, the data to be transmitted is written to the packet RAM in a linear sequence. This functionality is described in the **ADF7024** Reference Manual, UG-698. (The **ADF7024** Reference Manual, UG-698, is included in the **ADF7024** design resource package, which is available for download on the **ADF7024** product page.) The **ADF7024** packet RAM is 240 bytes long. If the packet length is greater than 240 bytes, additional measures are required. This application note describes a method for handling longer packet lengths on the **ADF7024**, up to a maximum length of 65,535 bytes, via a rolling buffer mechanism. This method reuses and renames several registers of the **ADF7024**.

Tx/Rx ROLLING DATA BUFFER

In rolling buffer mode, packet RAM locations Address 0x020 to Address 0x0FF are available for packet data. Packet RAM memory locations Address 0x000 to Address 0x01F are allocated for use by the **ADF7024** and must not be used for packet data. When rolling buffer mode is not enabled, Address 0x000 to Address 0x00F are allocated for use by the **ADF7024**, and Address 0x010 to Address 0x0FF are available for packet data.

ROLLING BUFFER REGISTERS

The registers to enable and configure the rolling buffer mode are outlined in Table 1. When the rolling buffer is enabled via the PKT_TESTMODES register (Address 0x139), the RADIO_PROFILE_18 register to the RADIO_PROFILE_21 register (Address 0x134 to Address 0x137) take on the rolling buffer control mechanism and no longer form part of the radio profile.

ROLLING BUFFER INTERRUPTS

Use the interrupts defined in Table 2 for rolling buffer operation. The normal operation of the INTERRUPT_SWM_RSSI_DET interrupt is not available when rolling buffer mode is enabled because this interrupt is replaced with the INTERRUPT_BUFFER_FULL interrupt. When rolling buffer mode is disabled, the INTERRUPT_SWM_RSSI_DET interrupt is again available and operates as described in the **ADF7024** Reference Manual, UG-698. (The **ADF7024** Reference Manual, UG-698, is included in the **ADF7024** design resource package, which is available for download on the **ADF7024** product page.)

Table 1. Configuration Registers Used by the Rolling Data Buffer Mode in Tx and Rx

Address (Hex)	Register Name with Rolling Buffer Mode Disabled (Normal Operation)	Register Name with Rolling Buffer Mode Enabled	Description
0x124	PKT_TX_BASE_ADR	PKT_TX_BASE_ADR	Start address in the packet RAM for the transmit buffer.
0x125	PKT_RX_BASE_ADR	PKT_RX_BASE_ADR	Start address in the packet RAM for the receive buffer.
0x134	RADIO_PROFILE_18	BB_RX_BUFFER_SIGNAL	Location in the packet RAM for the receive buffer nearly full signal.
0x135	RADIO_PROFILE_19	BB_RX_BUFFER_SIZE	Receive buffer size in bytes.
0x136	RADIO_PROFILE_20	BB_TX_BUFFER_SIGNAL	Location in the packet RAM for the transmit buffer nearly full signal.
0x137	RADIO_PROFILE_21	BB_TX_BUFFER_SIZE	Transmit buffer size in bytes.
0x139	PKT_TESTMODES	PKT_TESTMODES	Enable/disable the transmit and receive rolling buffer mode. See Table 3.

Table 2. Interrupts for Rolling Buffer Operation

Address	Bit	Interrupt Name in Normal Operation	Interrupt Name with Rolling Buffer Mode Enabled	Description
INTERRUPT_MASK_0, Address 0x100 and INTERRUPT_SOURCE_0, Address 0x336	6	INTERRUPT_SWM_RSSI_DET	INTERRUPT_BUFFER_FULL	Asserted in the INTERRUPT_SOURCE_0 register when the receive or transmit buffer is full. To enable this interrupt source and to mirror the interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.
	5	Reserved	INTERRUPT_BUFFER_ALMOST_FULL	Asserted in the INTERRUPT_SOURCE_0 register when the receive or transmit buffer is almost full. To enable this interrupt source and to mirror the interrupt on the IRQ_GP3 pin, set this bit to Logic 1 in the INTERRUPT_MASK_0 register.

Table 3. Address 0x139: PKT_TESTMODES for Use with Rolling Buffer

Bit	Bit Name in Normal Operation	Bit Name with Rolling Buffer Mode Enabled	Description
5	Reserved	ROLLING_BUFFER_PACKET_RX	1 is enable receive rolling buffer. 0 is normal operation.
4	Reserved	PAYLOAD_ONLY_PACKET_TX	1 is enable transmit payload only rolling buffer. 0 is normal operation.

Table 4. Maximum Packet Length Control

Address (Hex)	Name in Normal Operation	Name with Rolling Buffer Mode Enabled	Description
0x014	Available for packet data	TRX_BYTE_LOW	Bits[7:0] of MAX_ROLLING_BUFFER_LEN[15:0], the lower byte of the packet length control register.
0x015	Available for packet data	TRX_BYTE_HIGH	Bits[15:8] of MAX_ROLLING_BUFFER_LEN[15:0], the upper byte of the packet length control register.

ROLLING BUFFER: TRANSMIT MODE

Set Bit 4 of the PKT_TESTMODES register (Address 0x139) to 1 to enable only the payload rolling buffer in transmit mode. This mode allows the user to transmit a packet of up to 65,535 bytes long using a custom packet structure. The maximum transmit length is programmable up to 0xFFFF by setting the MAX_ROLLING_BUFFER_LEN[15:0] value as defined in Table 4, which is defined locally in the packet RAM in the rolling buffer mode.

The number and type of preamble, sync, payload, and cyclic redundancy check (CRC) are no longer bounded by the ADF7024; instead, the ADF7024 transmits what is placed in the transmit buffer. In this mode, the data in the transmit buffer is sent over the air until the MAX_ROLLING_BUFFER_LEN[15:0] number of bytes are sent, or a command is issued.

In transmit mode, the start of the rolling buffer in the packet RAM is set by the PKT_TX_BASE_ADR register. The size of the buffer is set by the BB_TX_BUFFER_SIZE register. The buffer size must not exceed the available packet RAM.

Set the value in the BB_TX_BUFFER_SIGNAL register so that an INTERRUPT_BUFFER_ALMOST_FULL interrupt is generated prior to the transmission of all the data in the buffer. Typically, the BB_TX_BUFFER_SIGNAL register is set so that the interrupt is asserted when half the data in the buffer is transmitted.

When an INTERRUPT_BUFFER_ALMOST_FULL interrupt is asserted, the host processor writes new data to the packet RAM, starting at the address value PKT_TX_BASE_ADR and ending at the address value, PKT_TX_BASE_ADR + BB_TX_BUFFER_SIGNAL.

When the data in the last byte of the transmit buffer is transmitted, the ADF7024 continues transmitting, starting with the data pointed to by the PKT_TX_BASE_ADR register. If enabled, an INTERRUPT_BUFFER_FULL interrupt is asserted when the last byte in the buffer is transmitted.

When an INTERRUPT_BUFFER_FULL interrupt is asserted, the host processor must write new data to the packet RAM, starting at the address value, PKT_TX_BASE_ADR + BB_TX_BUFFER_SIGNAL + 1, and finishing at the address value, PKT_TX_BASE_ADR + BB_TX_BUFFER_SIZE.

Transmission of data continues until the MAX_ROLLING_BUFFER_LEN[15:0] number of bytes are sent (TX_EOF), or the user issues the CMD_PHY_ON command.

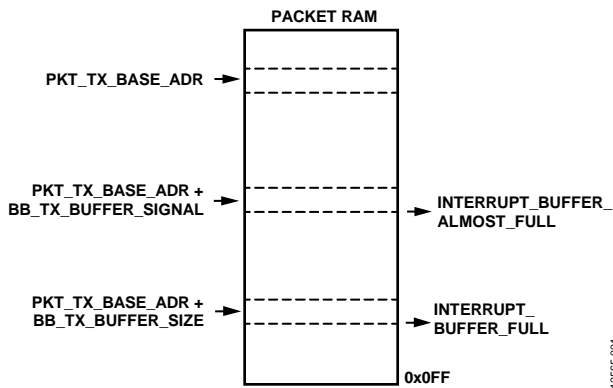


Figure 1. Rolling Buffer in Transmit Mode

ROLLING BUFFER: RECEIVE MODE

Set Bit 5 of the PKT_TESTMODES register (Address 0x139) to 1 to enable the rolling buffer in receive mode. The ADF7024 can receive packet lengths up to $2^{16} - 1$ bytes long (65,535 bytes) via the rolling buffer mechanism. The maximum packet length is programmable up to 0xFFFF by setting the MAX_ROLLING_BUFFER_LEN[15:0] value as defined in Table 4.

When Bit 5 of the PKT_TESTMODES register (Address 0x139) is set and the sync word is received, the packet handler uses the rolling buffer to capture the remainder of the packet.

In receive mode, the PKT_RX_BASE_ADR register sets the address pointer for the start of the rolling buffer in the packet RAM. Set the size of the buffer using the BB_RX_BUFFER_SIZE register. The buffer size must not exceed the available packet RAM size. When the value in the BB_RX_BUFFER_SIZE register is added to the address in the PKT_RX_BASE_ADR register, it must not exceed 0x0FF.

Set the value in the BB_RX_BUFFER_SIGNAL register so that an INTERRUPT_BUFFER_ALMOST_FULL interrupt is asserted prior to the buffer being filled by the received data. Typically, the BB_RX_BUFFER_SIGNAL register is set so the interrupt is asserted when half the buffer is filled with received data.

When an INTERRUPT_BUFFER_ALMOST_FULL interrupt is asserted, the host processor reads the data from the packet RAM, starting at the address value PKT_RX_BASE_ADR and ending at the address value, PKT_RX_BASE_ADR + BB_RX_BUFFER_SIGNAL.

When the last byte of the receive buffer is filled, the ADF7024 continues to write the received data, starting at the address value PKT_RX_BASE_ADR. If enabled, an INTERRUPT_BUFFER_FULL interrupt is asserted when the buffer is filled.

When an INTERRUPT_BUFFER_FULL interrupt is asserted, the host processor must read the data from the packet RAM, starting at the address value, PKT_RX_BASE_ADR + BB_RX_BUFFER_SIGNAL + 1, and ending at the address value, PKT_RX_BASE_ADR + BB_RX_BUFFER_SIZE.

Reception of data continues until the length programmed in the MAX_ROLLING_BUFFER_LEN[15:0] value is achieved (RX_EOF), or the host processor issues the CMD_PHY_ON command.

Note that it is up to the host processor to detect the end of the payload and perform an error checking operation on the data, such as CRC.

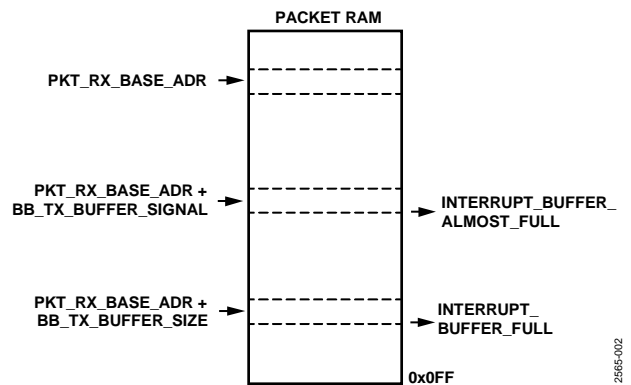


Figure 2. Rolling Buffer in Receive Mode