AN-1291
APPLICATION NOTE

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Digital Potentiometers: Frequently Asked Questions

INTRODUCTION

This application note answers a series of frequently asked questions (FAQs) about digital potentiometer products from Analog Devices, Inc. It includes general and specific questions, including product specific questions. In addition, it provides digital potentiometer configuration information.

Q: What is a digital potentiometer?

A: A digital potentiometer is a digitally controlled resistor that changes the impedance between the terminals and the wiper depending on the code loaded in the RDAC register. Digital potentiometers avoid the problems that mechanical potentiometers face, such as physical size and wear and tear, as well as sensitivity to vibration, temperature, and humidity. A digital potentiometer can be configured in two different modes: potentiometer mode and rheostat mode.

Potentiometer mode (see Figure 1) has three terminals: Terminal A, Terminal B, and Terminal W (wiper).

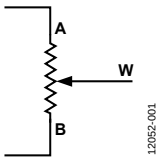

Figure 1. Potentiometer Mode

Rheostat mode has Terminal W hardwired to either Terminal A or Terminal B (see Figure 2). Some devices offer only two terminals: Terminal A and Terminal W.

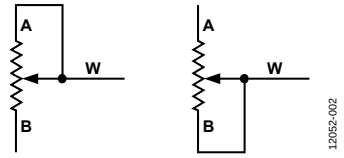

Figure 2. Rheostat Mode

Q: Where do I find the evaluation tools and software pertaining to the evaluation board?

A: The Windows®-compatible evaluation software and the driver software are included on a CD that comes with the evaluation board kit. For newer products, the evaluation software and the driver software information is available on the product page of the Analog Devices website.

Q: How can I obtain digital potentiometer technical support?

A: EngineerZone is an Analog Devices online support community with support for the digital potentiometer available in the Precision DACs community. Customers from all over the world can post questions, view existing questions and answers, and review and contribute to ongoing discussions in this community.

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REVISION HISTORY

3/15—Rev. 0 to Rev. A

Updated Layout ..... Universal
Changes to Introduction Section 1
Changes to General FAQs Section 3
Changes to FAQs About Digital Potentiometers with EEPROM Memory Section 7
Changed Applications Information Section to Circuit References Section 8
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Changes to Multiple Devices on One I^2C Bus Section, Level Shifting for Bidirectional Interface Section, and Gain Section 12
Changes to Linear Gain Setting Mode Section 13
Deleted Bipolar Programmable Gain Amplifier Section, Figure 18, and Table 3; Renumbered Sequentially 13
Changed Voltage to Current Conversion: Programmable Current Source Section to Programmable Current Source Section 14
Changes to Programmable Current Source Section and Figure 21 14
Changed Voltage to Current Conversion: Programmable Bidirectional Current Source Section to Programmable Bidirectional Current Source Section 15
Changes to Programmable Bidirectional Current Source Section and Programmable Low-Pass Filter Section 15
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Changed Miscellaneous Section to Other Usage Examples Section 17
Changes to Programmable Oscillator Section 17

5/14—Revision 0: Initial Version

DIGITAL POTENTIOMETER FAQs BY CATEGORY

GENERAL FAQs

Q: Is there a recommended power-up sequence?

A: Yes. The relevant product data sheet provides a recommended start-up sequence to refer to before powering up the device.

Generally, it is good practice to power the V_{DD} pin first and the V_{SS} pin second. The order of the voltages at Terminal A, Terminal B, and Terminal W (V_A, V_B, and V_W, respectively) is not important, but power these last.

There are ESD protection diodes between the V_{DD} pin and Terminal A, Terminal B, and Terminal W. For example, the cathode of one of the diodes connects to the V_{DD} pin and the anode connects to Terminal A. As a result, any voltage occurring at Terminal A before the V_{DD} pin forward biases the diode and powers the V_{DD} pin.

For some of the digital potentiometers, power the digital signals after the V_{DD} pin. This power sequence is documented in the relevant product data sheet.

Q: Are all digital potentiometers limited to |5 V|?

A: No. A wide portfolio of digital potentiometers are available to handle large unipolar and bipolar power supplies. See the Choosing the Correct digiPot for Your Application online brochure for an up to date product list.

Q: Do digital potentiometers handle bipolar and ac operations?

A: Yes. Analog Devices offers digital potentiometers with dual ±2.5 V, ±5 V, or ±15 V supplies that can handle bipolar or ac operation. The user can still achieve ac operation with a single dc supply by raising the dc offset. Terminal A, Terminal B, and Terminal W have no polarity constraints with respect to one another.

Q: For dual-supply digital potentiometers, if V_{DD} and V_{SS} are +2.5 V and −2.5 V, respectively, can digital inputs be fed from a standard 3.3 V complementary metal-oxide semiconductor (CMOS) logic component without logic level translation? What are the logic level thresholds when V_{DD} is +2.5 V and V_{SS} is −2.5 V?

A: When using a bipolar ±2.5 V digital potentiometer, the maximum digital supply is limited to V_{DD} + 0.3 V or V_{LOGIC} + 0.3 V. Otherwise, the internal protection diodes clamp the voltage and are damaged. See the relevant product data sheet for more details on digital potentiometer levels.

Q: Is there a dependency between the logic level and power consumption?

A: Yes. If the logic level is lower than the logic supply (V_{DD} or V_{LOGIC}, if available), the input gates do not switch completely and the device consumes more power.

Q: Why replace a mechanical potentiometer with a digital potentiometer?

A: There are a few advantages to using a digital potentiometer vs. a mechanical potentiometer, namely

- Higher resolution
- More reliability
- Better stability
- Faster adjustment
- More functions
- Better dynamic control

However, a digital potentiometer is not a direct replacement for a mechanical potentiometer. See the Is a digital potentiometer a real replacement for a mechanical potentiometer, or are there restrictions regarding voltage potentials? question for more information.

Q: Is a digital potentiometer a real replacement for a mechanical potentiometer or are there restrictions regarding voltage potentials?

A: A digital potentiometer is not an exact replacement for a mechanical potentiometer. V_A and V_B must not be greater than V_{DD} or less than V_{SS} (or GND if the device does not have a V_{SS} pin). For example, if the desired V_A and V_B are +2 V and −2 V, respectively, V_{DD} must be less than, or equal to, +2 V, and V_{SS} must be greater than, or equal to, −2 V.

See the AN-1121 Application Note, *Replacing Mechanical Potentiometers with Digital Potentiometers*, for more information on this topic.

Q: For digital potentiometers without nonvolatile memory, what is the state during power-up?

A: Most Analog Devices digital potentiometers (with the notable exception of the AD8400/AD8402/AD8403) contain power-on reset (POR) circuitry, which presets the wiper to terminal resistance to the middle value of the terminal to terminal resistance. For example, if the end to end resistance (R_{AB}) = 10 kΩ, at power-up, R_{WB} = R_{WA} = 5 kΩ, where R_{WB} is the resistance between Terminal W and Terminal B and R_{WA} is the resistance between Terminal W and Terminal A. For the digital potentiometers that do not have this feature, the wiper to terminal resistance can be anything at power-up. See the relevant product data sheet for more details.

Q: Is there a particularly low power digital potentiometer?

A: Yes. The AD5165 is an Analog Devices product that offers ultralow power consumption. The Choosing the Correct digiPot for Your Application online brochure provides an up to date product list.

Q: Does the memory allow the device to return to the last stored value without an update from a microprocessor?

A: Yes. The device is automatically set to the previously stored value each time the device is powered on. By default, the EEPROM is factory programmed to midscale.

Q: How good is the resistance matching between Channel 1 (Ch1) and Channel 2 (Ch2) in a dual digital potentiometer?

A: The matching is typically within 0.1% to 0.2% and ±1% is specified as a maximum mismatch. See the relevant product data sheet for more information.

Q: How is the resistance matching, device to device?

A: Assuming the devices come from the same batch, the resistance matching, device to device, is within ±1%.

Q: What is the resistance tolerance of digital potentiometers?

A: See the relevant product data sheet for an exact figure. If using the potentiometer in the 3-terminal potentiometer mode (without any series resistor), the tolerance is irrelevant because the resistances, R_{WA} and R_{WB}, are ratiometric. If using the potentiometer in the 2-terminal rheostat mode, account for the worst-case variation.

On some nonvolatile digital potentiometers, resistance tolerance is stored in the memory at the factory with an accuracy of 0.1%. Thus, users can retrieve the resistance tolerance and calibrate the system accordingly.

Q: Can I cascade, serialize, or parallel multiple digital potentiometers to get the resistance or resolution needed? My requirement is for a 250 Ω digital potentiometer with approximately 1 Ω per step. I plan to use four 1 kΩ AD8403 devices in parallel with each set to nominally the same value.

A: Yes. See the AN-582 Application Note, *Resolution Enhancements of Digital Potentiometers with Multiple Devices*, for more information.

Q: How is a digital potentiometer designed? How ideal are the wiper switches?

A: A digital potentiometer is purely a CMOS device. All switches are large, CMOS transmission gates operated in the linear region to yield low, uniform on resistance of the CMOS ($R_{DS(ON)}$). All resistor elements are polysilicon or thin film resistors.

Q: What is the temperature coefficient (TC) of the digital potentiometer?

A: Two components make up the resistance at any given setting: the polysilicon or thin film resistors (step resistor, R_S), and the CMOS switch resistor (R_{SW} = 50 Ω at 5 V supply). Together, these components add up such that

$$R_{WB} = R_S + R_{SW}$$

$$R_S = \frac{R_{AB}}{2^N}$$

where N is the number of bits of the digital potentiometer.

The TC of the step resistor, which is published in the relevant product data sheet, is typically −35 ppm/°C for thin film resistors or 600 ppm/°C for polysilicon. The resistance of the switch, on the other hand, doubles at 100°C. As a result, the overall TC is nonlinear and it is worse off at low value codes where the switch resistance dominates. See the TC graphs in the relevant product data sheet for more detailed information.

Q: What is the maximum current I can force into the digital potentiometer?

A: The maximum current is limited by three boundaries at a given resistance setting. The three boundaries are the maximum applied voltage across any two of Terminal A, Terminal B, or Terminal W, the power dissipation of the package, and the maximum current handling capabilities of the internal switches.

Each digital potentiometer data sheet refers to this maximum current in the Absolute Maximum Ratings section (see Table 1 for an example).

Table 1. Maximum Current Through Digital Potentiometer Terminal: Absolute Maximum Ratings Table Example

Parameter	Rating
I_A, I_B, I_W	
Pulsed	
Frequency > 10 kHz	
R_{AW} = 5 kΩ and 10 kΩ	±6 mA/d[1]
R_{AW} = 80 kΩ	±1.5 mA/d[1]
Frequency ≤ 10 kHz	
R_{AW} = 5 kΩ and 10 kΩ	±6 mA/√d[1]
R_{AW} = 80 kΩ	±1.5 mA/√d[1]
Continuous	
R_{AW} = 5 kΩ and 10 kΩ	±6 mA
R_{AW} = 80 kΩ	±1.5 mA

[1] Note that d is the pulse duty factor.

Calculating the pulsed current is dependent on the frequency. If the frequency is less than or equal to 10 kHz, the formula is as follows:

$$I_D = I_{PEAK} \times \sqrt{d}$$

where:
I_D is the maximum dc current.
I_{PEAK} is the maximum peak current value for waveform.
d is the duty factor (0.1 = 10% duty cycle).

If the frequency is greater than 10 kHz, the formula is as follows:

$$I_D = I_{PEAK} \times d$$

Q: Do Analog Devices digital potentiometers suffer from leakage currents, which could affect the gain of the circuit?

A: Analog Devices digital potentiometers are manufactured with a very low leakage analog switch process, which results in low leakage currents. Digital potentiometers are usually specified with a typical common-mode leakage current of 1 nA.

Q: Regarding the specification on resistor differential nonlinearity (R-DNL), I am concerned only with relative adjustments. What if I am not concerned with the actual value of the resistor in the digital potentiometer, but need it to be monotonic?

A: For a digital potentiometer that is in rheostat mode, there are two specifications known as resistor integral nonlinearity (R-INL) and R-DNL, respectively. INL is the maximum deviation between the ideal output of a digital-to-analog converter (DAC) and the actual output level. R-INL is the deviation from an ideal value measured between the maximum resistance wiper position and the minimum resistance wiper position. DNL is the maximum deviation between two consecutive codes over the DAC transfer function. R-DNL measures the relative step change from the ideal between successive tap positions.

All Analog Devices digital potentiometers are guaranteed monotonic.

Q: Is there analog crosstalk between Ch1 and Ch2 of a dual digital potentiometer such that a sine wave applied to Ch1 occurs in Ch2 as well?

A: Yes. The relevant product data sheet details such performance. The performance is typically specified at −70 dB. Figure 3 is an example of analog crosstalk.

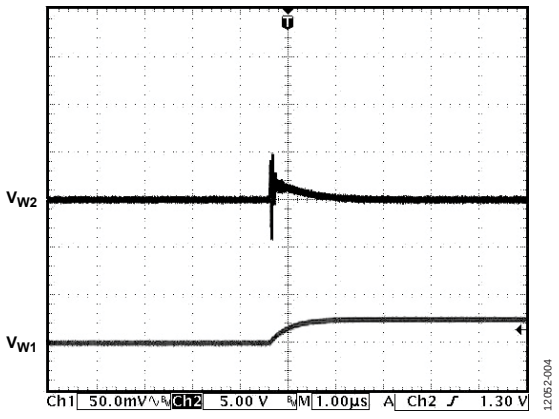


Figure 3. Analog Crosstalk

Q: If Ch1 is programmed from zero to full scale, should the user expect Ch2 to be disturbed?

A: This process is digital step response crosstalk, which is different from analog crosstalk, and the relevant product data sheet details this information. Digital step response crosstalk is typically in the range of 5 nV/sec to 10 nV/sec. Figure 4 shows an example of digital crosstalk.

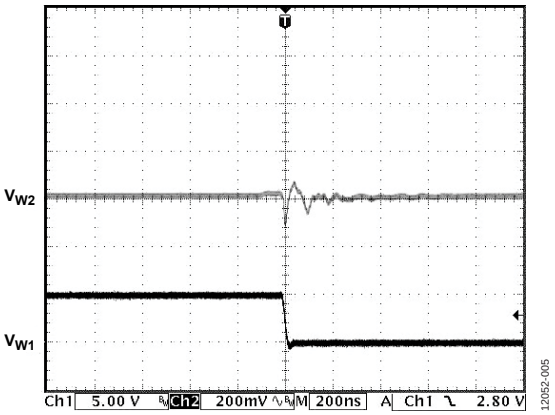


Figure 4. Digital Step Response Crosstalk

Q: What is digital feedthrough?

A: Digital feedthrough is the amount of noise from clock or data coupled into the output. It is usually very small (low nV/sec range). Figure 5 shows an example of digital feedthrough.

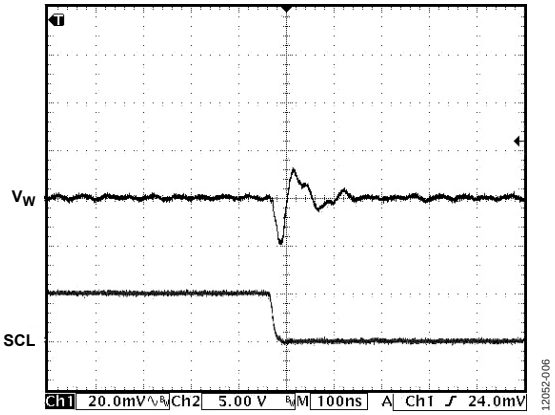


Figure 5. Digital Feedthrough

Q: How is the total harmonic distortion (THD) performance of the digital potentiometer?

A: THD performance is dependent on both code and V_{DD}. Typically, THD performance is in the range of −86.02 dB to −60 dB, but see the relevant product data sheet for specific performance. The best THD performance is achieved when the device operates at its maximum operating voltage. THD is also dependent on the end to end resistance. A higher end to end resistance yields better THD values, but reduces the −3 dB bandwidth. See the dynamic characteristics in the relevant product data sheet for more information.

Q: How can I control a digital potentiometer that requires a 6-bit word length using an 8-bit word length from my controller?

A: Serial peripheral interface (SPI) digital potentiometers operate by disregarding the first MSBs and reading the next six bits. See the relevant product data sheet for more information.

Q: How can I control a digital potentiometer that requires a 12-bit word length using an 8-bit word length from my controller?

A: Issue a 2-byte word. The first four MSBs are disregarded. See the relevant product data sheet for more information.

Q: How can multiple digital potentiometers be daisy-chained?

A: To daisy-chain digital potentiometers, the SDO pin of one package must be tied to the SDI pin of the next package. The clock period may need to be increased due to propagation delay.

In Figure 6, two AD5122/AD5142 digital potentiometers (U1 and U2) are tied together. In this setup, 32 bits are required. The first 16 bits are sent to U2 and the second 16 bits are sent to U1. During this 32-bit write, the $\overline{\text{SYNC}}$ pin remains low.

After all bits are clocked in, the $\overline{\text{SYNC}}$ pin is pulled high to complete the write. The AD5144 and similar SPI devices include internal counters to prevent data corruption due to noise. If the number of clocks is different from expected, the data is ignored. When the $\overline{\text{SYNC}}$ pin is high, the counter resets. See the relevant product data sheet for more information.

Q: Can I program two channels of a multichannel digital potentiometer at the same time?

A: Yes. With some digital potentiometers, such as the AD5251/AD5252/AD5253/AD5254 and the AD5232/AD5233/AD5235, the user can increment and decrement all the channels simultaneously. In addition, the user can write to each electronically erasable memory (EEMEM) and then issue a reset command to update all the RDAC register settings simultaneously.

Some products, such as the AD5144, include an $\overline{\text{LRDAC}}$ pin (for loading the RDAC input register), which transfers data from the input register to the RDAC register and updates the wiper position. A user can update either a single RDAC register or all RDAC registers at once.

Q: Can the wiper setting of digital potentiometers be read back? How about the contents of two RDAC registers of dual I²C-compatible digital potentiometers, such as the AD5242 and AD5282?

A: Yes. The user can read back the wiper setting with some digital potentiometers.

The user can also read back the RDAC register content (the RDAC address value of a specific channel); however, the user can only read the RDAC channel selected during the previous write mode. If the channel the user wants to read is different from the channel previously written to, a dummy write command is necessary to select the desired channel. Refer to the relevant product data sheet for details.

Q: Is there a digital potentiometer controlled by a parallel input?

A: No.

Q: What are the $\overline{\text{WP}}$ pin, the $\overline{\text{PR}}$ pin, and the RDY pin features?

A: The $\overline{\text{WP}}$ pin stands for write protect. For example, on the ADN2850, the $\overline{\text{WP}}$ pin disables any changes to the scratchpad register contents. A scratchpad register directly controls the digital resistor wiper and has no limit on the number of changes it can make (unlike the EEPROM, which has a limit on the number of writes).

However, commands that restore the wiper position using the EEPROM are allowed. Therefore, the $\overline{\text{WP}}$ pin is used as a method of protecting the EEPROM contents.

In addition, on the ADN2850, the hardware override preset ($\overline{\text{PR}}$) pin can be used to overwrite the scratchpad register with the EEPROM contents.

The RDY pin signifies when commands have been completed, thus indicating readiness for the next command.

See the relevant product data sheet for more information.

Q: What is the ESD rating of digital potentiometers?

A: All digital potentiometers have ESD ratings higher than 1 kV. See the relevant product data sheet for more information.

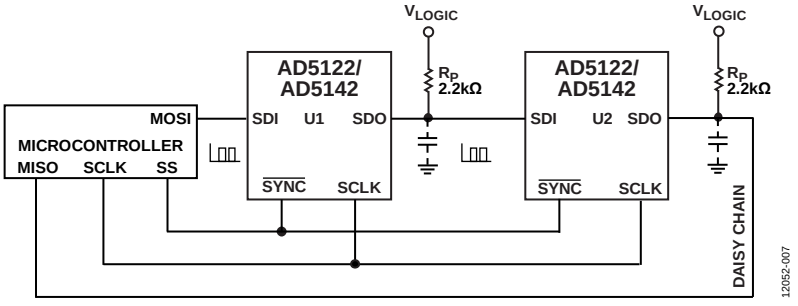


Figure 6. Daisy-Chaining Digital Potentiometers

Q: How can I determine the R_{AB} value on the digital potentiometer package?

A: The ordering guide section of each data sheet includes a model number and, for smaller packages, a branding code. For example, the AD8400 uses an SOIC package, which is branded with AD8400AR1, AD8400AR10, or AD8400AR100, and represents an R_{AB} of 1 kΩ, 10 kΩ, or 100 kΩ, respectively. With the more compact packages, three letter codes are used. Using the branding code in the relevant data sheet helps determine the R_{AB}.

FAQs ABOUT DIGITAL POTENTIOMETERS WITH EEPROM MEMORY

Q: Will the data in the EEMEM need to be refreshed after 15 years when it is operated at 55°C?

A: Yes. The EEPROM cells lose their charge over a period of 15 years when operating at 55°C.

Measured as retention time, the discharge is extrapolated using a model defined in the "Experimental and Theoretical Investigation of Nonvolatile Memory Data-Retention" IEEE article.

$$t_R = t_0 \times e^{\frac{E_a}{kT}}$$

where:
t_R is retention time based on temperature.
t_0 is retention time corresponding to an infinite temperature.
E_a is activation energy.
k is Boltzmann's constant.
T is temperature.

For other operating temperatures, see Figure 7.

As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit before data retention is characterized. This cycling means that the Flash/EE memory is guaranteed to retain its data for its fully specified retention lifetime every time the Flash/EE memory is reprogrammed. Note that retention lifetime, based on an activation energy of 0.7 eV, derates with T_J. This data applies to all nonvolatile memory digital potentiometers.

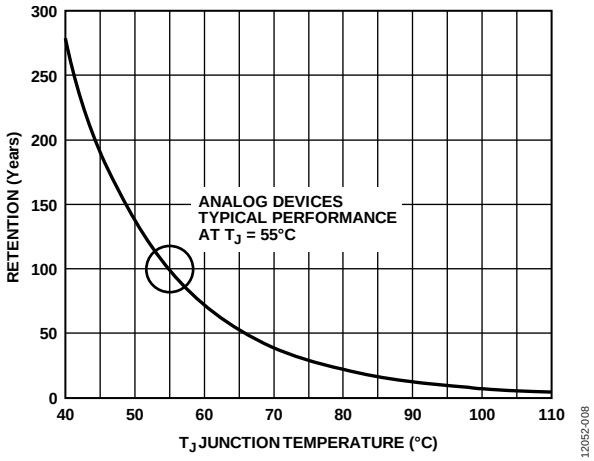


Figure 7. Example of Data Retention vs. Temperature

Q: After the specified EEMEM data retention timeout period, can the power be turned off and then back on so that the device is considered refreshed?

A: No. Doing so refreshes only the RDAC register, not the EEPROM. The data must be reloaded again after 15 years to put a fresh charge into the EEPROM cell. The data is reloaded by writing the RDAC wiper register data back to the EEPROM before the end of 15 years.

Q: Why is the maximum operating temperature for some digital potentiometers only 85°C instead of the standard 125°C?

A: Digital potentiometers that contain EEPROMs have a maximum operating temperature of up to 85°C because EEPROMs are guaranteed to safely operate below 85°C only.

CIRCUIT REFERENCES

AUDIO

Q: If I use the digital potentiometer in audio volume control, will I experience zipper noise?

A: There is noticeable zipper noise; however, a logarithmic audio volume control circuit with glitch reduction (developed by Analog Devices using the AD5292 digital potentiometer) is available (see Figure 8). See the AN-1209 Application Note, *Logarithmic Audio Volume Control with Glitch Reduction Using the AD5292 Digital Potentiometer* for more information.

Q: Can digital potentiometers do log taper adjustments?

A: Pseudolog taper adjustment is preferred in applications such as audio control. The answer, however, is yes for AD5231/AD5232/AD5233/AD5235 or ADN2850 users. Additionally, a pseudolog taper adjustment is possible in other linear adjustment potentiometers with a simple configuration. For more information, see the "Tack a Log Taper onto a Digital Potentiometer" EDN Network article published by Hank Zumbahlen in January 2000.

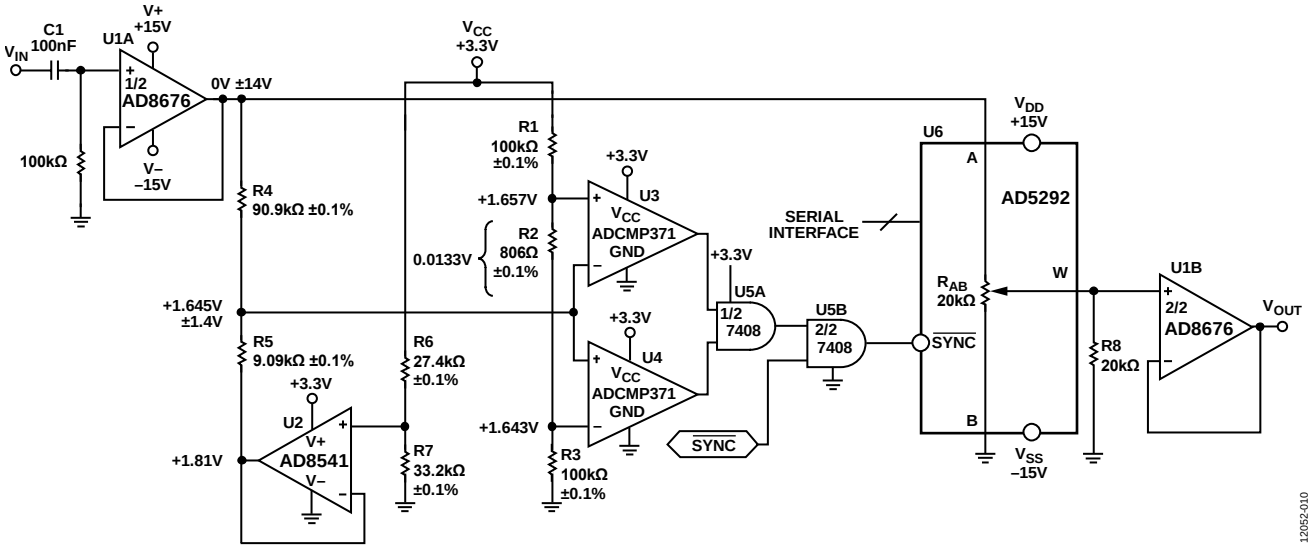


Figure 8. Logarithmic Audio Volume Control with Glitch Reduction (Simplified Schematic: Decoupling; All Connections Not Shown)

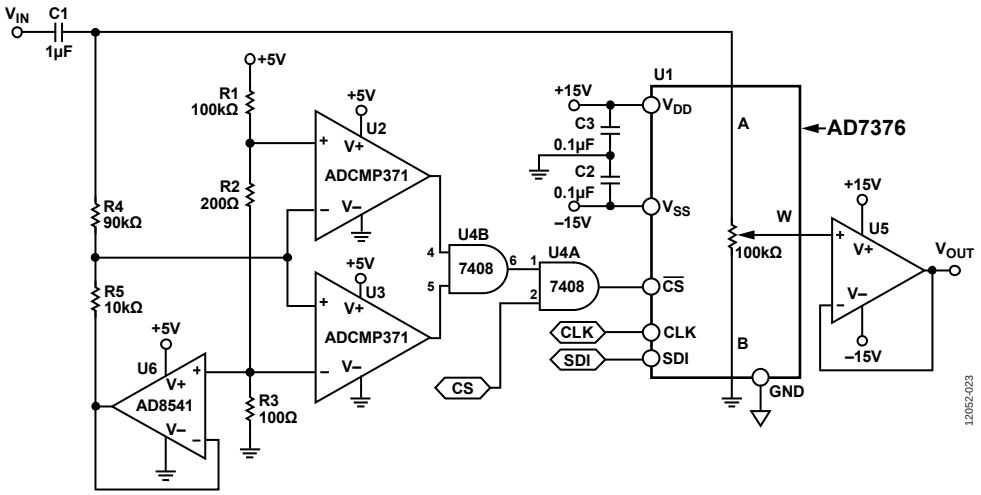


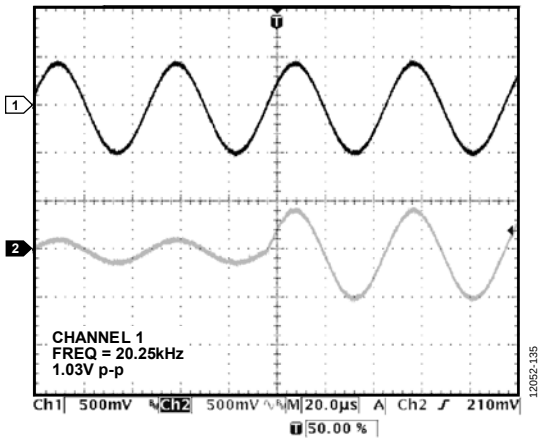
Figure 9. Audio Volume Control

Audio Volume Control

Because of its good THD performance and high voltage capability, the AD7376 can be used for digital volume control. If the AD7376 is used directly as an audio attenuator or gain amplifier, a large step change in the volume level at any arbitrary time can lead to an abrupt discontinuity of the audio signal, causing an audible zipper noise. To prevent this, a zero-crossing window detector is inserted into the $\overline{CS}$ line to delay the device update until the audio signal crosses the window. Because the input signal can operate on top of any dc levels rather than absolute zero volt level, zero crossing, in this case, means the signal is ac-coupled and the dc offset level is the signal zero reference point.

The configuration to reduce zipper noise and the result of using this configuration are shown in Figure 9 and Figure 10, respectively. The input is ac-coupled by C1 and attenuated down before feeding into the window comparator formed by the two ADCMP371 devices (U2 and U3) and two 7408 AND logic gates (U4A and U4B). The AD8541 (U6) is used to establish the signal zero reference. The upper limit of the comparator is set above its offset and, therefore, the output pulses high whenever the input falls between 2.502 V and 2.497 V (or 0.005 V window) in this example. This output is AND'ed with the chip select signal such that the AD7376 updates whenever the signal crosses the window. To avoid constant update of the device, the chip select signal is programmed as two pulses rather than the one shown in the AD7376 data sheet.

In Figure 10, the lower trace shows that the volume level changes from a quarter scale to full scale when a signal change occurs near the zero-crossing window. The AD7376 shutdown sleep mode programming feature is used to mute the device at power-up by holding the $\overline{SHDN}$ pin low and programming zero scale.



NOTES
1. THE LOWER TRACE SHOWS THAT THE VOLUME LEVEL CHANGES FROM QUARTER SCALE TO FULL SCALE, WITH THE CHANGE OCCURRING NEAR THE ZERO-CROSSING WINDOW.

Figure 10. Input (Trace 1) and Output (Trace 2) of the Circuit in Figure 9

Audio Amplifier with Volume Control

The AD5228 and the SSM2211 can form a 1.5 W audio amplifier with volume control that has adequate power and quality for portable devices, such as PDAs and cell phones. The SSM2211 can drive a single speaker differentially between Pin 5 and Pin 8 without any output capacitor. The high-pass cutoff frequency is as follows:

$$f_{H1} = 1/(2\pi \times R1 \times C1)$$

The SSM2211 can drive two speakers, as shown in Figure 11. However, the speakers must be configured in single-ended mode and output coupling capacitors are needed to block the dc current. The output capacitor and the speaker load form an additional high-pass cutoff frequency as follows:

$$f_{H2} = 1/(2\pi \times R5 \times C3)$$

As a result, C3 and C4 must be large to make the frequency as low as f_{H1}.

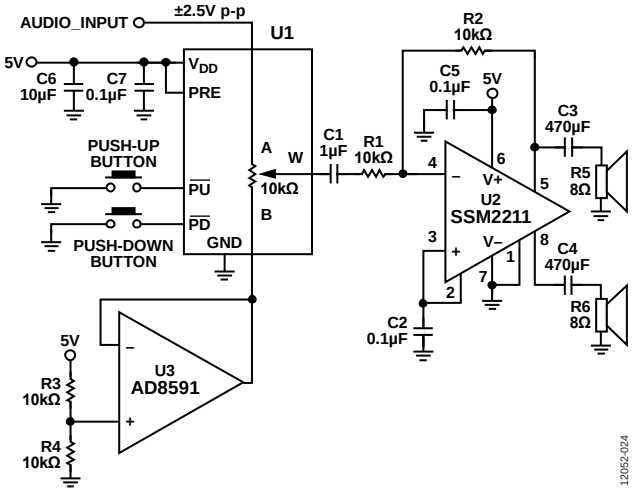


Figure 11. Audio Amplifier with Volume Control

INTERFACING

Q: Can I adjust the digital potentiometer for frequencies around 1 MHz to 10 MHz for adjusting the gain of a video signal?

A: Bandwidth is a function of the code and R_{AB}. Lower R_{AB} and lower codes yield higher bandwidth. Note that 10 MHz bandwidth or above is possible on some digital potentiometers. Refer to the relevant product data sheet for the Bode plots.

Q: What is the maximum frequency applicable to the digital potentiometer clock (CLK) input?

A: For SPI and up/down ($U/\overline{D}$) digital interfaced digital potentiometers, the maximum clock frequency is 10 MHz to 50 MHz. For I²C-compatible digital potentiometers, the maximum CLK frequency is guaranteed for 400 kHz.

LCD Panel V_{COM} Adjustment

A special feature of the AD5259 is its separation of the V_{LOGIC} supply pin and the V_{DD} supply pin. The separation provides greater flexibility in applications that do not always provide the needed supply voltages. In particular, LCD panels require a V_{COM} voltage in the range of 3 V to 5 V to provide a reference voltage to the back plane of the LCD panel.

Figure 12 shows a rare exception in which a 5 V supply is available to power the digital potentiometer.

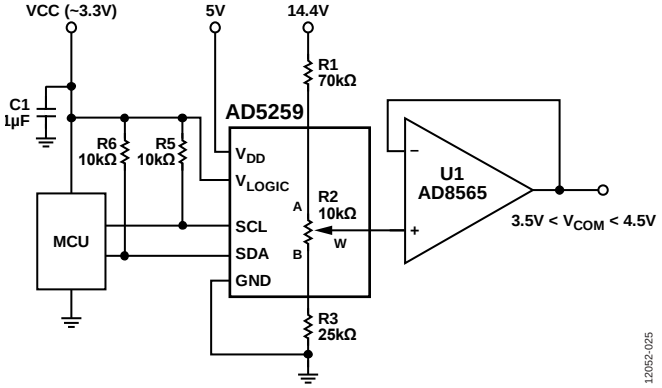


Figure 12. V_{COM} Adjustment Application

In the more common case shown in Figure 13, only analog voltage 14.4 V and digital logic 3.3 V supplies are available. By placing discrete resistors above and below the digital potentiometer, the V_{DD} pin is tapped off the resistor string itself. Based on the chosen resistor values, the voltage at the V_{DD} pin in this case equals 4.8 V, allowing the wiper to be safely operated up to 4.8 V. The current draw of the V_{DD} pin does not affect the bias of the node because it is only on the order of microamperes. The V_{LOGIC} pin is tied to the 3.3 V digital supply of the microcontroller because the V_{LOGIC} pin draws the 35 mA needed when writing to the EEPROM. It is impractical to source 35 mA through the 70 kΩ resistor; therefore, the V_{LOGIC} pin is not connected to the same node as the V_{DD} pin.

The V_{LOGIC} pin and the V_{DD} pin are two separate supply pins that can be either tied together or treated independently. The V_{LOGIC} pin can supply the logic/EEPROM with power while the V_{DD} pin biases Terminal A, Terminal B, and Terminal W for added flexibility.

For a detailed look at this application, see the "Simple VCOM Adjustment uses any Logic Supply Voltage" EDN magazine article in the September 30, 2004 issue.

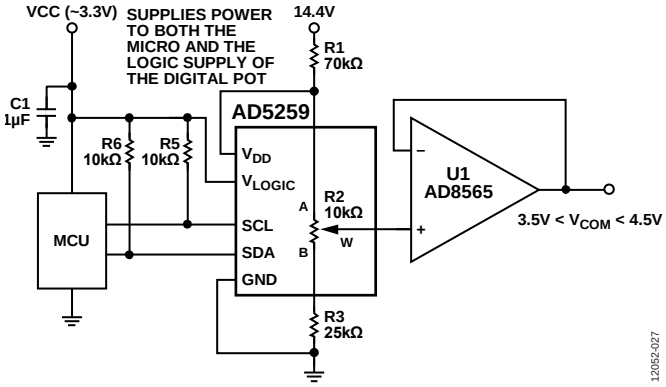


Figure 13. Circuitry When a Separate Supply Is Not Available for the V_{DD} Pin

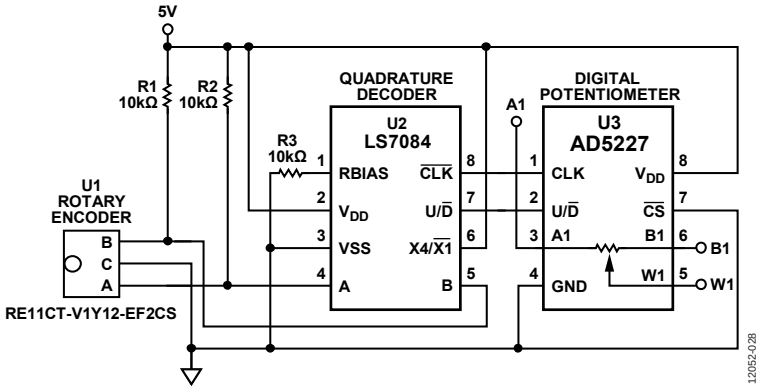


Figure 14. Manual Rotary Control

Manual Control with Rotary Encoder

Figure 14 shows a way of using the AD5227 (U3) to emulate a mechanical potentiometer in a rotary knob operation. The rotary encoder, U1, has a ground terminal, C, and out of phase signals, Signal A and Signal B.

When U1 is turned clockwise, a pulse generated from Terminal B leads a pulse generated from Terminal A and vice versa. Signal A and Signal B of U1 pass through a quadrature decoder, the LS7084 (U2), which translates the phase difference between Signal A and Signal B of U1 into compatible inputs for U3. Therefore, when Signal B leads Signal A (clockwise), U2 provides U3 with a logic high U/$\overline{D}$ signal, and vice versa. U2 also filters noise, jitter, and other transients and debounces the contact bounces generated by U1.

See the AN-1150 Application Note for information on how to control the AD5111, AD5113, and AD5115 with a traditional dial interface.

6-Bit Controller

The AD5227 can form a simple, 6-bit controller with a clock generator, a comparator, and output components. Figure 15 shows a generic 6-bit controller with a comparator that compares the sampling output with the reference level and then outputs either a high level or low level through the U/$\overline{D}$ pin of the AD5227. The AD5227 then changes step at every clock cycle in the direction indicated by the state of the U/$\overline{D}$ pin. This circuit is self contained, easy to design, and can adapt to various applications.

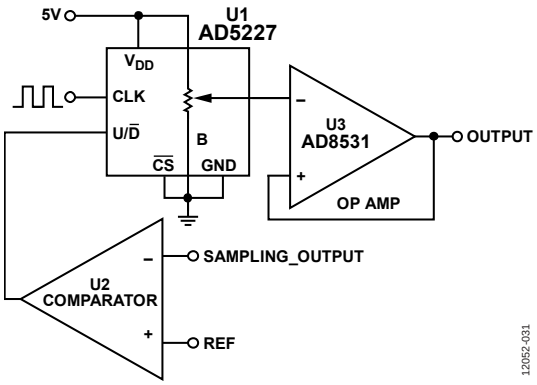


Figure 15. 6-Bit Controller

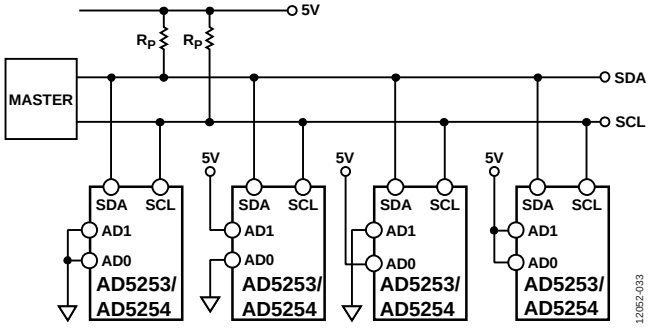


Figure 16. Multiple AD5253/AD5254 Devices on a Single Bus

Multiple Devices on One I²C Bus

The AD5253/AD5254 are equipped with two addressing pins, the AD1 pin and the AD0 pin, which allow up to four AD5253/AD5254 devices to be operated on one I²C bus. To operate both devices on one I²C bus, the states of the AD1 pin and the AD0 pin on each device must first be defined.

An example of addressing the AD1 pin and the AD0 pin is shown in both Table 2 and Figure 16. In I²C programming, each device is issued a different slave address—01011(AD1)(AD0)—to complete the addressing.

Table 2. Multiple Device Addressing

AD1	AD0	Device Addressed
0	0	U1
0	1	U2
1	0	U3
1	1	U4

In wireless base station smart antenna systems that require arrays of digital potentiometers to bias the power amplifiers, large numbers of AD5253/AD5254 devices can be addressed by using extra decoders, switches, and input/output buses, as shown in Figure 16. For example, to communicate to 16 devices, the user needs 4 decoders and 16 sets of combinational switches (four sets are shown in Figure 16). Two input/output buses serve as the common inputs of the four 2 × 4 decoders and select four sets of outputs at each combination. Because the four sets of combination switch outputs are unique, as shown in Figure 16, a specific device is addressed by properly programming the I²C with the slave address defined as 01011(AD1)(AD0).

This operation allows one of 16 devices to be addressed, provided that the inputs of the two decoders do not change states. The inputs of the decoders can change after the operation of the specified device is complete.

Level Shifting for Bidirectional Interface

While most legacy systems can be operated at one voltage, a new component can be optimized at another voltage. When two systems operate the same signal at two different voltages, proper level shifting is needed. For instance, users can employ a 3.3 V EEPROM to interface with a 5 V digital potentiometer. A level shifting scheme enables a bidirectional communication so the setting of the digital potentiometer can be stored in, and retrieved from, the EEPROM. Figure 17 shows one of the level shifting implementations. M1 and M2 can be any N-channel signal field effect transistors (FET), or if either V_{DD1} or V_{DD2} falls below 2.5 V, M1 and M2 can be low threshold FETs, such as the FDV301N. This circuit is not suitable for 1.8 V logic levels.

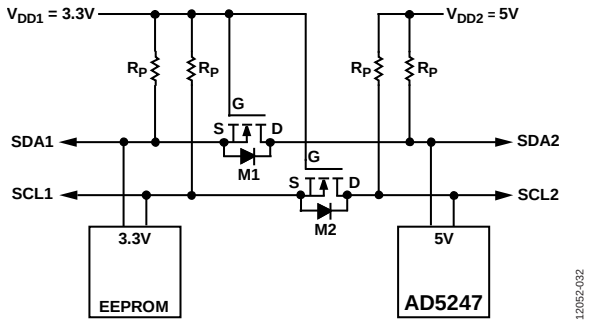


Figure 17. Level Shifting for Operation at Different Potentials

GAIN

The following circuits are designed for dc operation. If the circuits are used with an ac signal excitation, it can result in stability issues. To guarantee that the circuit does not oscillate, placing a 10 pF capacitor in the feedback loop is recommended.

Additionally, if the recommended op amps are substituted, take note of the following restrictions. The gain bandwidth product (GBP) is less than the bandwidth of V_{OUT} (BW(V_{OUT})), and

$$BW(V_{OUT}) = \frac{1}{2\pi \times R_{OUT} \times C}$$

where:
C is the pin capacitance of the V_{OUT} pin.
R_{OUT} is the amplifier output impedance.

R_{OUT} is generally specified in the data sheet specifications or in the typical performance characteristic plots. See the *Practical Techniques to Avoid Instability Due to Capacitive Loading* Analog Dialogue article, Volume 38, Number 2, 2004 for more information.

Linear Gain Setting Mode

Digital potentiometers are ideal for controlling the gain in an amplifier or setting the output voltage of a power supply regulator. However, using the digital potentiometer in potentiometer mode results in a logarithmic transfer function.

Logarithmic transfer functions are desirable in applications such as light or audio control because human senses respond better to these stimuli. For applications where a linear transfer function is preferred, there are some techniques that can be employed, such as the Analog Devices patented architecture, linear gain setting mode, implemented in the AD5144, AD5142, AD5144A, and AD5141.

For more information on linear gain setting mode and other linearizing techniques, see the AN-1169 Application Note, *Linear Setting Mode: A Detailed Description*.

Gain Control Compensation

A digital potentiometer is commonly used in gain control, such as the noninverting gain amplifier shown in Figure 18.

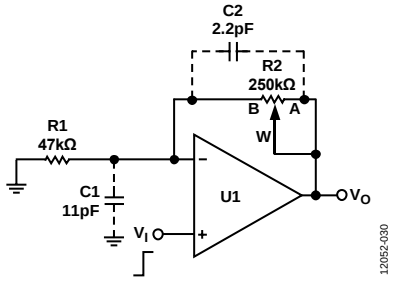


Figure 18. Gain Control Compensation

When the parasitic capacitance of Terminal B is connected to the op amp noninverting node, it introduces a zero for the $1/\beta_O$ term with 20 dB/dec, whereas a typical op amp gain bandwidth product (GBP) has −20 dB/dec characteristics. A large R2 and finite C1 can cause the frequency of this zero to fall well below the crossover frequency. The rate of closure, therefore, becomes 40 dB/dec, and the system has a 0° phase margin at the crossover frequency. If an input is a rectangular pulse or step function, the output can ring or oscillate. Similarly, it is also likely to ring when switching between two gain values, which is equivalent to a stop change at the input.

Depending on the op amp GBP, reducing the feedback resistor extends the frequency of the zero far enough to overcome the problem. A better approach is to include a compensation capacitor, C2, to cancel the effect caused by C1.

Optimum compensation occurs when R1 × C1 = R2 × C2. Optimum compensation is not an option because of the variation of R2. As a result, the user can use the previous relationship and scale C2 as if R2 were at its maximum value. Scaling C2 overcompensates and compromises the performance when R2 is set at low values. Alternatively, this scaling avoids the ringing or oscillation at the worst case. For critical applications, find C2 empirically to suit the oscillation. In general, setting C2 in the range of a few picofarads to no more than a few tenths of picofarads is adequate for the compensation.

Similarly, the capacitances of Terminal W and Terminal A are connected to the output (see Figure 18); their effect at this node is less significant and the compensation can be avoided in most cases.

LED DRIVER

Manual Adjustable LED Driver

The AD5228 can be used in many electronics level adjustments, such as LED drivers for LCD panel backlight controls. Figure 19 shows a manually adjustable LED driver. The AD5228 (U1) sets the voltage across the white LED D1 for brightness control. Because the AD8591 (U2) handles up to 250 mA of output current, a typical white LED with a forward voltage (VF) of 3.5 V requires a resistor, R1, to limit U2 current. This circuit is simple, but not power efficient. The shutdown pin of U2 can be toggled with a pulse-width modulation (PWM) signal to conserve power.

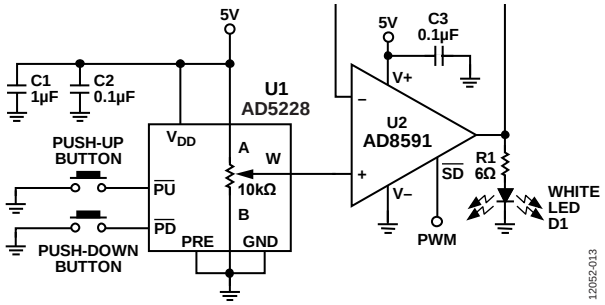


Figure 19. Low Cost Adjustable LED Driver

Adjustable Current Source for LED Driver

Because LED brightness is a function of current rather than of VF, an adjustable current source is preferred over a voltage source, as shown in Figure 20.

The load current is represented as the voltage between the wiper and Terminal B (V_{WB}) of the AD5227 divided by R_{SET}.

$$I_D = \frac{V_{WB}}{R_{SET}}$$

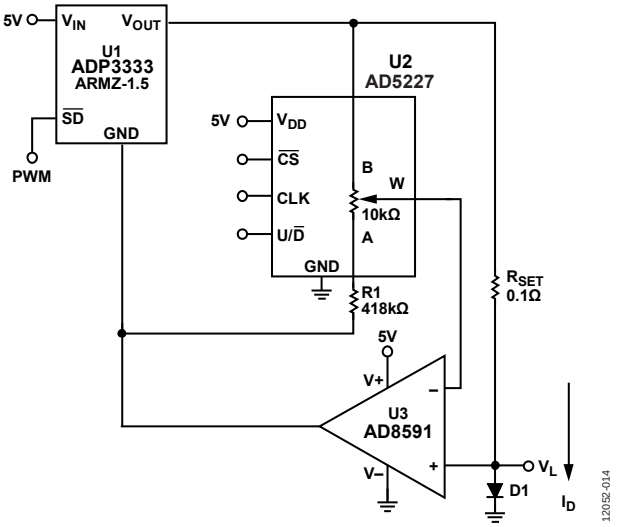


Figure 20. Adjustable Current Source for LED Driver

The ADP3333ARMZ-1.5 (U1) is a 1.5 V low dropout (LDO) regulator that is lifted above or lowered below 0 V. When the V_{WB} of the AD5227 is at a minimum, there is no current through the diode (D1), and thus the GND pin of the ADP3333 (U1) is at −1.5 V if the AD8591 (U3) is biased with dual supplies. As a result, some of the AD5227 (U2) low resistance steps have no effect on the output until the GND pin of U1 is lifted above 0 V.

When the V_{WB} of the AD5227 is at its maximum, V_{OUT} becomes the load voltage (V_L) plus the voltage across U2 (V_{AB}); thus, the U1 supply voltage must be biased with adequate headroom. Similarly, a PWM signal can be applied at the shutdown pin of U1 for power efficiency. This circuit works well for a single LED.

VOLTAGE TO CURRENT CONVERSION

Programmable Current Source

A programmable current source can be implemented with the circuit shown in Figure 21.

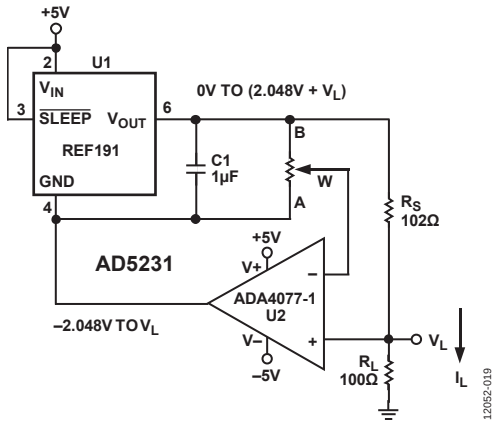


Figure 21. Programmable Current Source

The REF191 (U1) is a unique, low supply, headroom precision reference that can deliver the up to 20 mA at 2.048 V. The load current (I_L) is the voltage across Terminal B and Terminal W of the digital potentiometer divided by R_S.

$$I_L = \frac{V_{REF} \times D}{R_S \times 1024}$$

where:
D is the code of the digital potentiometer wiper (U3 in Figure 21).
V_{REF} is the voltage of the chosen reference (2.048 V in Figure 21).

The circuit in Figure 21 is simple, but be aware that there are two issues. First, dual-supply op amps are ideal because the ground potential of the REF191 can swing from −2.048 V, at zero scale, to the voltage of the load (V_L), at full scale, of the potentiometer mode setting. Although the circuit works under single supply, the programmable resolution of the system is reduced. Second, the voltage compliance at V_L is limited to 2.5 V or equivalent to a 125 Ω load. If higher voltage compliance is needed, users can consider digital potentiometers such as the AD5260, the AD5280, and the AD7376.

To achieve higher current, such as when driving a high power LED, the user can replace U1 in Figure 21 with an LDO, reduce R_S, and add a resistor in series with Terminal A of the digital potentiometer. This procedure limits the current of the potentiometer and increases the current adjustment resolution.

Programmable Bidirectional Current Source

For applications that require bidirectional current control or higher voltage compliance, a Howland current pump is one solution (see Figure 22).

If the resistors are matched, the load current is

$$I_L = \frac{(R2A + R2B)}{R1/R2B} \times V_W$$

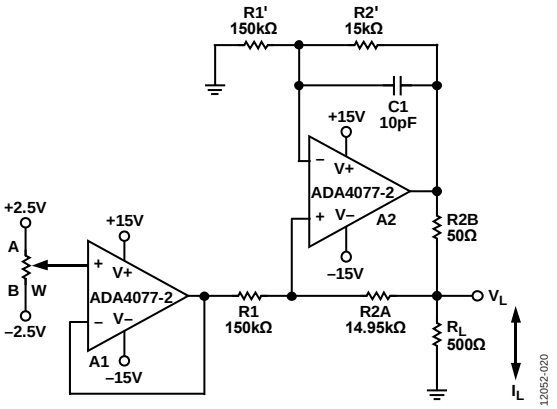


Figure 22. Programmable Bidirectional Current Source

R2B, in theory, can be made as small as necessary to achieve the current needed within the ADA4077-2 (A2) output current driving capability. In the circuit shown in Figure 22, A2 delivers ±5 mA in both directions and the voltage compliance approaches 15 V. It can be shown that the output impedance (Z_O) is

$$Z_O = \frac{R1'R2B(R1 + R2A)}{R1R2' - R1'(R2A + R2B)}$$

Z_O can be infinite if the R1' and R2' resistors match precisely with R1 and R2A + R2B, respectively. On the other hand, Z_O can be negative if the resistors are not matched.

As a result, C1, in the range of 1 pF to 10 pF, is needed to prevent oscillation from the negative impedance.

FILTERING

Programmable Low-Pass Filter

In analog-to-digital conversions, it is common to include an antialiasing filter to band limit the sampling signal. Therefore, the dual channel AD5235 (denoted by R1 and R2) can be used to construct a second order, Sallen-Key low-pass filter, as shown in Figure 23.

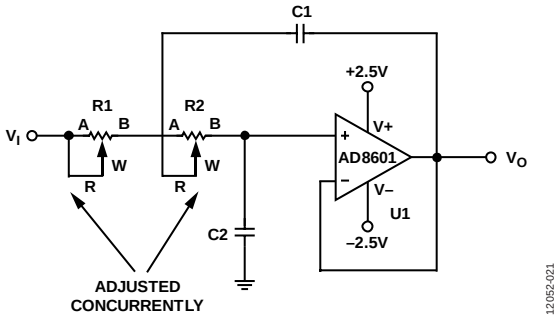


Figure 23. Sallen-Key Low-Pass Filter

The design equations for the Sallen-Key low-pass filter are

$$\frac{V_O}{V_I} = \frac{\omega f^2}{S^2 + \frac{\omega f}{Q}S + \omega f^2}$$

$$\omega_O = \sqrt{\frac{1}{R1R2C1C2}}$$

$$Q = \frac{1}{R1C1} + \frac{1}{R2C2}$$

First, users select convenient values for the capacitors. To achieve maximally flat bandwidth, where Q = 0.707, let C1 be twice the size of C2 and let R1 equal R2. As a result, the user can adjust R1 and R2 concurrently to the same setting to achieve the desirable bandwidth.

Programmable State Variable Filter

One of the standard circuits used to generate a low-pass filter or a band-pass filter is the state variable active filter. The AD5233 can be used in this application to provide full programmability of the frequency, gain, and Q of the filter outputs.

Figure 24 shows a filter circuit using a 2.5 V virtual ground, which allows a ±2.5 V peak input and output swing; the RDAC2 register and the RDAC3 register set the low-pass, high-pass, and band-pass cut off and center frequencies, respectively. To maintain the best Q of the circuit, the RDAC2 register and the RDAC3 register are programmed with the same data (as with ganged potentiometers).

The transfer function for the band-pass filter is

$$\frac{V_{BP}}{V_i} = \frac{A_O \times \frac{\omega_O}{Q} S}{S^2 + \frac{\omega_O}{Q} S + {\omega_O}^2}$$

where:
A_O is the gain.
V_i is the voltage input.
V_{BP} is the voltage at the band-pass filter.

For $R_{WB2} = R_{WB3}$, R1 = R2, and C1 = C2,

$$\omega_O = \frac{1}{R_{WB2} \times C1}$$

where R_{WBx} is the resistance between Terminal W and Terminal B corresponding to the RDACx register (where x is 1 to 4).

$$A_O = \frac{R_{WB1}}{R_{WA1}}$$

where R_{WAx} is the resistance between Terminal W and Terminal A corresponding to the RDACx register (where x is 1 to 4).

$$Q = \frac{R_{WA4}}{R_{WB4}} \times \frac{R_{WB1}}{R1}$$

Figure 24 shows the measured filter response at the band-pass output as a function of the RDAC2 register and the RDAC3 register settings. The settings produce a range of center frequencies from 2 kHz to 20 kHz.

The filter gain response at the band-pass output is shown in Figure 24. At a center frequency of 2 kHz, the gain is adjusted over the −20 dB to +20 dB range, determined by the RDAC1 register. The Q of the circuit is adjusted by the RDAC4 register and the RDAC1 register. Suitable op amps for this application are the ADA4077-2, the AD8604, the OP279, and the AD824.

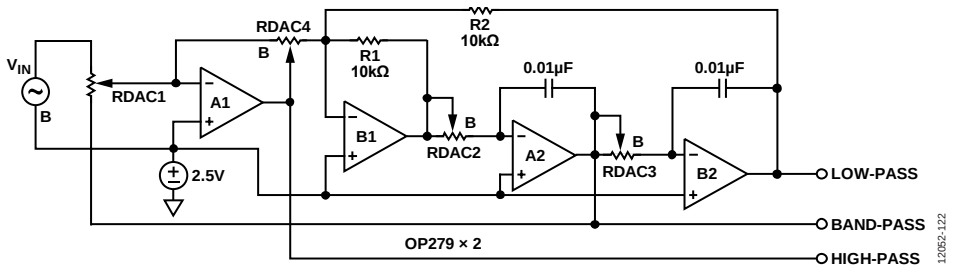


Figure 24. Programmable State Variable Filter

OTHER USAGE EXAMPLES

Programmable Voltage Source with Boosted Output

For applications that require high current adjustment, such as a laser diode driver or tunable laser, a boosted voltage source can be considered (see Figure 25).

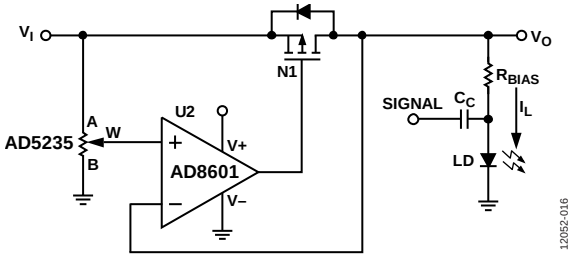


Figure 25. Programmable Booster Voltage Source

In this circuit, the inverting input of the op amp forces V_O to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the N-channel FET, N1 (see Figure 25). N1 power handling must be adequate to dissipate $(V_I - V_O) \times I_L$ power.

This circuit can source a 100 mA maximum with a 5 V supply. For precision applications, a voltage reference, such as the ADR421or the ADR03, can be applied at Terminal A of the digital potentiometer.

High Voltage DAC

The AD7376 can be configured as a high voltage DAC as high as 30 V. The circuit is shown in Figure 26. The output is

$$V_O(D) = \frac{D}{128}\left[1.2\text{ V} \times \left(1 + \frac{R2}{R1}\right)\right]$$

where D is the decimal code from 0 to 127.

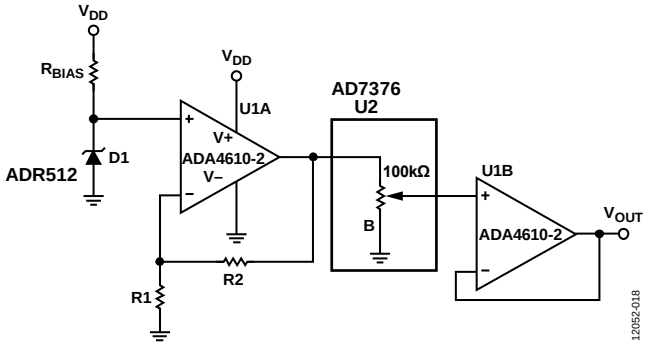


Figure 26. High Voltage DAC

Programmable Oscillator

In a classic Wien bridge oscillator, the Wien network (R||C, R'C') provides positive feedback, whereas R1 and R2 (split into R2A and R2B) provide negative feedback (see Figure 27).

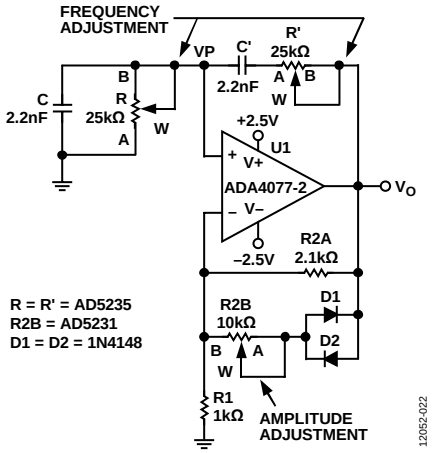


Figure 27. Programmable Oscillator with Amplitude Control

At the resonant frequency, f_O, the overall phase shift is zero, and the positive feedback causes the circuit to oscillate. With R = R', C = C', and R2 = R2A/(R2B + R_{DIODE}), where R_{DIODE} is the resistance of the two diodes (D1 and D2), the oscillation frequency is

$$\omega_O = \frac{1}{R \times C}$$

Or

$$f_O = \frac{1}{2\pi \times R \times C}$$

where R is equal to R_{WA} such that

$$R_{WA}(D) = \frac{1024 - D}{1024} \times R_{AB} + R_W$$

At resonance, setting R2/R1 = 2 balances the bridge. In practice, set R2/R1 slightly larger than 2 to ensure that oscillation can start. On the other hand, the alternate turn on of the diodes, D1 and D2, ensures that R2/R1 is smaller than 2, momentarily stabilizing the oscillation. When the frequency is set, the oscillation amplitude can be turned by R2B because

$$\frac{2}{3}V_O = I_D R2B + V_D$$

where:
I_D is the current through the diode.
V_D is the voltage drop across the diode.

V_O, I_D, and V_D are interdependent variables. With proper selection of R2B, an equilibrium is reached such that V_O converges. R2B can be in series with a discrete resistor to increase the amplitude, but the total resistance must not be too large to saturate the output.

Constant Bias with Supply to Retain Resistance Setting

Users who consider EEMEM potentiometers, but cannot justify the additional cost and programming for their designs, can consider constantly biasing the AD5227 with the supply to retain the resistance setting, as shown in Figure 28.

The AD5227 is designed specifically with low power to allow power conservation even in battery operated systems. As shown in Figure 29, a similar low power digital potentiometer is biased with a 3.4 V, 450 mA/hour, Li-Ion cell phone battery. The measurement shows that the device drains negligible power. Constantly biasing the potentiometer is a practical approach because most portable devices do not require detachable batteries for charging. Although the resistance setting of the AD5227 is lost when the battery must be replaced, this event occurs so infrequently that the inconvenience is minimal for most applications.

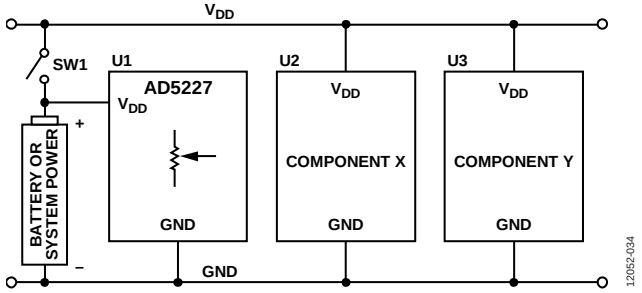


Figure 28. Constant Bias of the AD5227 for Resistance Retention

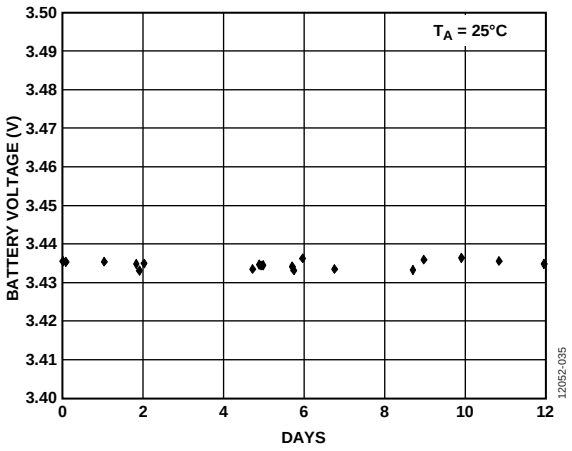


Figure 29. Battery Consumption Measurement

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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