ANALOG DEVICES

AN-1283
APPLICATION NOTE

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Receiving the 4:2:0 Stream with the ADV7619

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INTRODUCTION

This application note outlines the usage of the ADV7619 HDMI® video receiver for the 4:2:0 HDMI stream 4k × 2k at 60 Hz.

The ADV7619 can receive 4:2:0 video streams in a way similar to how t it receives 4:4:4 data in 4k × 2k modes. To enable this, set OP_FORMAT_SEL to the value of 0x54 and set all other I^2C writes in the same way as for 4k × 2k 4:4:4 video mode. Because the ADV7619 works only as a bypass for 4k × 2k modes, it outputs samples as they are received without providing color space conversion (CSC). The receiver bypasses CP core and thus neither CSC nor upconversion/down-conversion of video standard is available.

4:2:0 Transmission

The 4k × 2k at 60 Hz HDMI 4:2:0 8-bit data stream has a TMDS clock frequency of 297 MHz. It is the same as 4k × 2k at 30 Hz HDMI 4:4:4 8-bit data stream. The main difference between the 4:2:0 and 4:4:4 enabling 60 Hz refresh rate is the content of the stream.

The 4:2:0 stream sends two luma (Y) samples in the same period of time as the 4:4:4 stream sends one luma sample. This allows for a shortening period of line length, thus shortening the period of frame by half allowing for 60 Hz transmission. This increase of luma bandwidth in 4:2:0 is done at the cost of bandwidth reduction of chroma (Cb and Cr) samples.

Pixel Bus Output for 4:2:0 Transmission

The 4:2:0 4k × 2k at 60 Hz stream consists of two luma samples per dot clock and one chroma sample. The chroma sample contains blue (Cb) or red (Cr) components depending on the line being transmitted. Even lines (0, 2, 4, and so on) contain Cb samples whereas odd lines (1, 3, 5, and so on) contain Cr samples as shown in Figure 1 and Figure 2, respectively.

In 2 × SDR 4:4:4 interleaved mode, the pixel bus outputs two 2 × 24 bit data onto two 24-bit wide sub-buses (upper pixel output 47 to 24) and lower pixel output 23 to 0). Note that this mode is detailed in the Special SDR 4:2:2 and 4:4:4 Output Modes for Video with Pixel Clock Frequencies Above 170 MHz table in the ADV7619 data sheet.

This parallel output allows for dividing the clock frequency by half to 148.5 MHz from the original 297 MHz for 4k × 2k at 60 Hz 4:2:0.

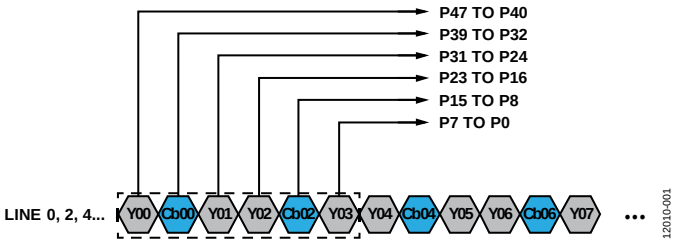

Figure 1. Pixel Lines Assignment of the 4:2:0 Stream (Even Line) in ADV7619

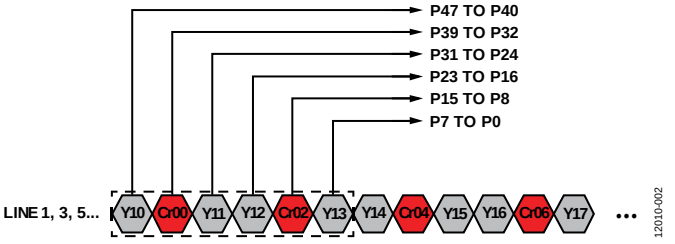

Figure 2. Pixel Lines Assignment of the 4:2:0 Stream (Odd Line) in ADV7619

The detailed pixel bus assignment is shown in Table 1.

CONVERSION 4:2:0 TO 4:4:4

The ADV7619 does not provide a color space converter that could handle a conversion between 4:2:0 and 4:4:4. The conversion can be performed in an external FPGA. The upscaling of 4:2:0 to 4:4:4 increases bandwidth by 2.

To convert 4:4:4 to 4:2:0, it is necessary to use line buffers that allow for collection of Cb and Cr data from consecutive video lines. Figure 3 shows the concept of upscaling 4:2:0 to 4:4:4 stream.

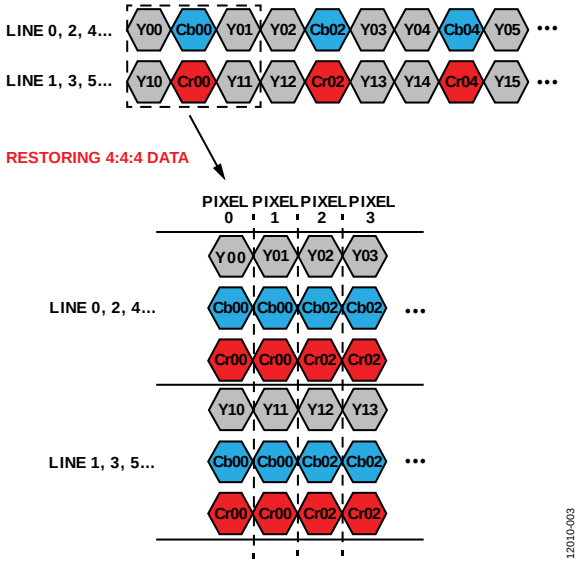

Figure 3. Concept of 4:2:0 to 4:4:4 Conversion

Table 1. Pixel Bus Output for 4:2:0 Mode with OP_FORMAT_SEL = 0x54

	Even Lines = 0, 2, 4, 6, …	Odd Lines = 1, 3, 5, 7, …
Pin	**2 × 24-Bit Mode 0**	**2 × 24-Bit Mode 0**
P47	Y7-0	Y7-0
P46	Y6-0	Y6-0
P45	Y5-0	Y5-0
P44	Y4-0	Y4-0
P43	Y3-0	Y3-0
P42	Y2-0	Y2-0
P41	Y1-0	Y1-0
P40	Y0-0	Y0-0
P39	Cb7-0	Cr7-0
P38	Cb6-0	Cr6-0
P37	Cb5-0	Cr5-0
P36	Cb4-0	Cr4-0
P35	Cb3-0	Cr3-0
P34	Cb2-0	Cr2-0
P33	Cb1-0	Cr1-0
P32	Cb0-0	Cr0-0
P31	Y7-1	Y7-1
P30	Y6-1	Y6-1
P29	Y5-1	Y5-1
P28	Y4-1	Y4-1
P27	Y3-1	Y3-1
P26	Y2-1	Y2-1
P25	Y1-1	Y1-1
P24	Y0-1	Y0-1
P23	Y7-2	Y7-2
P22	Y6-2	Y6-2
P21	Y5-2	Y5-2
P20	Y4-2	Y4-2
P19	Y3-2	Y3-2
P18	Y2-2	Y2-2
P17	Y1-2	Y1-2
P16	Y0-2	Y0-2
P15	Cb7-2	Cr7-2
P14	Cb6-2	Cr6-2
P13	Cb5-2	Cr5-2
P12	Cb4-2	Cr4-2
P11	Cb3-2	Cr3-2
P10	Cb2-2	Cr2-2
P9	Cb1-2	Cr1-2
P8	Cb0-2	Cr0-2
P7	Y7-3	Y7-3
P6	Y6-3	Y6-3
P5	Y5-3	Y5-3
P4	Y4-3	Y4-3
P3	Y3-3	Y3-3
P2	Y2-3	Y2-3
P1	Y1-3	Y1-3
P0	Y0-3	Y0-3

REFERENCES

ADV7619 Data Sheet. 2012. Analog Devices, Inc.

UG-237 Hardware User Guide. 2012. Analog Devices, Inc.

REVISION HISTORY

1/14—Revision 0: Initial Version

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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