Embedded Packet Error Rate Testing on the ADF7023 and ADF7023-J
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INTRODUCTION

This application note provides information on the built-in packet error rate (PER) test mode on the ADF7023 and ADF7023-J. This mode helps the user to set up a communication link and test its quality.

Up to 65,535 packets can be transmitted with a programmable delay between packets. The packet stored in packet RAM is transmitted each time. If the cyclic redundancy check (CRC) is correct, the receiver determines it has correctly received a packet.

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REVISION HISTORY

12/13—Revision 0: Initial Version

REGISTERS USED WITH EMBEDDED PER TEST

Table 1. 0x139: TESTMODES Register Used with Embedded PER Tests

Bit	Name	R/W	Description
3	PER_IRQ_SELF_CLEAR	R/W	1: Automatic clear of TX_EOF interrupt in transmit, CRC interrupt in receive. 0: Normal operation.
2	PER_ENABLE	R/W	1: Packet error rate enabled. 0: Packet error rate disabled.
1	CONTINUOUS_TX	R/W	1: Restart Tx after transmitting a packet. 0: Normal end of Tx.
0	CONTINUOUS_RX	R/W	1: Restart Rx after receiving a packet. 0: Normal end of Rx.

Table 2. PER Test Control Registers

Address (Hex)	Normal Operation	PER Mode Operation	Description
0x011	Available for packet data	PER_COUNT_LOW	Bits[7:0] of PER_COUNT[15:0] (PER_COUNT increments in Rx and decrements in Tx).
0x012	Available for packet data	PER_COUNT_HIGH	Bits[15:8] of PER_COUNT[15:0] (PER_COUNT increments in Rx and decrements in Tx).
0x013	Available for packet data	PER_TX_WAIT_TIME	In Tx, delay between packets transmitted.

The PER test is controlled from the TESTMODES register (0x139) as defined in Table 1.

When PER test mode is enabled, the packet RAM locations take on a new function as shown in Table 2; these locations are therefore no longer available for packet data. When PER test mode is disabled, these locations are once again available for packet data.

Packet RAM locations 0x20 to 0xFF are available for packet data in the PER test. Bytes 0x00 to 0x1F are allocated for use by the on-chip processor and must not be used for packet data.

Some packet RAM locations are given up for use with the embedded PER test as outlined in Table 2. The receive and transmit packet counters are stored in packet RAM locations 0x011 and 0x012, and the delay between packets in transmit mode is programmed in Address 0x013.

RECEIVER PER SETUP

In receive mode (Rx), the user enables Bit 3, Bit 2, and Bit 0 of the TESTMODES register (Address 0x139). Bit 3 (PER_IRQ_SELF_CLEAR) automatically clears the CRC interrupt, preparing the receiver for the next packet. Bit 2

(PER_ENABLE) enables the PER test, and Bit[0] (CONTINUOUS_RX) restarts the Rx after receiving a packet.

Then, each time a valid packet (CRC correct) is received, the PER_COUNT registers get incremented, the CRC interrupt is cleared, and Rx is restarted.

Note that it is up to the user to initialize this counter when needed. Therefore, at the start of a PER test, PER_COUNT should be set to 0x0000. The sample Rx PER script provided here does this. This may be appended to the normal Rx script to enable Rx PER testing.

```
//Zero the packet RAM used for PER counters
181100      //PER_COUNT_LOW
181200      //PER_COUNT_HIGH
            //Initializes PER_COUNT to 0x0000
19390D      //CONTINUOUS_RX, PER_ENABLE
            //PER_IRQ_SELF_CLEAR
B2          //Start PHY_RX
```

Once testing is finished, PER_COUNT[15:0] (Address 0x012 and Address 0x011) holds the number of received packets (CRC corrects).

TRANSMITTER PER SETUP

In transmit mode (Tx), if Bit 3, Bit 2, and Bit 1 of the TESTMODES register (Address 0x139) are set to 1, the [ADF7023](#) transmits the packet in the Tx buffer, PER_COUNT + 1 number of times (+ 1 because it counts down to 0).

Bit 3, PER_IRQ_SELF_CLEAR, automatically clears the TX_EOF interrupt. Bit 2, PER_ENABLE, enables the PER test, and Bit 1 CONTINUOUS_TX, restarts the Tx after transmitting a packet.

The user initializes PER_COUNT for the desired number of packets to Test − 1. After every TX_EOF interrupt, the PER_COUNT is decremented, the TX_EOF interrupt is cleared, and the Tx is restarted after a user-defined wait time. When PER_COUNT reaches zero, CONTINUOUS_TX (Bit 1 of TESTMODES) is cleared, thus terminating packet transmission.

The wait period separating each packet, the interpacket delay, is, at a minimum, the PHY_TX to PHY_TX state transition time, but additional time can be added by programming the value in Register PER_TX_WAIT_TIME (Address 0x013). This value controls the number of additional time steps to add to the interpacket delay.

The value of the time step depends on the value in TRANSITION_CLOCK_DIV (Address 0x13A).

If the fast transition time is enabled (FAST_TRANSITION = 1 in TRANSITION_CLOCK_DIV), the time step has a value of 2.5 μs.

If the fast transition time is not enabled (FAST_TRANSITION = 4 or FAST_TRANSITION = 0 in TRANSITION_CLOCK_DIV), then the time step will have a value of 10 μs.

The wait period between packets for a nonzero value in PER_TX_WAIT_TIME is

$$PHY\_TX\ to\ PHY\_TX\ StateTransitionTime$$
$$+\ PER\_TX\_WAIT\_TIME \times T\_STEP$$

where:
T_STEP = 2.5 μs or 10 μs depending on the value of $FAST\_TRANSITION$ in Address 0x13A.

If a value of 0 is programmed into PER_TX_WAIT_TIME, then the interpacket delay will be approximately 10.4 ms for fast transition time disabled, and approximately 2.8 ms for fast transition time enabled.

The script shown here is a sample Tx PER script.

```
1811E7          // PER_COUNT_LOW
181203          //PER_COUNT_HIGH - 1000 resends
1813FF          //Delay between packets
19390E          //CONTINUOUS_TX, PER_ENABLE
                //PER_IRQ_SELF_CLEAR
B5              //Start PHY_TX
```

TEST OUTCOME

By comparing the number of packets received (PER_COUNT in the receiving device) with the number of packets transmitted (initial PER_COUNT + 1 in the transmitting device), the user can easily deduce the PER and thus the link quality of the channel.

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