ANALOG DEVICES

AN-1275
APPLICATION NOTE

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Rolling Data Buffer on the ADF7023

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INTRODUCTION

When the ADF7023 receives a packet in packet mode, it stores the data in a linear sequence in the packet RAM. Prior to transmission, the data to be transmitted is written to the packet RAM in a linear sequence. This functionality is described in the ADF7023 data sheet. The ADF7023 packet RAM is 240 bytes long. If the packet length is greater than 240 bytes, additional measures are required. This application note describes a method of how to handle longer packet lengths on the ADF7023, up to a maximum length of 65,535 bytes, via a rolling buffer mechanism. This method reuses and renames several registers of the ADF7023.

Tx/Rx ROLLING DATA BUFFER

Use the registers shown in Table 1 for the rolling buffer operation. In rolling buffer mode, packet RAM locations Address 0x020 to Address 0x0FF are available for packet data. Packet RAM memory locations Address 0x000 to Address 0x01F[1] are allocated for use by the on-chip processor and must not be used for packet data.

Use the interrupts defined in Table 2 and Table 3 for rolling buffer operation. Note that these interrupts are reused from their normal operation, and are not available for their normal operation when rolling buffer mode is enabled. When rolling buffer mode is disabled, they revert back to the functions described in the ADF7023 data sheet.

ROLLING BUFFER REGISTERS

When the rolling buffer is enabled via the TESTMODES register (Register 0x139), Register 0x134 to Register 0x137 take on the rolling buffer control mechanism and are not available for address matching or for a static register fix at the same time. The following tables supply the ADF7023 register names and their equivalent rolling buffer register names.

[1] When rolling buffer mode is not enabled, Address 0x000 to Address 0x00F are allocated for use by the on-chip processor, and Address 0x010 to Address 0x0FF are available for packet data (see the ADF7023 data sheet).

Table 1. Tx/Rx Rolling Data Buffer Registers

Address (Hex)	Register	Rolling Buffer Name	Description
0x124	TX_BASE_ADR		Start location in packet RAM of transmit buffer
0x125	RX_BASE_ADR		Start location in packet RAM of receive buffer
0x134	Address Filtering	BB_RX_BUFFER_SIGNAL	Receive buffer nearly full
0x135	Address Filtering	BB_RX_BUFFER_SIZE	Receive buffer full
0x136	Address Filtering	BB_TX_BUFFER_SIGNAL	Transmit buffer nearly full
0x137	Address Filtering	BB_TX_BUFFER_SIZE	Transmit buffer full
0x139	TESTMODES		Enable test modes for use with rolling buffer

Table 2. Address 0x100: INTERRUPT_MASK_0 Interrupts Reused for Rolling Buffer Operation[1]

Bit	Name	Rolling Buffer Name	R/W	Description
[6]	INTERRUPT_SWM_RSSI_DET	INTERRUPT_BUFFER_FULL	R/W	Interrupt when the receive or transmit buffer is full 1 = interrupt enabled; 0 = interrupt disabled
[5]	INTERRUPT_AES_DONE	INTERRUPT_BUFFER_ALMOST_FULL	R/W	Interrupt when the receive or transmit buffer is almost full 1 = interrupt enabled; 0 = interrupt disabled

[1] When rolling buffer is enabled, these bits take on a new function, and when rolling buffer is disabled, they revert back to the ADF7023 data sheet definition.

Table 3. Address 0x336: INTERRUPT_SOURCE_0 Interrupts Reused for Rolling Buffer Operation[1]

Bit	Name	Rolling Buffer Name	R/W	Description
[6]	INTERRUPT_SWM_RSSI_DET	INTERRUPT_BUFFER_FULL	R/W	Asserted when the receive or transmit buffer is full (receive or transmit buffer size is reached)
[5]	INTERRUPT_AES_DONE	INTERRUPT_BUFFER_ALMOST_FULL	R/W	Asserted when the receive or transmit buffer is almost full (receive or transmit buffer signal is reached)

[1] When rolling buffer is enabled, these bits take on a new function, and when rolling buffer is disabled, they revert back to the ADF7023 data sheet definition.

Table 4. Address 0x139: TESTMODES for Use with Rolling Buffer

Bit	Name	Rolling Buffer Name	R/W	Description
[5]	RESERVED	ROLLING_BUFFER_PACKET_RX	R/W	1 = enable receive rolling buffer; 0 = normal operation
[4]	RESERVED	PAYLOAD_ONLY_PACKET_TX	R/W	1 = enable transmit payload only rolling buffer; 0 = normal operation

Table 5. Maximum Packet Length Control[1]

Address (Hex)	Name	Rolling Buffer Name	Description
0x014	Available for packet data	TRX_BYTE_LOW	Bits[7:0] of MAX_ROLLING_BUFFER_LEN[15:0], the lower byte of the packet length control register
0x015	Available for packet data	TRX_BYTE_HIGH	Bits[15:8] of MAX_ROLLING_BUFFER_LEN[15:0], the upper byte of the packet length control register

[1] When rolling buffer is enabled, these packet RAM memory locations take on a new function and are no longer available for packet data. When rolling buffer is disabled, they revert back to the ADF7023 data sheet definition.

ROLLING BUFFER: TRANSMIT MODE

Set Bit[4] of the TESTMODES register (Address 0x139) to 1 to enable the payload only rolling buffer in transmit mode. This mode allows the user to transmit a packet of up to 65,535 bytes long using the custom packet structure. The maximum transmit length is programmable up to 0xFFFF by programming the MAX_ROLLING_BUFFER_LEN[15:0] bits as defined in Table 5, which are defined locally in the packet RAM in the rolling buffer mode.

The number and type of preamble, sync, payload, and cyclic redundancy check (CRC) is no longer bounded by the ADF7023; instead, the device transmits what is placed in the transmit buffer. This mode can be used in all three modulations: frequency shift keying (FSK), Gaussian frequency shift keying (GFSK), and on-off keying (OOK).

The payload only mode is an alternative to sport mode for users who interface with the device via the SPI only. In this mode, the data in the transmit buffer is sent over the air until MAX_ROLLING_BUFFER_LEN[15:0] bytes are sent or a command is issued.

In transmit mode, the start of the rolling buffer in packet RAM is set by TX_BASE_ADR. The size of the buffer is set by the BB_TX_BUFFER_SIZE register. The buffer size must not exceed the available packet RAM. When the value in the BB_TX_BUFFER_SIZE register is added to the address in the TX_BASE_ADR register, do not exceed 0x0FF.

Set the value in the BB_TX_BUFFER_SIGNAL register so that an INTERRUPT_BUFFER_ALMOST_FULL interrupt is generated prior to the transmission of all the data in the buffer. Typically, the BB_TX_BUFFER_SIGNAL register is set so that the interrupt is asserted when half the data in the buffer is transmitted.

When an INTERRUPT_BUFFER_ALMOST_FULL is asserted, the host microprocessor writes new data to the locations from the TX_BASE_ADR register to the TX_BASE_ADR register + the BB_TX_BUFFER_SIGNAL register.

When the data in the last byte of the transmit buffer is transmitted, the ADF7023 continues transmitting, starting with the data at the TX_BASE_ADR register. If enabled, an INTERRUPT_BUFFER_FULL interrupt is asserted when the last byte in the buffer is transmitted.

When an INTERRUPT_BUFFER_FULL is asserted, the host microprocessor writes new data to the locations from TX_BASE_ADR + BB_TX_BUFFER_SIGNAL + 1 to TX_BASE_ADR + BB_TX_BUFFER_SIZE.

Transmission of data continues until the MAX_ROLLING_BUFFER_LEN[15:0] bytes are sent (Tx_EOF) or the user issues the CMD_PHY_ON command.

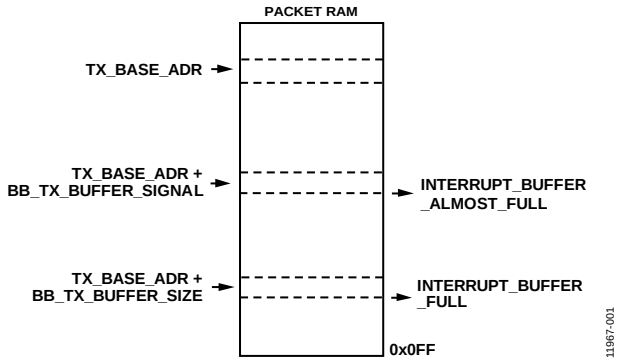

Figure 1. Rolling Buffer in Transmit Mode

ROLLING BUFFER: RECEIVE MODE

Set Bit[5] of the TESTMODES register (Address 0x139) to 1 to enable the rolling buffer in receive mode. The ADF7023 can receive packet length up to $2^{16} - 1$ bytes long (65,535 bytes) via the rolling buffer mechanism. The maximum packet length is programmable up to 0xFFFF by programming the MAX_ROLLING_BUFFER_LEN[15:0] bits, as defined in Table 5.

When Bit[5] of the TESTMODES register (Address 0x139) is set and the sync word is received, the packet handler uses the rolling buffer to capture the remainder of the packet. This mode is available for FSK/GFSK/OOK operation.

In receive mode, the RX_BASE_ADR register sets the start of the rolling buffer in packet RAM. Set the size of the buffer using the BB_RX_BUFFER_SIZE register. The buffer size must not exceed the available packet RAM. When the value in the BB_RX_BUFFER_SIZE register is added to the address in the RX_BASE_ADR register, do not exceed 0x0FF.

Set the value in the BB_RX_BUFFER_ register so that an INTERRUPT_BUFFER_ALMOST_FULL interrupt is asserted prior to the buffer being filled by the received data. Typically, the BB_RX_BUFFER_SIGNAL register is set so the interrupt is asserted when half the buffer is filled with received data.

When an INTERRUPT_BUFFER_ALMOST_FULL is asserted, the host microprocessor reads in the data in the locations from the RX_BASE_ADR register to the RX_BASE_ADR register + the BB_RX_BUFFER_SIGNAL register.

When the last byte of the Rx buffer is filled, the ADF7023 continues to write the received data starting at the RX_BASE_ADR register.

If enabled, an INTERRUPT_BUFFER_FULL interrupt is asserted when the buffer is filled.

When an INTERRUPT_BUFFER_FULL is asserted, the host microprocessor reads in the data in the locations from the RX_BASE_ADR register + the BB_RX_BUFFER_SIGNAL register + 1 to the RX_BASE_ADR register + the BB_RX_BUFFER_SIZE register.

Reception of data continues until the length programmed in the MAX_ROLLING_BUFFER_LEN[15:0] register is achieved (Rx_EOF) or the host micro issues the CMD_PHY_ON command.

Note that it is up to the user to detect the end of the payload and perform some error checking operation on the data, such as CRC.

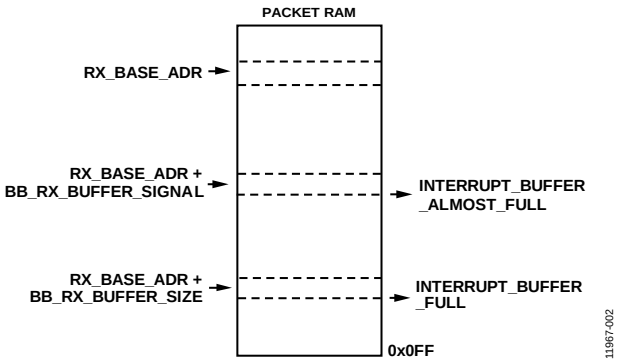

Figure 2. Rolling Buffer in Receive Mode

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