

Differences Between the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) and [ADE7854/ADE7858/ADE7868/ADE7878](#) Products

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INTRODUCTION

The [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) are enhanced versions of the [ADE7854/ADE7858/ADE7868/ADE7878](#) energy measurement ICs. This application note describes the differences between these products and is recommended for use alongside the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) data sheet.

The ICs are pin to pin compatible with the following exception regarding Pin 20, REF_GND. In the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#), it is recommended that REF_GND is tied to ground while in the [ADE7854/ADE7858/ADE7868/ADE7878](#), this pin is a No Connect. Note, however, that there is no degradation of performance even if this pin is left floating in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#).

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REVISION HISTORY

7/14—Revision 0: Initial Version

NEW AND IMPROVED FEATURES

ACCMODE Register Settings

Phase B Voltage Calculation for Delta Configuration

For 3-phase, 3-wire delta configuration, Bits[5:4] (CONSEL[1:0] bits) of the ACCMODE register must be set to 01 in the [ADE7854/ADE7858/ADE7868/ADE7878](#). Because Phase B is used as the reference ground in this configuration, Phase B voltage is not measured. Thus, in the enhanced models, Phase B voltage is calculated as the difference between the voltages of Phase A and Phase C, yielding

$$V_B = V_A - V_C$$

Thus, the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) compute BVRMS in 3-phase, 3-wire delta configuration.

Absolute Reactive Energy Mode

An absolute reactive energy mode is made available in the CFx outputs of [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#). When the VARACC, Bits[1:0] in the ACCMODE register are set to 11, though the reactive powers are accumulated in signed mode in the xVARHR registers, the CFx pulses output energy according to an absolute accumulation.

PSM2 Level Changes

The [ADE7868A/ADE7878A](#) offer an option to select from eight different threshold levels, one being 587 times lower than the analog full-scale level. This allows the user to set much lower thresholds than in the [ADE7868/ADE7878](#). There is also an optional PSM2 $\overline{\text{IRQ1}}$ only mode where $\overline{\text{IRQ0}}$ functionality is disabled. This avoids any glitches in the $\overline{\text{IRQ0}}$ interrupt from erroneously indicating that a tamper condition has or has not occurred.

By default, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ are enabled which results in a larger measurement window than that in the [ADE7868/ADE7878](#). As shown in Table 1, there is a single interrupt mode, which has the same measurement period as in the [ADE7868/ADE7878](#). It is recommended to use the $\overline{\text{IRQ1}}$ only mode, along with an external timer, for quicker tamper detection.

Table 1. PSM2 Level Measurement Window

Product	$\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ Default Mode	$\overline{\text{IRQ1}}$ Only Mode
ADE7868/ADE7878	(LPLINE[4:0] + 1)/50 sec	Mode not available.
ADE7868A/ADE7878A	(LPLINE[4:0] + 10)/50 sec	Measurement period decided by user; external timer can be used. Recommended measurement period: (LPLINE[4:0] + 1)/50 sec.

Calculation of Neutral Current RMS from IA, IB, and IC

The [ADE7868A](#) and [ADE7878A](#) provide the user with the option to compute the sum of the instantaneous phase currents and store it in the NIRMS register, if Bit 0 (the INSEL bit) of the CONFIG_A register is set to 1.

When the INSEL bit is set to 1, the NIRMSOS register does not provide an offset to the NIRMS register. There is also an option to calculate the neutral current rms from the IN channel inputs, such as in the [ADE7868/ADE7878](#), when the INSEL bit is set to 0.

CF Output—Increased Drive Strength

The CF output in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) can sink 8 mA, up from 2 mA, on the [ADE7854/ADE7858/ADE7868/ADE7878](#), which makes it easier to drive LEDs and opto couplers.

Low Ripple RMS Measurements

Apart from the regular rms measurements, a separate set of rms measurements can be taken, using the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) with more averaging. To make these measurements accessible to the user, seven new registers (IARMS_LRIP, VARMS_LRIP, IBRMS_LRIP, VBRMS_LRIP, ICRMS_LRIP, VCRMS_LRIP, and INRMS_LRIP) are provided. These measurements are obtained as a result of averaging 8192 consecutive rms register readings and the registers are updated every 1.024 seconds. The reading settles after 2.048 seconds.

SPI Burst Read Mode

An SPI burst read mode is enabled in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#). Registers from Address 0xE50C through Address 0xE51B, that store the instantaneous current, voltage, and power values on each phase, can be read back continuously with just one command.

Once the start address is made available to the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#), it keeps transmitting the values of successive registers starting at that location, one-by-one, until the last register (0xE51B). The user has the option to terminate the operation by bringing the $\overline{\text{SS}}$ line high at any time during this transfer.

Deglitch Filter

An improved deglitch filter is used in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) that helps prevent high frequency crystal perturbations from affecting the performance of the product.

Communication Verification Registers

Five new registers have been added, LAST_ADDR, LAST_OP, LAST_RWDATA_8, LAST_RWDATA_16, and LAST_RWDATA_32, for communication verification purposes. The LAST_ADDR stores the most recent accessed memory address, LAST_OP stores the recent most performed operation, and the LAST_RWDATA_x registers store the recent most register data corresponding to the last address and operation performed.

Checksum Register

The Checksum (CHECKSUM) register of the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) includes a CRC calculation done on a much wider set of registers than done with the [ADE7854/ADE7858/ADE7868/ADE7878](#). All the configuration registers are now a part of the CRC calculation. Some registers, such as APHCAL, BPHCAL, CPHCAL, and CONFIG_A, are added to the list, along with the register list that already existed in the CRC calculation of the [ADE7854/ADE7858/ADE7868/ADE7878](#). Also, the DSP data memory RAM registers starting from Address 0x4380 through Address 0x43BE, were added to the list. Though the resultant checksum is still a 32-bit register, the number of bits that enter the LFSR is 2344, in the enhanced model. This provides a more comprehensive check of the default settings, when compared to the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#). A CRC interrupt is also made available to the user, which flags any change in the Checksum register.

POR Threshold

The POR threshold has been changed from 2.0 V in the [ADE7854/ADE7858/ADE7868/ADE7878](#) to 2.5 V in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#). This results in a reduction in the supply voltage operation range for the PSM1 and PSM2 levels of the [ADE7868A/ADE7878A](#). The range for the [ADE7868A/ADE7878A](#) is 2.7 V to 3.7 V, instead of 2.4 V to 3.7 V in the [ADE7868/ADE7878](#).

Increased Filtering for Power Computations

An increased filtering option is available to the active and reactive power computations in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#). A stronger low-pass filter (LPF) with twice the settling time, and almost twice the ripple attenuation, is enabled when Bit 1 (the LPFSEL bit) of the CONFIG_A register is set to 1.

Table 2. Increased Power Filtering Option

LPFSEL Bit	Settling Time	Ripple Attenuation
0	650 ms	65 dB
1	1300 ms	128 dB

REGISTER CHANGES AND INCLUSIONS

The [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) contain all [ADE7854/ADE7858/ADE7868/ADE7878](#) registers, with modifications to certain registers. Several new registers are also available in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#).

Table 3 represents all the new registers that have been included in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#), while Table 4 represents the registers that are present in [ADE7854/ADE7858/ADE7868/ADE7878](#) products, but are modified in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#).

Table 3. New Registers

Registers Added	Address Location
IARMS_LRIP	0xE530
VARMS_LRIP	0xE531
IBRMS_LRIP	0xE532
VBRMS_LRIP	0xE533
ICRMS_LRIP	0xE534
VCRMS_LRIP	0xE535
INRMS_LRIP	0xE536
CONFIG_A	0xE740
LAST_OP	0xE7FD
LAST_ADDR	0xE6FE
LAST_RWDATA_8	0xE7FC
LAST_RWDATA_16	0xE6FF
LAST_RWDATA_32	0xE5FF

Table 4. Modified Registers

Registers Modified	Address Location
CHECKSUM	0xE51F
ACCMODE	0xE701
LPOILVL	0xEC00
CONFIG2	0xEC01
STATUS1	0xE503
MASK1	0xE50B

MIGRATING TO THE ENHANCED PRODUCT

Moving over from the [ADE7854/ADE7858/ADE7868/ADE7878](#) to the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) offers multiple advantages. All features available in the [ADE7854/ADE7858/ADE7868/ADE7878](#) are also available for the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#). Further, there is no need to change the layout or evaluation setup when migrating to the enhanced version of the product. The evaluation board, evaluation software, and firmware codes provided for the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#), are backward compatible with the [ADE7854/ADE7858/ADE7868/ADE7878](#) family of parts.

Hardware Compatibility

[ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) products can be used in the application with the same hardware as the [ADE7854/ADE7858/ADE7868/ADE7878](#) products. No design changes are required. The evaluation board for the [ADE7854/ADE7858/ADE7868/ADE7878](#) products can be used to evaluate the enhanced products as well.

Pin 20, REF_GND

This pin, NC, in the [ADE7854/ADE7858/ADE7868/ADE7878](#), is a ground pin in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#). It is recommended to ground this pin externally. This change should not cause any major impact because the recommended layout of [ADE7854/ADE7858/ADE7868/ADE7878](#) recommends grounding the NC pins externally. However, the performance of the A version of the products remains similar to the [ADE7854/ADE7858/ADE7868/ADE7878](#) even when the existing layout has left the pin floating.

Software Compatibility

The microcontroller code and its protocol, developed for the [ADE7854/ADE7858/ADE7868/ADE7878](#) products, works with the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) without requiring any modifications to be made with the exception of the changes described in this section.

LPOILVL Register

The default value of the LPOILVL register remains the same, but the default threshold level and measurement period vary. In the [ADE7854/ADE7858/ADE7868/ADE7878](#), the default threshold level is 7/8th of the full scale; in the enhanced version, the default threshold level is 1/587th of full scale. Similarly, as shown in Table 1, the default measurement window in the enhanced product differs from the [ADE7854/ADE7858/ADE7868/ADE7878](#).

Checksum Register

The default values of the Checksum register in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#) ICs are different from those of the [ADE7854/ADE7858/ADE7868/ADE7878](#) ICs. However, while monitoring the checksum in the application, if the configuration registers are read initially to obtain the default value, and then tracked continuously for changes, then the change in functionality of this register does not cause any problems.

Note that all the configuration registers are now a part of the CRC calculation and thus any change in the value of the registers that have been newly added to the Checksum list are reflected in the value of the Checksum register.

New Functionalities Assigned to Previously Reserved Bits

Some of the reserved bits of the ACCMODE, CONFIG2, STATUS1, and MASK1 registers in the [ADE7854/ADE7858/ADE7868/ADE7878](#) have been assigned new functionalities in the [ADE7854A/ADE7858A/ADE7868A/ADE7878A](#). The operation remains the same when the default values of these bits are preserved.

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