ANALOG DEVICES

AN-1221
APPLICATION NOTE

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Very Low Jitter Encode (Sampling) Clocks for High Speed Analog-to-Digital Converters Using the ADF4002 PLL

CIRCUIT FUNCTION AND BENEFITS

This circuit utilizes the ADF4002 frequency synthesizer to generate a very low jitter encode (sampling) clock to control sampling on the AD9215 analog-to-digital converter. Jitter on the encode clock produces degradation in the overall signal-to-noise ratio (SNR). The relationship is given by the formula

$$SNR = 20 \log_{10}\left(\frac{1}{2\pi f t_j}\right) \qquad (1)$$

where f is the full-scale analog input frequency, and t_j is the rms jitter. "SNR" in Equation 1 is the SNR due solely to clock jitter and does not depend on the resolution of the ADC.

CIRCUIT DESCRIPTION

Table 1. Devices Connected/Referenced

Product	Description
ADF4002	Phase detector/PLL frequency synthesizer
AD9215-80	10-Bit, 65 MSPS/80 MSPS/ 105 MSPS, 3 V ADC
HSC-ADC-EVALB-DCZ	Evaluation board

The ADF4002 consists of a low noise digital phase frequency detector (PFD), precision charge pump, programmable reference divider, and programmable N divider. The 14-bit reference counter (R counter) allows selectable REFIN frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and voltage controlled oscillator (VCO).

Figure 1 shows the ADF4002 with a VCXO to provide the encode clock for a high speed analog-to-digital converter. The converter used in this application is an AD9215-80, a 10-bit converter that accepts up to an 80 MHz encode clock. To realize a stable low jitter clock, use a 77.76 MHz, narrow-band VCXO. This example assumes a 19.44 MHz reference clock. To minimize the phase noise contribution of the ADF4002, the smallest multiplication factor of 4 is used. Thus, the R divider is programmed to 1, and the N divider is programmed to 4. The charge pump output of the ADF4002 (Pin 2) drives the loop filter. The loop filter bandwidth is optimized for the best possible rms jitter, a key factor in the signal-to-noise ratio of the ADC. Too narrow a bandwidth allows the VCXO noise to dominate at small offsets from the carrier frequency. Too wide a bandwidth allows the ADF4002 noise to dominate at offsets where the VCXO noise is lower than the ADF4002 noise. Thus, the intersection of the VCXO noise and the ADF4002 in-band noise is chosen as the optimum loop filter bandwidth.
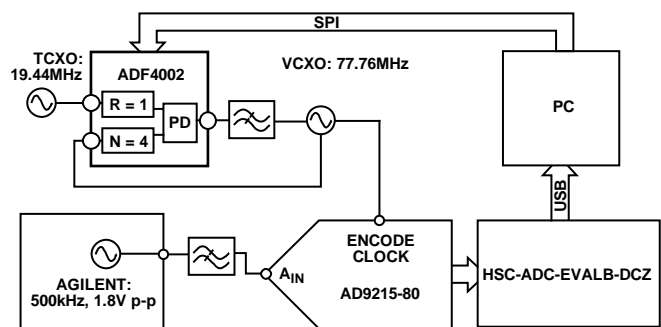

Figure 1. Using the ADF4002 as the Encode (Sampling) Clock for a High Speed ADC

The design of the loop filter uses the ADIsimPLL™ design tool (Version 3.0). This is available as a free download at analog.com/pll. The rms jitter is measured at <1.2 ps, which yields a theoretical SNR (due to jitter only) of 76.4 dB, assuming a 20 MHz input signal and using the above formula given by Equation 1. This value is 17.4 dB greater than the 59 dB SNR specified for the ADC and causes a degradation in overall SNR of only 0.1 dB. If the jitter is increased to 6 ps rms, the corresponding SNR due to jitter at 20 MHz is 62.4 dB, yielding an overall SNR of 57.4 dB.

A low noise, low distortion analog input source is required for accurate measurements. This is achieved using a good quality signal generator followed by a band-pass filter tuned to the frequency of interest. Although the source shown in Figure 1 uses a 500 kHz source, higher frequencies should also be tested. A separate band-pass filter is required for each additional frequency.

The setup shown in Figure 1 using the ADF4002, AD9215, and HSC-ADC-EVALB-DCZ allows the user to quickly and effectively determine the suitability of the converter and encode clock. The SPI interface is used to control the ADF4002, and the USB interface helps control the operation of the AD9215-80. The controller board sends back FFT information to the PC that, if using Analog Devices ADC Analyzer™ software, provides all conversion results from the ADC. Excellent layout, grounding, and decoupling techniques must be used throughout the system to achieve the desired performance.

COMMON VARIATIONS

The PLL-based clock generation circuit shown in Figure 1 is often used to generate a clean, low jitter clock from a noisy system clock. Analog Devices offers a variety of frequency synthesis and clock generation products suitable for similar applications. Refer to analog.com/clock-timing for more information.

LEARN MORE

ADIsimPLL Phase-Locked Loop Circuit Design Software.

HSC-ADC-EVALB-DCZ High Speed ADC Data Capture Kit.

Kester, Walt. 2005. *The Data Conversion Handbook.* Analog Devices. Chapters 6 and 7.

Kester, Walt. 2006. *High Speed System Applications.* Analog Devices. Chapter 2, "Optimizing Data Converter Interfaces,"

Kester, Walt. 2006. *High Speed System Applications.* Analog Devices. Chapter 3, "DACs, DDSs, PLLs, and Clock Distribution."

MT-101 Tutorial, *Decoupling Techniques.* Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of AGND and DGND.* Analog Devices.

Data Sheets and Evaluation Boards

AD9215 Data Sheet.

ADF4002 Data Sheet.

HSC-ADC-EVALB-DCZ Evaluation Board.

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