AN-1145
APPLICATION NOTE

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ADP1047/ADP1048 Advanced Power Metering

by Kevin Huang

INTRODUCTION

The increasingly high cost of energy is pushing data centers and other related computing businesses toward finding intelligent strategies for power management at all levels. The implementation of such strategies requires an accurate collection of data for consumed power down to the power supply level. Today, digital communication techniques and intelligent power supplies make the task easier; however, practical challenges still exist in implementing accurate power measuring because, with a few exceptions, power supplies are not measurement equipment.

Currently, ac power monitoring is implemented in some high end systems, mainly by using dedicated ac power monitors and meters. However, in most cases, only the total rack power is monitored. Because most of these systems require a power factor correction (PFC) stage, where input current and voltage have to be measured by the control loop, it is logical to consider adding power metering within the PFC controller.

The ADP1047/ADP1048 are digital PFC controllers with accurate input power metering capabilities built-in. They provide accurate measurement, such as input and output voltage, input current, and power. The information can be reported to the microcontroller of the power supply via the PMBus interface.

CIRCUIT SETUP AND MEASUREMENT

Figure 1 shows the ac power metering interface. The measured point of the input current is the same as the one used for PFC current loop control. If the current sensing resistor is used, it measures the return current flowing through R_{SENSE} after the main bridge rectifier. The input voltage is rectified through an auxiliary bridge rectifier, divided by the voltage divider (R1 and R2), and then fed into the ADP1047/ADP1048. The advantage of using the auxiliary bridge rectifier is that it can measure the input voltage accurately even during a soft start condition.

This approach measures V and I within the PFC stage. In this case, the measurement is less challenging to perform and does not require isolation; however, it is subject to errors caused by the input bridge and EMI filter. These errors can be particularly significant at light load, when the currents in the EMI filter are comparable to the load currents. By using a proper calibration algorithm, these errors can be mitigated. Two first-order, sigma-delta (Σ-Δ) analog-to-digital converters (ADCs) are used to sense the input voltage and input current. The sampling frequency of the ADCs is 1.6 MHz. True rms values are calculated at the end of each half ac line cycle by integrating the square of the instantaneous values.

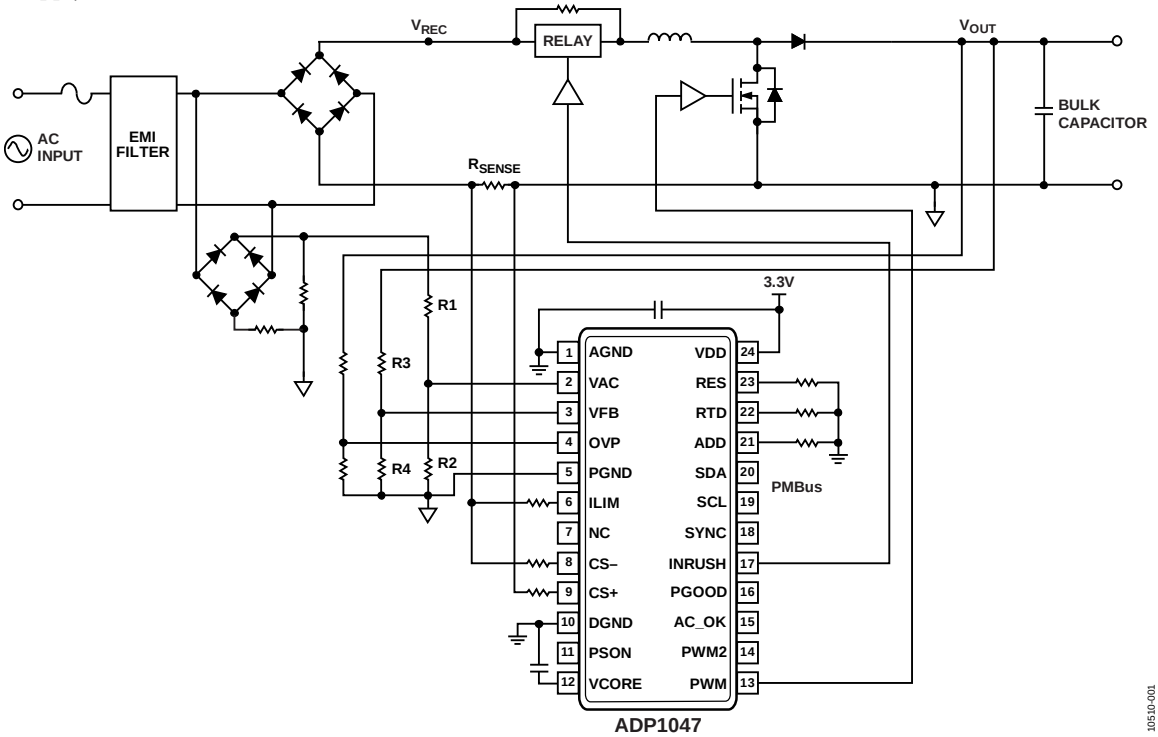

Figure 1. AC Power Metering Circuit Configuration

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REVISION HISTORY

3/12—Revision 0: Initial Version

MEASUREMENT

INPUT VOLTAGE MEASUREMENT

The input voltage is sensed through the voltage divider, R1 and R2, and the divided voltage is fed into the VAC ADC. The ADP1047 can internally calculate the input voltage value according to the VAC ADC reading and the value put in the 0xFE3B register, which is the input voltage resistor divider value.

The input voltage is reported in linear format with a two byte value. Y is an 11-bit, twos complement integer, and N is a 5-bit twos complement integer. Therefore, the real-world value is $X = Y \times 2^N$. The exponent of READ_VIN must be set in Register 0xFE39, Bits[5:3]. The three options available to set the exponent that determines the maximum input voltage are listed in Table 1.

Table 1. VIN Exponent Options and Maximum Input Voltages

Binary of Bits[5:3] of Register 0xFE39	VIN Exponent (N)	Maximum Input Voltage (V)
101	−3	256
110	−2	512
111	−1	1024

For the universal input line, 85 V rms to 265 V rms, the exponent should be −2.

The voltage divider ratio K_{VIN}, which is set in linear format as well, is

$$K_{VIN} = (R2 + R1)/R2$$

The exponent of K_{VIN} is Bits[13:11] of Register 0xFE3B, and the mantissa is Bits[9:0] of Register 0xFE3B. The five exponent values available to program are listed in Table 2.

Table 2. K_{VIN} Exponent Options and Maximum Input Voltage Divider Ratios

Binary of Bits[13:11] of Register 0xFE3B	K_{VIN} Exponent (N)	Maximum Input Voltage Divider Ratio
100	−4	64
101	−3	128
110	−2	256
111	−1	512
000	0	1024

If K_{VIN} = 385, the exponent has be either −1 or 0. Program the mantissa to be $2^{10} \times 385/512$ if the exponent is −1, and program the mantissa to be 385 if the exponent is 0.

INPUT CURRENT MEASUREMENT

The input current sensed signal is fed into the CS+ and CS− pins. The ADP1047/ADP1048 internally calculate the input current value according to the CS ADC reading and the input current sense ratio, IIN_GSENSE, which is set in the 0xFE3C register. The input current sense ratio, IIN_GSENSE = $1/R_{SENSE}$, is set in linear format as well.

The exponent of IIN_GSENSE is Bits[15:11] of the 0xFE3C register, and the mantissa is Bits[9:0] of the 0xFE3C register. There are nine exponent values available to program. Table 3 shows the exponent values and corresponding maximum current sense ratios.

Table 3. IIN_GSENSE Exponent Options and Maximum Current Sense Ratios

Binary of Bits[15:11] of Register 0xFE3C	IIN_GSENSE Exponent (N)	Maximum Current Sense Ratios
10110	−10	1
10111	−9	2
11000	−8	4
11001	−7	8
11010	−6	16
11011	−5	32
11100	−4	64
11101	−3	128
11110	−2	256

For instance, if R_{SENSE} is 50 mΩ, the IIN_GSENSE is 20. To get the best resolution, set the IIN_GSENSE exponent to −5. The mantissa of IIN_GSENSE is $2^{10} \times 20/32$.

The input current is reported in linear format through the PMBus command. The exponent, Bits[10:6] of Register 0xFE39, must be programmed according to the maximum input current specification. To report IIN correctly, the following condition must be satisfied:

$$IIN\_MAX < 2^{11} \times 2^N$$

Therefore,

$$N > \log_2 \frac{IIN\_MAX}{2^{11}}$$

Table 4. IIN Exponent Options and Maximum Input Currents

Binary of Bits[10:6] of Register 0xFE39	IIN Exponent (N)	Maximum Input Current (A)
10110	−10	2
10111	−9	4
11000	−8	8
11001	−7	16
11010	−6	32
11011	−5	64

INPUT POWER MEASUREMENT

The input power is reported with the PMBus command in linear format. There are eight exponent values available to set. The exponent, Bits[2:0] of Register 0xFE39, must be programmed according to the maximum input power specification. To report PIN correctly, the following condition must be satisfied:

$$PIN < 2^{11} \times 2^{N}$$

Therefore,

$$N > \log_2 \frac{PIN}{2^{11}}$$

For example, if the maximum PIN is 600 W, the exponent N should be larger than −2. To get the best resolution, the exponent N should be −1.

Table 5. PIN Exponent Options and Maximum Input Power

Binary of Bits[2:0] of Register 0xFE39	PIN Exponent (N)	Maximum Input Power
101	−3	256
110	−2	512
111	−1	1024
000	0	2048
001	+1	4096
010	+2	8192
011	+3	16384
100	+4	32768

The averaging window is programmable from zero full line cycles to 4096 full line cycles using Bits[2:0] of Register 0xFE3A. At the end of each averaging period, the new value for average power is written to the READ_PIN register (Register 0x97) and is available to be read back through the interface until it is overwritten by the next averaged value at the end of the next averaging period.

OUTPUT VOLTAGE MEASUREMENT

The output voltage is sensed through the voltage divider (R3 and R4), and the divided voltage is fed into the VFB ADC. The ADP1047 internally calculates the output voltage value according to the VFB ADC reading and the value of VOUT_SCALE_MONITOR set in the 0x2A register, which is the output voltage resistor divider value.

The VOUT_SCALE_MONITOR, K, which is set in linear format as well, is

$$K = (R3 + R4)/R4$$

The exponent of K is Bits[13:11] of Register 0x2A, and the mantissa is Bits[9:0]of Register 0x2A. The five exponent values available to program are list in Table 6.

Table 6. VOUT_SCALE_MONITOR Exponent Options

Binary of Bits[13:11] of Register 0x2A	K Exponent (N)	Maximum VOUT_SCALE_MONITOR
100	−4	64
101	−3	128
110	−2	256
111	−1	512
000	0	1024

For best performance, the VFB ADC voltage is recommended to be 1 V. Therefore, if the nominal output voltage is 385 V, the exponent should be −1 for best resolution.

The output voltage is reported in linear format as well. The exponent of READ_VOUT must be set in Bits[2:0]of Register 0x20. The four options available to set the exponent that determines the maximum output voltage are listed in Table 7.

Table 7. V_{OUT} Exponent Options and Maximum Output Voltages

Binary of Bits[2:0] of Register 0x20	V_{OUT} Exponent (N)	Maximum Output Voltage (V)
101	−3	256
110	−2	512
111	−1	1024
000	0	2048

For an output voltage of around 385 V or 400 V, the exponent should be −2.

AC LINE PERIOD MEASUREMENT

The input voltage and current rms values are calculated at the end of each half ac line cycle by integrating the instantaneous values across each line cycle. Line period measurement is a critical step that correctly determines the rms values of the ac input voltage, the current, and, ultimately, the rms ac power.

The controller implements an adaptive algorithm to determine the zero crossing transitions. The interval between two consecutive crossings in the positive and negative direction of an adaptive threshold is measured. The zero crossing is calculated as the middle point of the interval. Once the zero crossing is measured, the interval between zero crossings is the semi period of the ac line. This method allows operating in several different line conditions, providing a reliable indication of the period.

For the dc input system, the ADP1047 uses the value of MAX_AC_PERIOD_SET as the value of period to run the calculation. Therefore, the ADP1047 can also report accurate input voltage, current, and power for the dc input system.

VOLTAGE, CURRENT, AND POWER CALIBRATION

The input voltage and current can be calibrated individually to minimize the error caused by the sensors, as well as those introduced by the ADCs. This calibration is performed via gain and offset adjustments. Once current and voltage are accurate, it is still possible to do further calibration on the power measurement. This offset and gain calibration can be optimized for different line conditions to eliminate the errors introduced by the EMI filter and input bridge rectifier.

Three Σ-Δ ADCs have a digital trimming function in the ADP1047, which include the following:

- VAC_ADC to measure the input voltage
- CS_ADC to measure the input current
- VFB_ADC to measure the feedback voltage

In the Power Supply System Calibration and Trim section of ADP1047/ADP1048 data sheet, only gain trimming is discussed. This application note discusses how to use both the gain trim and offset trim.

Ten registers are used for these digital trimmings. The meanings of the register and how to set these numbers is discussed in the following sections.

These 11 8-bit registers include the following:

- VAC ADC offset trim (Register 0xFE53)
- VAC ADC gain trim (Register 0xFE40)
- CS ADC offset trim (Register 0xFE54 and Register 0xFE7F)
- CS ADC gain trim (Register 0xFE42 and Register 0xFE7E)
- VFB ADC gain trim (Register 0xFE41)
- Power metering offset trim for low line input register (Register 0xFE33)
- Power metering gain trim for low line input register (Register 0xFE34)
- Power metering offset trim for high line input register (Register 0xFE8E)
- Power metering gain trim for high line input register (Register 0xFE8F)

TRIMMING

INPUT VOLTAGE DIGITAL TRIMMING

The VAC ADC offset trim register trims the offset error of the input voltage, and the VAC ADC gain trim register trims the gain error of the input voltage.

Input Voltage Digital Trimming Register Definition

The following lists the register definitions for the VAC ADC offset trim and VAC ADC gain trim registers:

- $Offset\ error = (\frac{VAC\ ADC\ offset\ trim[7:0]}{2^{11}}) \times 1.6 \times K_{VIN}$

  When the VAC ADC offset trim register, Bits[7:0] = 0x0, the offset range is 0, and when the VAC ADC offset trim register, Bits[7:0] = 0xFF , the offset is 12.5% of the full input range, which is 1.6 V × K_{VIN}.
- When $1 - \frac{VIN}{VIN\_R} > 0$, $VAC\ ADC\ gain\ trim[7] = 1$
- When $1 - \frac{VIN}{VIN\_R} \leq 0$, $VAC\ ADC\ gain\ trim[7] = 0$

  where:
  VIN is the reading of the input voltage from a calibrated multimeter.
  VIN_R is the reading of input voltage from the ADP1047/ADP1048.
- $Gain\ error = \frac{VAC\ ADC\ gain\ trim[6:0]}{2^{11}}$

  When the VAC ADC gain trim register, Bits[7:0] = 0x0, the gain error is zero; when the VAC ADC gain trim register, Bits[7:0] = 0xFF, the gain error is −6.2%; and when the VAC ADC gain trim register, Bits[7:0] = 0x7F, the gain error is +6.2%.

Input Voltage Digital Trimming Trim Steps

The trim steps for the input voltage digital trimming include the following:

1. Apply a zero input voltage to the PFC and read the READ_VIN register. In addition, adjust the VAC ADC offset trim register value until the mantissa of the READ_VIN register is 0.
2. Connect a calibrated multimeter to the input terminal of the PFC circuit. Apply a 110 V ac input voltage to the PFC circuit and set the load to a full load condition. Adjust the VAC ADC gain trim register until the READ_VIN register equals the input voltage reading from the multimeter.

$$VAC\ ADC\ offset\ trim[6:0] = \left|\frac{VIN}{VIN\_R} - 1\right| \times 2^{11}$$

CS ADC DIGITAL TRIMMING

The CS ADC offset trim register trims the offset error of the PFC input current, and the CS ADC gain trim register trims the gain error of the PFC input current. Because the CS ADC input range has 500 mV and 750 mV options, the trim registers are, respectively, available for each range selection.

CS ADC Digital Trimming Register Definition

The following lists the register definitions for the CS ADC offset trim and CS ADC gain trim registers:

- $Offset\ error = (\frac{CS\ ADC\ offset\ trim[7:0]}{2^{11}}) \times \frac{CS\_RANGE}{RSENSE}$

  CS_RANGE is 500 mV or 750 mV as determined by the user selection. Bit[1] of the register sets the CS ADC input range. When the CS ADC offset trim register, Bits[7:0] = 0x0, the offset range is 0, and when the CS ADC offset trim register, Bits[7:0] = 0xFF, the offset is 12.5% of the full input current range, which is CS_RANGE/R_{SENSE}.
- $Gain\ error = \frac{CS\ ADC\ gain\ trim[6:0]}{2^{11}}$

  When the CS ADC gain trim register, Bits[7:0] = 0x0, the gain error is zero; when the CS ADC gain trim register, Bits[7:0] = 0xFF, the gain error is −6.2%; and when the CS ADC gain trim register, Bits[7:0] = 0x7F, the gain error is +6.2%.

CS ADC Digital Trimming Trim Steps

The trim steps for the CS ADC digital trimming include the following:

1. The CS ADC gain trim register and the CS ADC offset trim register are set to 0. Use a calibrated multimeter to measure the input current.
2. Apply a 110 V ac input voltage to the PFC, set the load to half of the full load, and read READ_IIN; this number is IIN_Y1 in terms of current. Under this condition, the multimeter reading of the input current is IIN_X1.
3. Set the load to full load and read READ_IIN; this number is IIN_Y2 in terms of current. Under this condition, the multimeter reading of the input current is IIN_Y2. The input current offset error is

$$IIN\_OFF\_ERR = \frac{IIN\_X1 \times IIN\_Y2 - IIN\_X2 \times IIN\_Y1}{IIN\_X1 - IIN\_X2}$$

$$\text{CS ADC offset trim}[7:0] = IIN\_OFF\_ERR \times 2^{11}$$

4. Set the load to full load and read READ_IIN; this number is IIN_R in terms of current. Under this condition, the multimeter reading of the input current is IIN.

   When $1-\frac{IIN}{IIN\_R} > 0$, *CS ADC gain trim[7]* = 1

   When $1-\frac{IIN}{IIN_R} \leq 0$CS, *ADC gain trim[7]* = 0

   $$CS\ ADC\ gain\ trim[6:0] = \left|\frac{IIN}{IIN\_R}-1\right|\times 2^{11}$$

Note that the previous trim step can be used for both of the CS ADC input ranges.

VFB ADC DIGITAL TRIMMING

The VFB ADC gain trim register trims the gain error of the output voltage. No offset trimming was designed for trimming the offset error of the output voltage. The actual output voltage is defined as V_{OUT}, and the ideal output voltage is defined as V_{REF}.

VFB ADC Digital Trimming Register Definition

The following lists the register definitions for VFB ADC gain trim register:

- When $1-\frac{V_{REF}}{V_{OUT}} > 0$, *VFB ADC gain trim[7]* = 1
- When $1-\frac{V_{REF}}{V_{OUT}} \leq 0$, *VFB ADC gain trim[7]* = 0
- $Gain\ error = \frac{VFB\ ADC\ gain\ trim[6:0]}{2^{11}}$

  When the VFB ADC gain trim register, Bits[7:0] = 0x0, the gain error is zero; when the VFB ADC gain trim register, Bits[7:0] = 0xFF, the gain error is −6.2%; and when the VFB ADC gain trim register, Bits[7:0] = 0x7F, the gain error is 6.2%.

VFB ADC Digital Trimming Trim Steps

The trim steps for the VFB ADC digital trimming include the following:

1. Turn on the PFC circuit. Use a calibrated multimeter to perform the output voltage reading.
2. Adjust the VFB ADC gain trim register (Register 0xFE41) until the power supply outputs the exact value in the READ_VOUT register (Register 0x8B).

   $$VFB\ ADC\ gain\ trim[6:0] = \left|\frac{V_{REF}}{V_{OUT}}-1\right|\times 2^{11}$$

POWER METERING DIGITAL TRIMMING

The power metering offset trim for the low line input register is designed to correct the offset error to the input power measurement under the low line input. The power metering gain trim for the low line input register is designed to correct the gain error of the input power measurement under the low line input.

The power metering offset trim for the high line input register is designed to correct the offset error to the input power measurement under the high line input. The power metering gain trim for high line input register is designed to correct the gain error of the input power measurement under the high line input.

These four registers are designed for customers to compensate power loss of the EMI filter and bridge rectifier.

Power Metering Digital Trimming Register Definition

The following lists the register definitions for the power metering offset trim for the low line input register, the power metering gain trim for low line input register, the power metering offset trim for high line input register, and the power metering gain trim for high line input register.

For low line input,

- $Offset\ error = \left(\frac{Power\ Metering\ Offset\ Trim\ for\ Low\ Line\ Input\ [6:0]}{2^{11}}\right)\times 1.6\times K_{VIN}\times\frac{CS\_RANGE}{RSENSE}$

  When the power metering offset trim for low line input register, Bits[7:0] = 0x0, the offset range is 0; when the power metering offset trim for low line input register, Bits[7:0] = 0x7F, the offset is +6.2% of the full power; and when the power metering offset trim for low line input register, Bits[7:0] = 0xFF, the offset is −6.2% of the full power.
- $P_{FULL}\ (the\ full\ power) = 1.6\times K_{VIN}\times\frac{CS\_RANGE}{RSENSE}$
- $Gain\ error = \frac{Power\ Metering\ Gain\ Trim\ for\ Low\ Line\ Input[6:0]}{2^{11}}$

  When the power metering gain trim for low line input register, Bits[7:0] = 0x0, the gain error is zero; when the power metering gain trim for low line input register, Bits[7:0] = 0xFF, the gain error is −6.2%; and when power metering gain trim for low line input register, Bits[7:0] = 0x7F, the gain error is +6.2%.

For the high line input,

- *Offset error* = $\left(\frac{Power\ Metering\ Offset\ Trim\ for\ High\ Line\ Input\ [6:0]}{2^{11}}\right)\times 1.6\times K_{VIN}\times\frac{CS\_RANGE}{RSENSE}$

  When the power metering offset trim for high line input register, Bits[7:0] = 0x0, the offset range is 0; when the power metering offset trim for high line input register, Bits[7:0] = 0x7F, the offset is +6.2% of the full power; and when the power metering offset trim for high line input register, Bits[7:0] = 0xFF, the offset is −6.2% of the full power.
- *Gain error* = $\frac{Power\ Metering\ Gain\ Trim\ for\ High\ Line\ Input[6:0]}{2^{11}}$

  When the power metering gain trim for high line input register, Bits[7:0] = 0x0, the gain error is zero; when the power metering gain trim for high line input register, Bits[7:0] = 0xFF, the gain error is −6.2%; and the when power metering gain trim for high line input register, Bits[7:0] = 0x7F, the gain error is +6.2%.

Power Metering Digital Trimming Trim Steps

The trim steps for the power metering digital trimming include the following:

1. The power metering offset trim for low line input register and the power metering gain trim for low line input register are set to zero. Apply a 110 V ac input voltage to the PFC circuit.
2. Set the load to 20% of full load. Read the READ_PIN register and the reading is recorded as P_{m1}. The input power reading from a calibrated power meter is recorded as P_1.
3. Set the load to full load. Read the READ_PIN register and the reading is recorded as P_{m2}. The input power reading from a calibrated power meter is recorded as P_2.

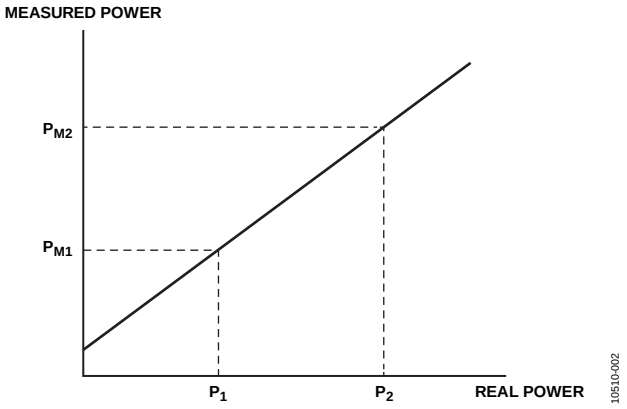

Figure 2. Measured Power vs. Real Power

4. Based on these points, the offset error and gain error can be calculated as follows:

   $Offset\ error = \frac{P_1P_{m2}-P_2P_{m1}}{P_1-P_2}$

   $Gain\ error = \left|\frac{P_1-P_2}{P_{m1}-P_{m2}}-1\right|$
5. Power metering offset trim for the low line input register:

   when $\frac{P_1P_{m2}-P_2P_{m1}}{P_1-P_2}\geq 0$ Bit[7] = 0.

   ,

   Power metering offset trim for the low line input register:

   when $\frac{P_1P_{m2}-P_2P_{m1}}{P_1-P_2}<0$ Bit[7] = 1.

   ,

   Power metering offset trim for the low line input register,

   $Bit[6:0] = \frac{P_1P_{m2}-P_2P_{m1}}{P_1-P_2}\times\frac{2^{11}}{P_{FULL}}$.

   Power metering gain trim for low line input register,

   when $1-\frac{P_1-P_2}{P_{m1}-P_{m2}}>0$ Bit[7] = 1.

   ,

   Power metering gain trim for the low line input register,

   when $1-\frac{P_1-P_2}{P_{m1}-P_{m2}}\leq 0$, Bit[7] = 0.

   Power metering gain trim for the low line input register,

   $Bit[6:0] = \left|\frac{P_1-P_2}{P_{m1}-P_{m2}}-1\right|\times 2^{11}$.
6. The power metering gain trim for the high line input register and the power metering offset trim for the high line input register are set to zero. Apply 230 V ac input voltage to the PFC circuit.
7. Repeat Step 2 to Step 4.
8. Power metering offset trim for the high line input register,

   when $\frac{P_1P_{m2}-P_2P_{m1}}{P_1-P_2}\geq 0$ Bit[7] = 0.

   ,

   Power metering offset trim for the high line input register,

   when $\frac{P_1P_{m2}-P_2P_{m1}}{P_1-P_2}<0$ Bit[7] = 1.

   ,

   Power metering offset trim for the high line input register,

   $Bit[6:0] = \frac{P_1P_{m2}-P_2P_{m1}}{P_1-P_2}\times\frac{2^{11}}{P_{FULL}}$.

   Power metering gain trim for the high line input register,

   when $1-\frac{P_1-P_2}{P_{m1}-P_{m2}}>0$ Bit[7] = 1.

   ,

   Power metering gain trim for the high line input register,

   when $1-\frac{P_1-P_2}{P_{m1}-P_{m2}}\leq 0$, Bit[7] = 0.

   Power metering gain trim for the high line input register,

   $Bits[6:0] = \left|\frac{P_1-P_2}{P_{m1}-P_{m2}}-1\right|\times 2^{11}$.

EXPERIMENTAL RESULT

Measurements were performed on a 300 W demonstration board implemented using the ADP1047. The demonstration board is designed to operate at 100 kHz in CCM, and the output voltage is regulated at 385 V.

Figure 3 shows the measured power error compared with the commercial power meter under a wide input range with an ideal input source. The test is done at room temperature at 25°C. Figure 4 through Figure 7 show the experimental results for nonideal sinusoidal ac line voltages at 25°C. In addition, Figure 4 through Figure 7 show the benefits of true rms power measurements so that the accuracy can be maintained even with nonideal ac line voltages. Note that the rectified input voltage for the input ac source shown in Figure 6 is approximately similar to the dc input voltage.

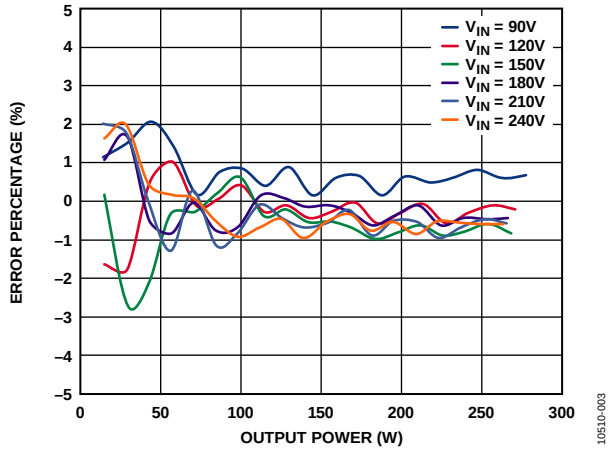

Figure 3. Measured Power Error with Ideal Input AC Source

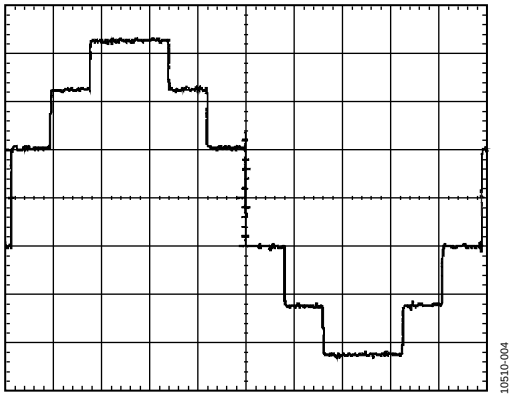

Figure 4. Nonideal Input AC Source 1 Waveform

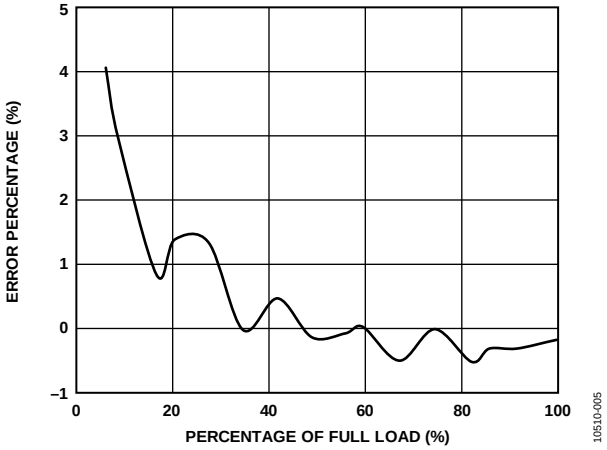

Figure 5. Measured Power Error with Nonideal Input AC Source 1

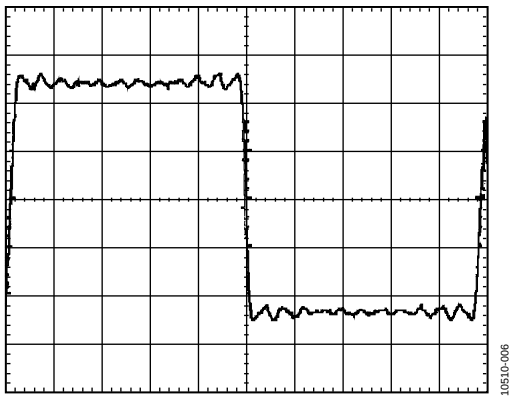

Figure 6. Nonideal Input AC Source 2 Waveform

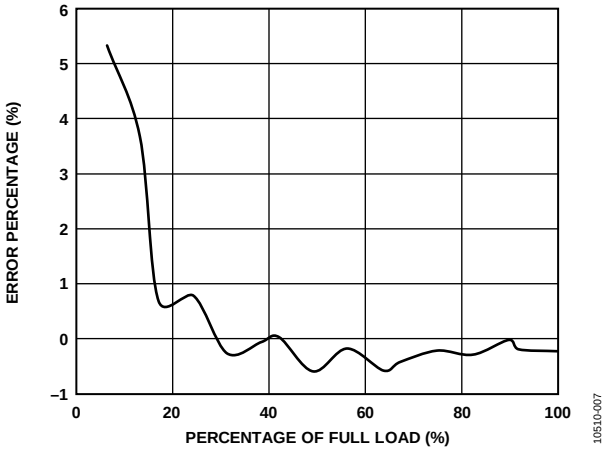

Figure 7. Measured Power Error with Nonideal Input AC Source 2

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