ANALOG DEVICES

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APPLICATION NOTE

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An Improved Topology for Creating Split Rails from a Single Input Voltage

by Kevin Tompsett

INTRODUCTION

Even with the widespread use of rail-to-rail single supply op amps, there is still often the requirement for dual rails (for example, ±15 V) to be generated from a single (positive) input power rail to power different parts of the analog signal chain. These are often low current (such as 10 mA to 500 mA) with relatively well-matched loads on the positive and negative supplies.

One solution to this problem is to use two different converters; one to provide the positive rail and one to provide the negative rail. This can be expensive and, as this application note shows, unnecessary. Another solution is using a flyback; however, the supplies tend not to track each other very well with differential loading, it requires a large and expensive transformer, and it tends to be inefficient.

A better solution is a SEPIC-Ćuk converter. This topology consists of an unregulated Ćuk converter tied to the same switching node as a regulated SEPIC converter. This combination results in two supplies that track each other very well under all but a 100% load mismatch.

An analysis of the converter's operation and implementation using the Analog Devices, Inc., ADP161x demonstrates the versatility of this topology. In addition, a revolutionary new design tool is introduced, providing a quick path to implementing a SEPIC-Ćuk in user applications.

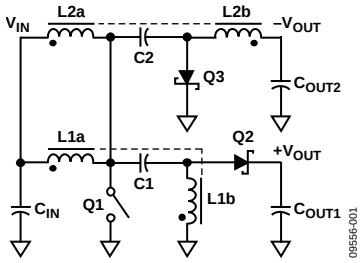

Figure 1. Schematic of the SEPIC-Ćuk Converter

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REVISION HISTORY

7/13—Rev. 0 to Rev. A

Changes to Figure 8 6

7/11—Revision 0: Initial Version

DESCRIPTION OF TOPOLOGY

Initially, the SEPIC-Ćuk appears to be a complicated converter with four different inductors and switches. Fortunately, it can be broken down into its two constituent converters, simplifying the analytical problem. For a SEPIC or Ćuk converter, the Q1 and Q2 switches operate in the opposite phase from one another. Figure 2 shows the current flow diagram for the two different switch states in a SEPIC converter.

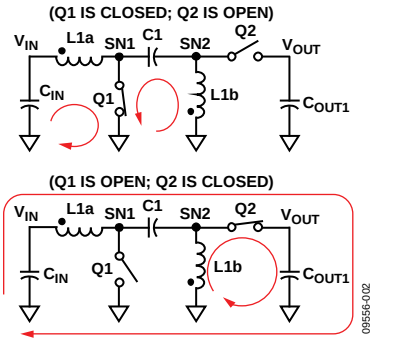

Figure 2. Current Flow in a SEPIC Converter

It is not immediately obvious, but the transfer capacitor (C1) voltage is approximately constant V_{IN} (with small ripple).

Figure 4 shows the idealized waveforms for a SEPIC converter. When Q1 is on, the voltage at SN2 is equal to $-V_{IN}$. Thus, during the time that Q1 is on (Q2 is off), the voltage across both L1a and L1b is V_{IN} and when Q1 is off (Q2 is on), then the voltage across both L1a and L1b is $-V_{OUT}$. Applying the principles of inductor-volt second balance, the equilibrium dc conversion ratio as shown in Equation 1 can be calculated. D is the converter's duty cycle (the fraction of the switching cycle that Q1 is on).

$$\frac{V_{OUT\,SEPIC}}{V_{IN}} = \frac{D}{(1-D)} \quad (1)$$

The Ćuk converter operates in a similar manner to the SEPIC converter, however, in this case, Switch Q2 is connected to ground rather than the output and the Inductor L2b is connected to the output instead of ground. Figure 3 shows a current flow diagram for the Ćuk converter during both switch positions.

The Ćuk is a negative output converter, so current flowing out of the load is actually delivering power to the output.

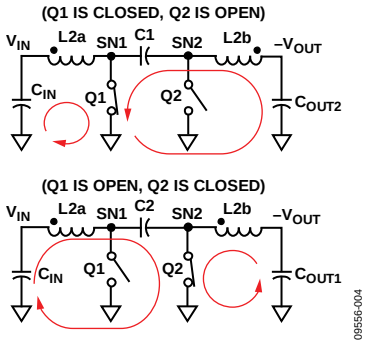

Figure 3. Current Flow in a Ćuk Converter

The idealized waveforms for a Ćuk converter are shown in Figure 4. Applying the principles of inductor-volt second balance and capacitor charge balance, the voltage across C2 is $V_{IN} + V_{OUT}$. Therefore, the SN2 switch node switches between GND, when Q2 is closed, and $-(V_{IN} + V_{OUT})$. The voltage across both L2a and L2b while Q1 is on (Q2 is off), is V_{IN} and, while Q1 is off (Q2 is on), the voltage across both L2a and L2b is $-V_{OUT}$.

Comparing the waveforms in Figure 4 and Figure 5, note that the voltages across the inductors in a Ćuk are identical to those for the SEPIC. Thus, the duty cycle equation for a Ćuk is simply negative the duty cycle for the SEPIC,` as shown in Equation 2.

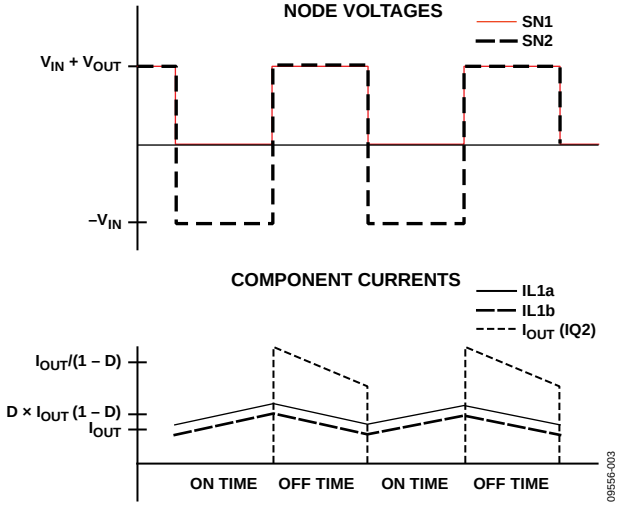

Figure 4. Idealized Waveforms SEPIC

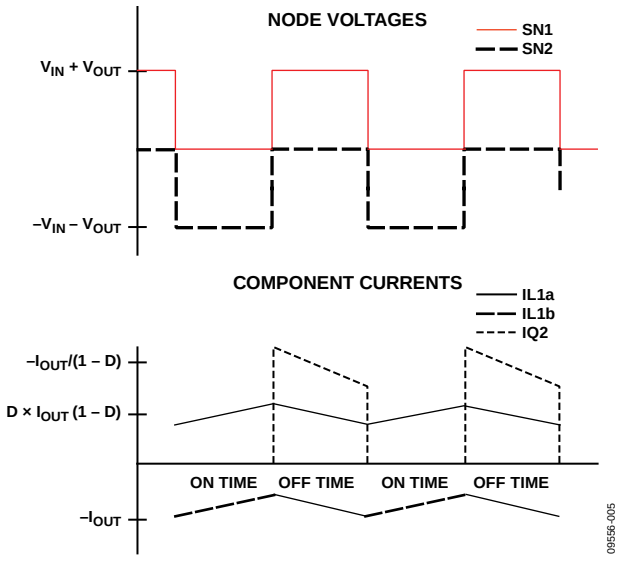

Figure 5. Idealized Waveforms Ćuk

$$\frac{V_{OUT\,Cuk}}{V_{IN}} = \frac{-D}{(1-D)} \tag{2}$$

The fact that the duty cycles are equal and opposite, the switch node (SN1) voltages are identical, and the inductor currents are identical is what makes it possible to simply attach the two converters together at Node SN1. The combined converter is shown in Figure 1.

Q2 and Q3 have been replaced by diodes because these supplies are generally lower power analog supplies where an asynchronous controller makes good sense. In addition, two inductors (L1a and L2a) are in parallel. The reason for this is that L1a and L1b, and L2a and L2b, are coupled together using two separate coupled inductors. This has multiple advantages.

Coupling the inductors reduces current ripple in the inductors by a factor of two (see the Ćuk-Middlebrook paper cited in the References section). In addition, it significantly reduces the complexity of the small signal model and enables higher bandwidth by eliminating the SEPIC and Ćuk resonances located according to Equation 3 and Equation 4. This enables the use of a wide variety of off-the-shelf parts since there are not many three winding 1:1:1 inductors available.

$$f_{\text{SEPIC resonance}} = \frac{1}{2\pi\sqrt{(L_{1a}+L_{1b})C_1}} \tag{3}$$

$$f_{\text{Cuk resonance}} = \frac{1}{2\pi\sqrt{(L_{2a}+L_{2b})C_2}} \tag{4}$$

A six winding part, such as found in Coilcraft's Hexapath line product line, or a custom three winding transformer could also be used.

LIMITS TO THE COUPLING COEFFICIENT

Even though coupling the inductors has distinct advantages, it is undesirable for the coupling to be tight enough for there to be significant energy transfer through the core. To avoid this situation, the designer must ensure that the magnitude of the complex impedance of C1 (and C2) at the switching frequency is less than a tenth that of the impedance of the leakage inductance (L_{LKG}) plus the DCR of a single winding.

This inequality is designated in Equation 5. The leakage inductance (L_l) can be calculated using Equation 6 and the coupling coefficient (K) generally found on coupled inductor data sheets. L_m is the measured self-inductance that appears in the data sheet. Note that in Equation 5, the x in C_x and L_x refers to either C1 or C2 or L1 or L2.

$$|Z_{C_x}| = \sqrt{ESR_{C_x}{}^2 + \left(\frac{1}{2\pi C_{C_x} f_{sw}}\right)^2} \le \frac{|Z_{L_{lkg\,L_x}}|}{10} = \frac{\sqrt{DCR_{L_x}{}^2 + 2\pi L_{L_{lkg\,L_x}}}}{10} \tag{5}$$

$$L_{lkg} = L_m(1-K) \tag{6}$$

DIFFERENTIAL LOAD AND OUTPUT VOLTAGE TRACKING

By nature, the Ćuk (negative) output of the SEPIC-Ćuk is unregulated; thus, there is some amount of load variation with changes in output current and, particularly with load mismatch, compared to the SEPIC (positive) output. Note that the tracking is much better than a similarly configured flyback converter, especially in the case of a transient or a load mismatch. This is because the coupling between channels is a direct connection rather than through the transformer with its inherent leakage inductance.

Figure 6 shows a 30 mA transient applied to the Ćuk ($-V_{OUT}$) output of a SEPIC-Ćuk converter, while a constant 100 mA remains on the SEPIC output. It shows that both outputs respond to the transient load. This is the worst-case transient because the Ćuk output is unregulated. Interestingly, most of the deviation shown on the $-V_{OUT}$ rail is actually dc regulation shift caused by the mismatch between the loads applied to the two rails ($I_{OUT}+$, $I_{OUT}-$).

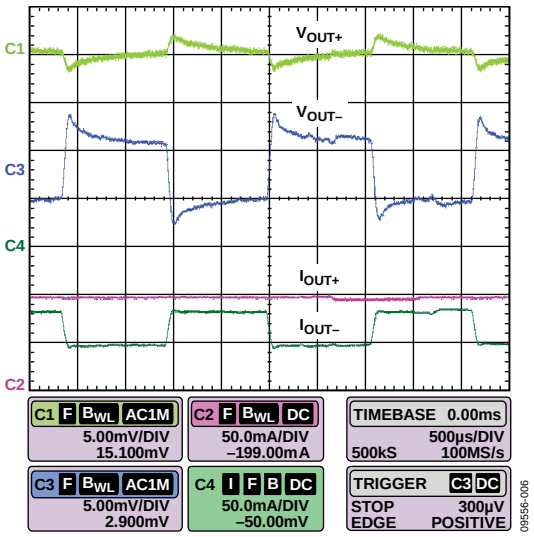

Figure 6. Transient Response from a 30 mA Step Load Applied to the Negative (Ćuk) Output

With an identical load on both supplies, at steady state, the most significant error terms are a mismatch in the DCR of the inductors and the forward voltage of the diodes, both of which can be made quite small relative to the output voltage.

With substantial load mismatch, the error grows as shown in Figure 7. Therefore, in some applications it may be necessary to put a small dummy load on one or both of the channels to keep both supplies in their regulation window. Note that, in general, analog chips, like op amps, are largely insensitive to dc changes in their power supplies as long as there is sufficient head room available.

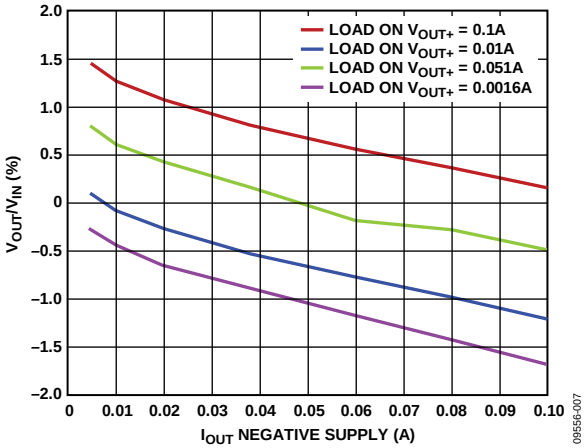

Figure 7. Relative Voltage Regulation Between Rails with Differential Loading

SMALL-SIGNAL ANALYSIS AND LOOP COMPENSATION

A complete small-signal analysis of the SEPIC-Ćuk converter is beyond the scope of this paper; however, the equations provided in this application note should allow the designer to correctly compensate their design. The ADP161x SEPIC-Ćuk design tool uses a more complete model which is more accurate, but much more complicated. The equations shown refer to the ADP161x part in SEPIC-Ćuk and may not be accurate for other parts made by Analog Devices or the company's competitors.

The small-signal model for a SEPIC-ĆUK looks very similar to a SEPIC converter with no attached Ćuk as long as a few design requirements are met. It is assumed that identical inductors are used on the SEPIC-Ćuk rails. This requirement makes sense because both outputs are designed for the same voltage and current.

In their paper, Ćuk and Middlebrook (see the References section) show that a coupled inductor, from both a small signal and a large signal, behaves like an inductor with twice its single winding inductance value, without the SEPIC or Ćuk resonances. Therefore, analysis in this application note is shown using the effective inductance, that is, twice the single winding inductance value that appears on coupled inductor data sheets. The analysis assumes identical resistive loads, though the converter remains stable with significant load imbalance. The two transfer capacitances (C1 and C2) should be nearly the same value, erring on the side of having C2 slightly larger than C1. These are assumed to be ceramic capacitors and, thus, the designer needs to take into account the differences in their dc bias value when calculating their effective capacitances.

The first step in compensating a SEPIC Ćuk is to choose an achievable target crossover frequency. Like most boost and buck-boost topologies, the SEPIC-Ćuk has a right half plane zero (RHP) located according to Equation 7. An RHP has the dual effect of adding gain, like a zero, and subtracting phase, like a pole. Therefore, the converter must be compensated for a crossover frequency a maximum of one fifth of the frequency of the RHP (f_{RHP}).

The SEPIC-Ćuk has an additional resonance caused by the leakage inductance (L_{lkg}) and transfer capacitance (C1) that occurs at F_{res}. This resonance is generally well damped by the DCR of the inductors, but can introduce significant phase lag; therefore, it is good to crossover at least a decade before it. In addition, a current mode controller with standard Type II compensation is used, thus, the maximum achievable crossover frequency is approximately one-tenth the switching frequency. Target f_u should, therefore, be chosen as the minimum of these three constraints, as shown in Equation 9.

$$f_{RHP} = \frac{R_{LOAD}\, D_{Q2}^{1.5}}{L \times D_{Q1}} \quad (7)$$

$$f_{res} = \frac{1}{2\pi\sqrt{L_{lkg} C_1}} \quad (8)$$

$$f_u = minimum\left(\frac{f_{RHP}}{5}, \frac{f_{res}}{10}, \frac{f_{fsw}}{10}\right) \quad (9)$$

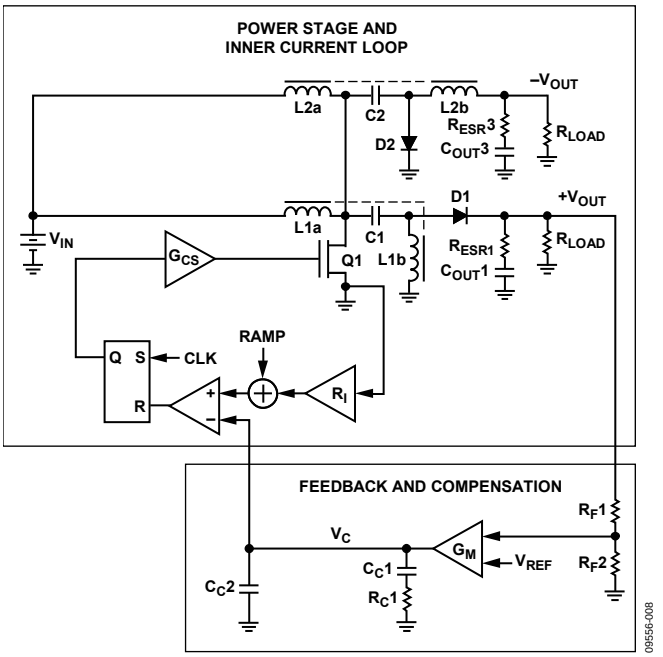

Figure 8. Block Diagram Showing Power Stage and Compensation Components

The compensation values in Figure 8 can be calculated as follows. Since it is assumed ceramic output capacitors will be used, C_C2 can be selected as 10 pf.

$$C_{C1} = -C_{C2} + \sqrt{\frac{V_{REF}^2 G_m^2 A_c^2}{4\pi^2 V_{OUT}^2}\left(\frac{1}{f_p^2} + \frac{1}{f_u^2}\right) - C_{C2}^2\left(\frac{1}{2} + \frac{f_u^2}{f_p^2}\right)} \quad (10)$$

$$R_c = \frac{1}{2\pi f_p C_{C1}} \quad (11)$$

where:

f_p is the dominant pole for the current mode converter with some correction factors to account for ramp compensation and finite current gain.

$$f_p = \frac{(1-D_{off})^{0.25}}{\left(\frac{D_{off} M_c}{D_{on}}\right)^{0.45}} \frac{2}{(C_{out1} + C_{out3} + C_2)R_{LOAD}} \quad (12)$$

A_c is the magnitude of the open-loop converter gain at the crossover frequency f_u.

$$A_c = \frac{F_m}{2D_{on}D_{off}\left(1 + \frac{F_m V_{out}(1+D_{on})}{D_{on}D_{off}^2 R_{load}}\right)} \frac{\sqrt{1+\left(\frac{f_u}{f_{rhp}}\right)^2}}{\sqrt{1+\left(\frac{f_u}{f_p}\right)^2}} \quad (13)$$

M_c and F_m are terms derived from Ridley's thesis (see the References section) on current mode control.

$$M_c = 1 + \frac{V_{RAMP} f_{sw} L_1 A_{cs}}{2 V_{IN}} \quad (14)$$

$$F_m = \frac{L f_{sw} A_{cs}}{4 M_c V_{IN}} \quad (15)$$

V_{ramp} and A_{cs} are fixed constants within the chip.

$$V_{RAMP} = 0.1 \text{ (ADP1612/ADP1613)} \quad (16)$$

$$A_{cs} = 13.5 \text{ (ADP1612/ADP1613)} \quad (17)$$

POWER COMPONENT STRESS

As is often the case, a 30% ripple in the inductors generally results in a reasonable value (see Equation 19). However, with large step down ratios it can be more optimal to increase this ripple percentage in the input inductor to 50% or 60%.

$$I_{IN} = \frac{V_{OUT} I_{OUT}}{V_{IN}} \text{ (into each inductor L1a and L2 a)} \quad (18)$$

$$\Delta I_L = 0.3 I_{IN} \quad (19)$$

$$I_{pkLx_a} = I_{IN} + \frac{\Delta I_L}{2} \quad (20)$$

$$I_{pkLx_b} = I_{OUT} + \frac{\Delta I_L}{2} \quad (21)$$

$$L1 = \frac{V_{IN} V_{OUT}}{(V_{IN} + V_{OUT}) f_{sw} \Delta I_L} \quad (22)$$

The currents in the FET Switch Q1 and the two diode switches, Q2 and Q3, are shown in Figure 9. The dc components of the switch current are also shown in Figure 9. Note that Q1 carries the current for both the SEPIC and the Ćuk rails. The peak currents depend on the ripple chosen in Equation 19.

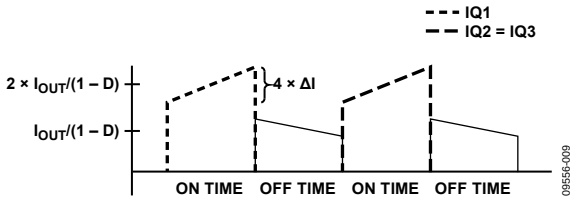

Figure 9. Idealized Waveforms for SEPIC-Ćuk

Calculating the switching loss in the primary Switch Q1 is beyond the scope of this application note. Note that, in many cases, the switching loss can be quite large since the voltage swing the switch sees is large (~V_{IN} + V_{OUT}) and so are the currents (see Figure 9).

The ADP1612/ADP1613 work to reduce this loss by switching very quickly. The FET chosen must be rated to withstand at least V_{IN} + V_{OUT} and good engineering allows some margin for switch node ringing due to stray inductances, in addition to thermal stress from RDS on loss and switching losses.

The peak-to-peak output voltage ripple on the SEPIC (positive) output is ($\Delta V_{ripple\ SEPIC}$) and is approximated by

$$\Delta V_{ripple\ SEPIC} \approx \frac{I_{OUT} D_{ON}}{f_{sw} C_{OUT1}} + ESR_{COUT1} \times I_{OUT}(1 - D_{ON}) \quad (23)$$

The value of the current through the capacitor ($I_{RMS\ Cout\ SEPIC}$) is

$$I_{rms\_COUT\_SEPIC} = \frac{I_{OUT} D_{ON}}{(1 - D_{ON})} \sqrt{1 + \left(\frac{1}{3}\right)\left(\frac{\Delta I_L (1 - D_{ON})}{2 I_{OUT}}\right)^2} \quad (24)$$

The peak-to-peak output voltage ripple on the Ćuk (negative) output ($\Delta V_{ripple\ Ćuk}$) is approximated by

$$\Delta V_{ripple\ Cuk} \approx \frac{\Delta I_L D_{ON}}{8 f_{sw} C_{OUT3}} + ESR_{COUT3} \times I_L \quad (25)$$

The I rms value of the current into the C_{OUT} on the Ćuk (negative) output ($\Delta V_{rip\ Ćuk}$) is approximated by

$$I_{rms\_COUT\_Cuk} = \frac{\Delta I_L}{\sqrt{3}} \quad (26)$$

The ripple on C1 and C2 should be chosen for around 5% of V_{IN}. As stated earlier, they should have similar values despite the difference in dc voltage across them.

$$V_{ripple\_Cx} = \frac{(1 - D_{ON}) I_{IN}}{f_{sw} C_1} + I_{IN} ESR_{C_x} \quad (27)$$

It is important to consider I rms ratings when choosing C1 and C2 since the current through them is quite large.

$$I_{rms\_C1 \times C2} = \sqrt{\frac{(1 - D_{ON})}{3}\left(I_{pk\_L_{xa}}{}^2 + I_{pk\_L_{xa}}\left(I_{IN} - \frac{\Delta I_L}{2}\right) + \left(I_{IN} - \frac{\Delta I_L}{2}\right)^2\right) + \left(\frac{D_{ON}}{3}\right)\left(I_{pk\_L_{xb}}{}^2 + I_{pk\_L_{xb}}\left(I_{OUT} - \frac{\Delta I_L}{2}\right) + \left(I_{OUT} - \frac{\Delta I_L}{2}\right)^2\right)} \quad (28)$$

$$V_{ripple\_Cx} = \frac{(1 - D_{ON}) I_{IN}}{f_{sw} C_1} + I_{IN} ESR_{Cx} \quad (29)$$

Since Q2 and Q3 are generally diodes, there are several things to consider when choosing a component. $V_{ds\ max}$ must be rated to at least $V_{IN} + V_{OUT}$. The continuous current should be at least 1/3 the peak current to be seen. Interestingly, because of the phase relationship between the output voltage ripple of the two supplies, the SEPIC diode actually receives the full switch for some amount of time before the current achieves a more even split. As expected though, the average current through both diodes is the same, I_{OUT}. In addition, the package must be able to handle the I_{OUT} in the thermal environment of the application.

$$I_{DC\_diode\_current\_rating} \geq \frac{2}{3}\left(I_{IN} + I_{OUT} + \Delta I_L\right) \quad (30)$$

OUTPUT FILTER

The SEPIC-Ćuk as a dual rail converter is typically used for analog power supplies, which often require very low output ripple. Low output ripple (down to 1 mV) is generally easily achieved on the Ćuk (negative) output rail simply by using ceramic output capacitors because the output current is continuous like the output current of a buck converter.

On the SEPIC (positive) rail, the output current is discontinuous like the input current of a buck converter. This results in a step change in the current into the output capacitors. These switching spikes are not well attenuated even by ceramic capacitors because of their inductance. Therefore, it is often necessary to put a small, damped output pi filter on the output of the SEPIC winding.

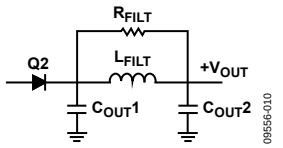

Figure 10. Schematic of the Output Filter

Although this filter affects the small-signal model in new and interesting ways, this issue is not fully discussed in this application note. As long as the damping resistor is chosen according to the Equation 31 and Equation 32, and the converter is designed to crossover at a tenth of ω_o or less, no instability should be caused by the pi filter.

C_{OUT1} should be chosen for around 2% output ripple and C_{OUT2} should be chosen to match the output capacitor of the Ćuk output using the equations in the power components stress section. A good value for L_{filt} is generally 1 µH, and Q_o should be set to 1.

$$\omega_o = \sqrt{\frac{2\left(C_{OUT1} + C_{OUT2}\right)}{\left(L_{filt} C_{OUT1}\ C_{OUT2}\right)}} \quad (31)$$

$$R_{filt} = \frac{\left(R_{load} L_{filt}\left(C_{OUT1} + C_{OUT2}\right) - \frac{L_{filt}}{Q_o \omega_o}\right)}{\frac{R_{load}\left(C_{OUT1} + C_{OUT2}\right)}{Q_o \omega_o} - L_{filt} C_{OUT1}} \quad (32)$$

ADP161X DESIGN TOOL

The ADP161x SEPIC-Ćuk design tool is a fully integrated Excel®-based designer for the ADP161x chips in a SEPIC-Ćuk configuration. Once the user has enabled macros (which may require a change of the security settings in Excel), the **Enter Inputs** dialog box appears, or can be found by pressing the **Find Solution** button. In the dialog box, enter the voltages and currents required for the design and choose whether to optimize for cost, loss, or size.

If the **View Solution** button is pressed, the design tool outputs a complete, optimized design. This includes a costed BOM with compensation values, an accurate, tested efficiency plot across load, a plot of power loss across load, a full load bode plot, performance parameters, component stresses, and power dissipation for every component. In addition, the **Build Your Design** tab provides the same BOM, but with the components arranged to fit on the blank demo board (ADP161x-BL3-EVZ) and any extra components required to configure the demo board .

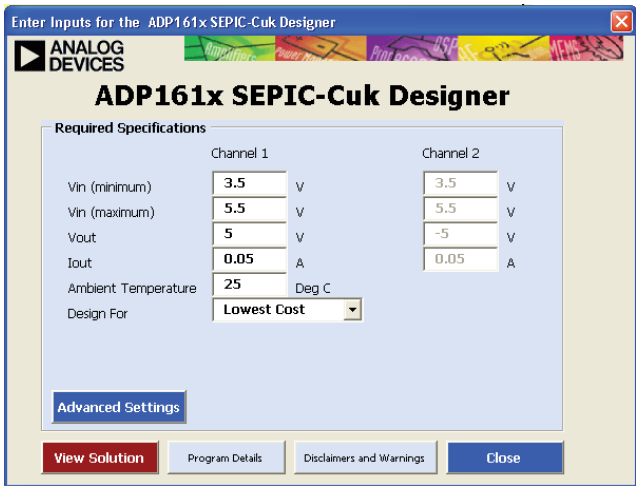

Figure 11. Basic Inputs Dialog Box

Additional customization tools are available in the **Advanced Settings** dialog box. Here the user can select parameter specifications for output voltage ripple, current, transient response, optional output filter usage, an external UVLO, and more. A more in-depth description of the functionality of these options is provided in the **Program Details** dialog box available by clicking the **Program Details** button found on the **Enter Inputs** dialog box.

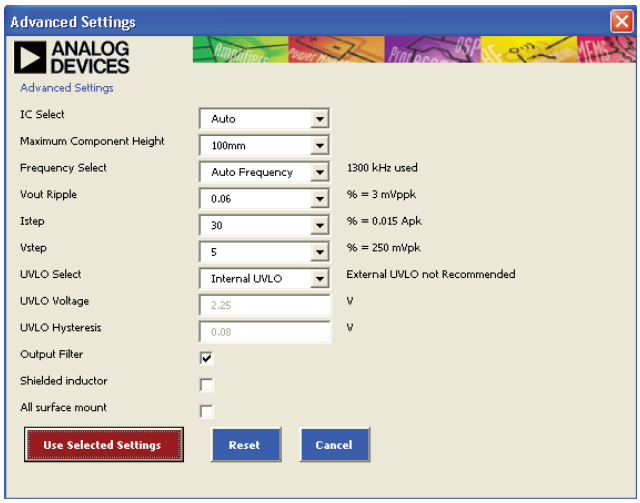

Figure 12. Advanced inputs Dialog Box

One of the most powerful features of this tool are the component buttons found on the **User Interface** tab. This functionality gives the user the ability to individually change each component to fully customize the design.

Each of the components in the drop-down list have been preselected from a database of thousands of components to produce a functional design, and sorted according to the optimization chosen in the **Enter Inputs** dialog box. The components must be selected in order, from top to bottom, since there are dependencies between the different components.

LAB RESULTS

To demonstrate the efficacy of the design tool, a design was done using the tool for 5 V_{IN}, ±5 V_{OUT} at 50 mA with the advanced specifications shown in Figure 11 and Figure 12. In addition, the diode was changed for slightly lower loss. The jagged efficiency line at around 10 mA is caused by the converter going into discontinuous mode. Once both the switches have turned off, the switch node rings causing zero voltage switching at specific load currents. A schematic for the circuit is shown in Figure 14.

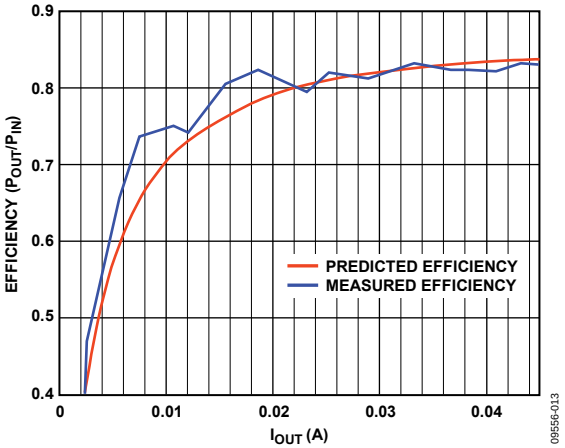

Figure 13. Efficiency Verification

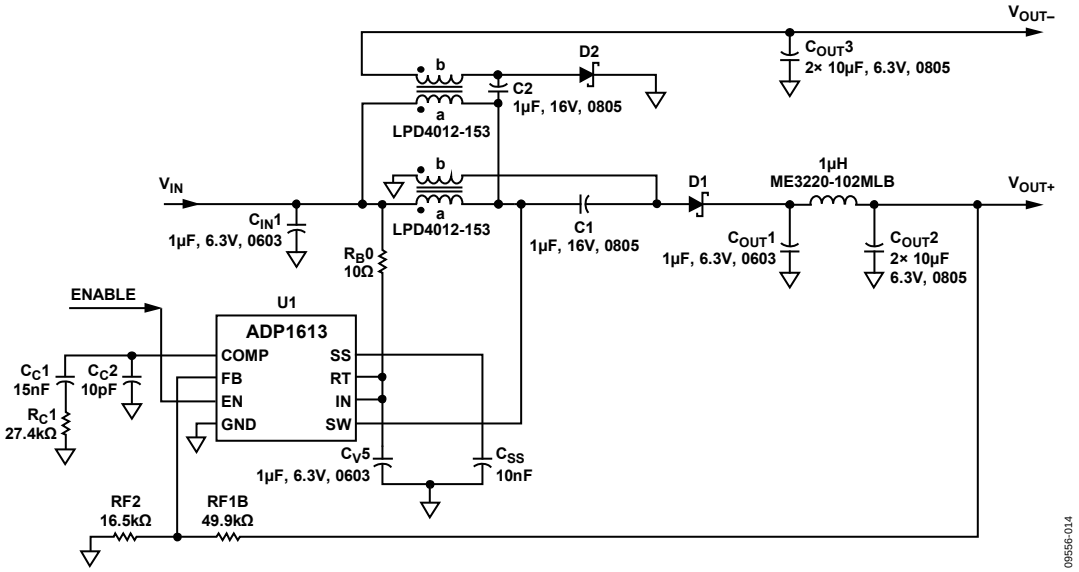

Figure 14. Schematic of Test Circuit

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CONCLUSION

In conclusion, the SEPIC-Ćuk provides an inexpensive and robust way to create dual rails using only one controller. The ADIsimPOWER™ design tool allows complete customization of the design and can be relied on to create robust SEPIC-Ćuk designs quickly.

NOTES

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