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ADXL346 Quick Start Guide
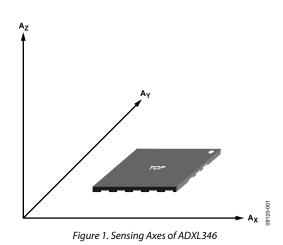## by Tomoaki Tusuzki and Harvey Weinberg

PHYSICAL MOUNTING

The ADXL346 is 3-axis accelerometer. The sensing axes are shown in Figure 1.

The ADXL346 senses positive acceleration when it is accelerated in the positive direction of the sensing axes. The user must be careful when sensing gravity because positive acceleration is sensed when the direction of the sensing axis is opposite to gravity. Figure 2 shows the output response to gravity.

The ADXL346 is supplied in a small, thin, 3 mm × 3 mm × 1 mm, 16-lead, plastic package. Refer to the ADXL346 data sheet for recommended printed circuit board land pattern.

Figure 1. Sensing Axes of ADXL346
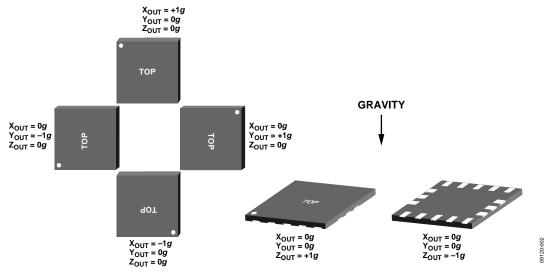

Figure 2. Output Response vs. Orientation to Gravity

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ELECTRICAL CONNECTION

ADXL346 communication is done via either I²C or SPI (3- or 4-wire). Figure 3 shows the recommended electrical connections for 4-wire SPI mode. Note that the SDO pin can be disconnected when using 3-wire SPI mode.
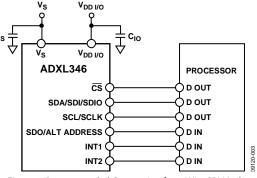
Figure 3. Recommended Connection for 4-Wire SPI Mode

Figure 4 shows the recommended electrical connection for I²C mode. The 7-bit I²C address for the device is 0x53, followed by the R/W̄ bit. The user can select alternate I²C address by connecting an SDO/ALT ADDRESS pin to the $V_{DD\,I/O}$ pin. The 7-bit I²C address for that configuration is 0x1D, followed by the R/W̄ bit.
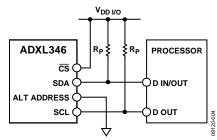
Figure 4. Recommended Connection for I²C Mode

Refer to the ADXL346 data sheet for details on power supply decoupling.

COMMUNICATION INTERFACE

Table 1 gives the list of typical configuration settings for the master processor requirements for SPI communication with the ADXL346. These settings are normally in control registers. Refer to the ADXL346 data sheet for timing specification and command sequence.

Table 1. SPI Settings

Processor Setting	Description
Master	ADXL346 operates as slave
SPI Mode	Clock polarity (CPOL) = 1
	Clock phase (CPHA) = 1
Bit Sequence	MSB first mode

For I²C communication, refer to the ADXL346 data sheet and *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007 for processor settings as well as timing specifications and command sequence.

Sometimes it is important to confirm the validity of communication before going to the next design stage. This can be done by reading the DEVID register (Address 0x00). It is a read only register that contains 0xE6. If the data read from DEVID is not 0xE6, it is the indication that either the physical connection or command sequence is incorrect.

INITIALIZATION

Figure 5 shows the minimum initialization sequence. The ADXL346 operates in a 100 Hz ODR with the DATA_READY interrupt on the INT1 pin during this start-up sequence. When setting other interrupts or using the FIFO, it is recommended that those registers used are set before the POWER_CTL and INT_ENABLE registers. Refer to the ADXL346 data sheet and AN-1025 Application Note for other operation modes of the ADXL346 and details about FIFO.

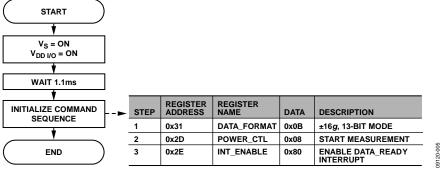| STEP	REGISTER ADDRESS	REGISTER NAME	DATA	DESCRIPTION
1	0x31	DATA_FORMAT	0x0B	±16*g*, 13-BIT MODE
2	0x2D	POWER_CTL	0x08	START MEASUREMENT
3	0x2E	INT_ENABLE	0x80	ENABLE DATA_READY INTERRUPT

Figure 5. Minimum Initialization Sequence

READING OUTPUT DATA

The DATA_READY interrupt signal indicates that 3-axis acceleration data is updated in the data registers. It is latched high when new data is ready. (The interrupt can be configured to be latched from low-to-high through the DATA_FORMAT register. Refer to the ADXL346 data sheet for details.) Use the low-to-high transition to trigger action on an interrupt service routine. Data is read from DATAX0, DATAX1, DATAY0, DATAY1, DATAZ0, and DATAZ1 registers. To ensure data coherency, it is recommended that multibyte reads are used to retrieve data from ADXL346. Figure 7 shows the read sequence example for 4-wire SPI.
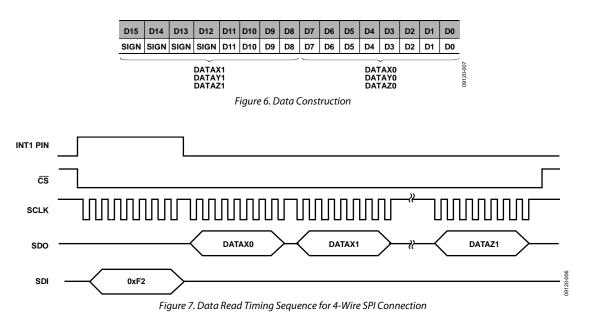
DATA FORMAT

The data format of the ADXL346 is 16 bits. Once acceleration data is acquired from data registers, the user must reconstruct the data. DATAX0 is the low byte register for X-axis acceleration and DATAX1 is the high byte register. In 13-bit mode, the upper 4 bits are sign bits (see Figure 6). Note that other data formats are available by setting the DATA_FORMAT register. See the ADXL346 data sheet for more details.

The ADXL346 uses twos complement data format. When in 13-bit mode, 1 LSB represents about 3.9 mg.

Table 2. ADXL346 Output Data Format

16-Bit Code (Hex)	Twos Complement Representation (Dec)	Acceleration (mg)
0FFF	4095	+1599
…	…	…
0002	+2	+7.8
0001	+1	+3.9
0000	0	0
FFFF	−1	−3.9
FFFE	−2	−7.8
…	…	…
F000	−4095	−1600

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SIGN	SIGN	SIGN	SIGN	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

DATAX1
DATAY1
DATAZ1

DATAX0
DATAY0
DATAZ0

Figure 6. Data Construction

Figure 7. Data Read Timing Sequence for 4-Wire SPI Connection

USING THE SELF-TEST FEATURE

The ADXL346 provides a self-test feature that enables an electromechanical test on the device without external mechanical stimulus. Figure 8 outlines a recommended self-test sequence. Note that the ADXL346 should be placed in a stable environment when conducting the self-test sequence.
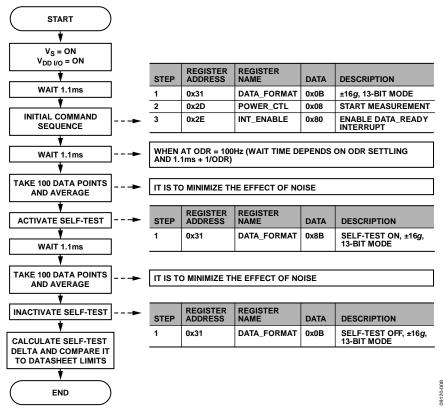

STEP	REGISTER ADDRESS	REGISTER NAME	DATA	DESCRIPTION
1	0x31	DATA_FORMAT	0x0B	±16*g*, 13-BIT MODE
2	0x2D	POWER_CTL	0x08	START MEASUREMENT
3	0x2E	INT_ENABLE	0x80	ENABLE DATA_READY INTERRUPT

WHEN AT ODR = 100Hz (WAIT TIME DEPENDS ON ODR SETTLING AND 1.1ms + 1/ODR)

IT IS TO MINIMIZE THE EFFECT OF NOISE

STEP	REGISTER ADDRESS	REGISTER NAME	DATA	DESCRIPTION
1	0x31	DATA_FORMAT	0x8B	SELF-TEST ON, ±16*g*, 13-BIT MODE

IT IS TO MINIMIZE THE EFFECT OF NOISE

STEP	REGISTER ADDRESS	REGISTER NAME	DATA	DESCRIPTION
1	0x31	DATA_FORMAT	0x0B	SELF-TEST OFF, ±16*g*, 13-BIT MODE

Figure 8. Self-Test Sequence

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USING OFFSET REGISTERS

The [ADXL346](#) has offset registers that facilitate offset calibration. The data format for the offset registers is 8-bit, twos compliment. The resolution of the offset registers about 15.6 mg/LSB. If the offset calibration must be finer than 15.6 mg/LSB, the calibration needs to be done at the processor. The offset register adds the value written in the register to measured acceleration. For example, if the offset is +156 mg, then −156 mg should be written to offset register. Figure 9 shows the typical offset calibration sequence.

For this routine, X-/Y-axes errors are zero when 0 g input is applied, whereas Z-axis errors are zero when 1 g input is applied. Greater accuracy can be achieved if it is possible to rotate the ADXL346 at calibration.

STEP	REGISTER ADDRESS	REGISTER NAME	DATA	DESCRIPTION
1	0x31	DATA_FORMAT	0x0B	±16g, 13-BIT MODE
2	0x2D	POWER_CTL	0x08	START MEASUREMENT
3	0x2E	INT_ENABLE	0x80	ENABLE DATA_READY INTERRUPT

WHEN AT ODR = 100Hz (WAIT TIME DEPENDS ON ODR SETTLING AND 1.1ms + 1/ODR)

IT IS TO MINIMIZE THE EFFECT OF NOISE

X_CALIB = −(OUTPUT (X) ÷ 4)
Y_CALIB = −(OUTPUT (Y) ÷ 4)
Z_CALIB = −((OUTPUT (Z) − 256) ÷ 4)

STEP	REGISTER ADDRESS	REGISTER NAME	DATA	DESCRIPTION
1	0x1E	OFSTX	X_CALIB	X_CALIB TO BE 8 BIT
2	0x1F	OFSTY	Y_CALIB	Y_CALIB TO BE 8 BIT
3	0x20	OFSTZ	Z_CALIB	Z_CALIB TO BE 8 BIT

Figure 9. Offset Calibration Sequence

NOTES

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