ANALOG DEVICES

AN-1069
APPLICATION NOTE

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Zero Latency for the AD7190, AD7192, AD7193, AD7194, and AD7195

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INTRODUCTION

The ADCs listed above are ultralow noise, 24-bit, sigma-delta (Σ-Δ) analog-to-digital converters with PGA. These products include a digital filter as an integral part of the converter. There are a number of ways to configure this filter, one which allows it to operate without the settling time latency commonly associated with Σ-Δ ADCs. This application note describes this behavior, and compares it to the more conventional filtering also available on these ADCs.

ZERO-LATENCY MODE

These ADCs include an option to place the filter into a zero-latency mode or single cycle settling mode. In this mode, the ADC output period is always equal to the filter settling time. Therefore, the ADC's output data rate is the same regardless of whether the converter is converting on a single channel or whether the input channel is periodically changed.

By simply setting bit SINGLE in the Mode register to 1, the ADC operates as a zero-latency ADC.

The ADCs discussed in this application note have two filter types: a sinc^3 filter and a sinc^4 filter (selectable using the SINC3 bit in the Mode register).

In zero-latency mode, the output data rate is equal to

$$f_{ADC} = f_{CLK}/(3072 \times FS[9:0])$$

for the sinc^3 filter and

$$f_{ADC} = f_{CLK}/(4096 \times FS[9:0])$$

for the sinc^4 filter

where:
f_{CLK} is the master clock (4.92 MHz nominal).
$FS[9:0]$ is the decimal equivalent of the code in Bits FS9 to FS0 of the Mode register.

This is the equation for the output data rate when chop is disabled. Note that chop is assumed to be disabled in this application note, unless otherwise stated.

In both cases, the settling time is equal to

$$t_{SETTLE} = 1/f_{ADC}$$

for the sinc^3 or sinc^4 filter.

Table 1 and Table 2 provide examples of output data rates and the corresponding FS values for the sinc^3 and sinc^4 filters.

Table 1. Examples of Output Data Rates and the Corresponding Settling Time (Sinc^4 Filter)

FS[9:0]	Output Data Rate (Hz)	Settling Time (ms)
480	2.5	400
96	12.5	80
80	15	66.6
12	100	10
5	240	4.17
1	1200	0.83

Table 2. Examples of Output Data Rates and the Corresponding Settling Time (Sinc^3 Filter)

FS[9:0]	Output Data Rate (Hz)	Settling Time (ms)
480	3.3	300
96	16.7	60
80	20	50
16	100	10
5	320	3.125

Channel Change

Figure 1 shows the response of the ADC to a channel change when zero-latency mode is enabled. From Figure 1, the conversion time when converting on Channel A and Channel B is the same. In addition, there is no additional delay when switching from Channel A to Channel B.

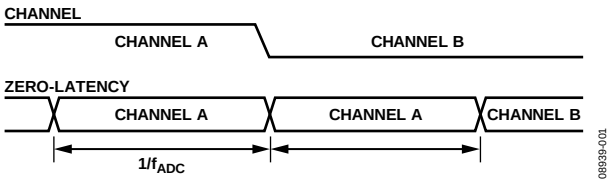

Figure 1. Channel Change (Zero-Latency Mode)

Analog Input Step Change on Selected Input

If a step change occurs in the analog input voltage, the ADC does not detect such a change and continues to output all conversions. It is possible that the next conversion will not fully reflect the change in the analog input as the complete settling must elapse after the step change (see Figure 2). In this case, it is the second conversion after the channel change that fully reflects the change in the analog input. Therefore, zero latency does not ensure that all conversions are completely settled.

The $\overline{\text{SYNC}}$ pin is useful to prevent these intermediate conversions, which contain samples from the old analog input and the new analog input. Taking $\overline{\text{SYNC}}$ low resets the filter and modulator. When $\overline{\text{SYNC}}$ is returned high, the modulator and filter begin sampling the new analog input. Therefore, the next conversion fully reflects the new analog input.

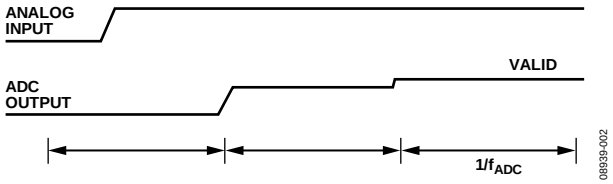

Figure 2. Asynchronous Analog Input Step Change (Zero Latency)

FILTER FREQUENCY RESPONSE

The filter notches are determined by the value in the FS[9:0] bits and the filter type selected (sinc^3 or sinc^4, chop enabled/disabled). For example, if FS[9:0] equals 96, chop is disabled and the sinc^4 filter is selected; the output data rate equals 12.5 Hz when zero latency is enabled. The output data rate equals 50 Hz when zero latency is disabled. In both cases, the filter response is the same—the first filter notch is at 50 Hz with subsequent notches at multiples of 50 Hz. Thus, enabling zero-latency mode changes the output data rate, but it does not change the filter response. Therefore, for a given frequency response, the output data rate is 3 (sinc^3 filter) or 4 (sinc^4 filter) times less when zero latency is enabled.

NOISE

The rms noise is determined by the value in the FS[9:0] bits and the filter type selected. When FS[9:0] equals 1023 and the sinc^4 filter is selected, the rms noise equals 8.5 nV for the AD7190. With zero latency enabled, the output data rate equals 1.17 Hz for the above conditions. With zero latency disabled, the output data rate equals 4.7 Hz. Therefore, for a given rms noise, the ADC has a lower output data rate when zero latency is enabled compared with zero latency disabled.

How does the rms noise compare when the output data rate is the same for both zero latency enabled and disabled? The rms noise is higher when zero latency is enabled. For example, when the output data rate is 50 Hz and the gain is set to 128, the AD190 has an rms noise of 28 nV (sinc^4 filter, chop disabled) when zero latency is disabled. This corresponds to 18.5 bits noise-free (peak-to-peak) resolution. With zero-latency mode enabled and the output data rate set to 50 Hz, the rms noise is typically 55 nV (gain = 128, sinc^4 filter, chop disabled). This corresponds to 17.5 bits noise-free resolution. Therefore, for the same output data rate, the rms noise is higher by a factor of 2 (approximately) when zero latency is enabled.

DEFAULT MODE

To compare the operation of the ADC with zero latency enabled and disabled, this section discusses the default mode of operation (zero latency disabled).

When zero latency is disabled and conversions are being performed on a single channel, the output data rate (f_{ADC}) is equal to

$$f_{ADC} = f_{CLK}/(1024 \times FS[9:0])$$

where:
f_{CLK} is the master clock (4.92 MHz nominal).
FS[9:0] is the decimal equivalent of the code in Bits FS9 to FS0 of the Mode register.

This is the equation for the output data rate when chop is disabled. Note that chop is assumed to be disabled in this application note, unless otherwise stated.

If the analog input is continuous, the digital filter generates a conversion that fully reflects the analog input every $1/f_{ADC}$ when converting on a single channel. The ADC uses analog input samples over a window of N conversions to generate a conversion (N being the order of the sinc filter). Table 3 and Table 4 provide examples of output data rates and the corresponding FS values for the sinc^3 and sinc^4 filters.

Table 3. Examples of Output Data Rates and the Corresponding Settling Time (Sinc^4 Filter)

FS[9:0]	Output Data Rate (Hz)	Settling Time (ms)
480	10	400
96	50	80
80	60	66.6
48	100	40
12	400	10
5	960	4.17
1	4800	0.83

Table 4. Examples of Output Data Rates and the Corresponding Settling Time (Sinc^3 Filter)

FS[9:0]	Output Data Rate (Hz)	Settling Time (ms)
480	10	300
96	50	60
80	60	50
48	100	30
16	300	10
5	960	3.125

If the analog input or the gain is changed, the filter cannot use the information from previous conversions to generate the present conversion. The digital filter needs to be flushed and loaded with information relevant to the new analog input. The time required to achieve this is equal to the settling time of the filter.

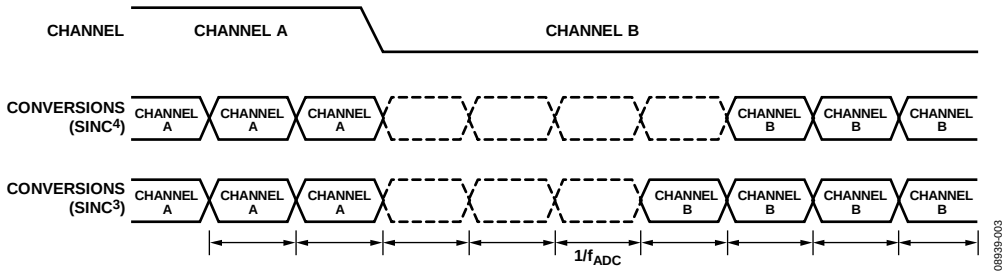

Figure 3. Channel Change (Free-Running Filter)

When the sinc^3 filter is selected, the settling time is equal to

$$t_{SETTLE} = 3/f_{ADC}$$

and when the sinc^4 filter is selected, the settling time is equal to

$$t_{SETTLE} = 4/f_{ADC}$$

Figure 3 shows the operation of the ADC for a channel change.

The ADC detects a channel change or a change in configuration (gain, output data rate, and so on). When such a change occurs, the ADC does not output the next conversion until the settling time has elapsed and a valid conversion is available. $\overline{\text{DRDY}}$ goes high during this period, returning low when the valid conversion is available. Therefore, the ADC only outputs conversions that fully reflect the analog input.

If the channel or configuration is not changed but the analog input voltage has a step change, this change is not detected by the ADC. Thus, it continues to output every conversion. In this case, there are some intermediate conversions, which do not fully reflect the analog input voltage. The settling time must elapse before a fully settled conversion is obtained. Figure 4 shows the operation of the ADC when a step change occurs in the analog input.

While the intermediate conversions do not fully reflect the new analog input voltage, they do provide some useful information. They indicate that a change has occurred in the analog input voltage. In some industrial applications, such as pressure systems, the system must quickly react to such changes. The intermediate conversions indicate that a change has occurred. This means that the system can react to this change after reading a few of the intermediate conversions—it does not need to wait until the completely settled conversion is available.

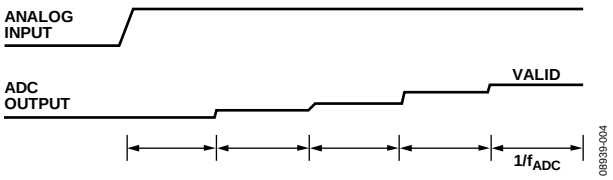

Figure 4. Step Change in the Analog Input Voltage (Sinc^4 Filter).

In Figure 4, the step change is synchronized with the conversion process so the time required to generate a fully settled conversion is ($4/f_{ADC}$) since the sinc^4 filter is selected. If the step change is asynchronous with the conversion process, the ADC requires one extra conversion cycle to generate a fully settled conversion (see Figure 5).

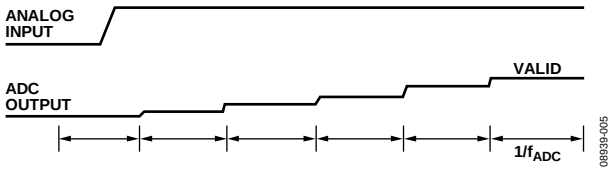

Figure 5. Asynchronous Step Change (Sinc^4 Filter)

CONCLUSION

Some system designers prefer zero-latency ADCs because the ADC result is fully settled at every conversion. This results in a constant output data rate for a single channel and a multichannel design—there is no extra latency when switching channels. The disadvantage of a zero-latency ADC is the low output data rate for a given filter frequency response. Therefore, if a system requires 50 Hz rejection, for example, the ADC needs to operate at rates less than 50 Hz. Similarly, the part operates at a lower output data rate for a given noise performance.

With zero latency disabled, the ADC can operate at a higher output data rate once the digital filter has settled. The disadvantage of this mode is the extra time required to generate the first conversion after a channel change. However, this mode allows higher output data rates for a given frequency response. With zero latency disabled, the ADC can operate at 50 Hz and still give rejection at 50 Hz. The ADC can also operate at higher output data rates for a given noise performance. With zero latency disabled, the part operates at the highest output data rate possible for a given noise performance or filter response when continuously converting on a single channel.

NOTES

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