AN-1036
APPLICATION NOTE

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Clear to Any Voltage Using the AD5370

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INTRODUCTION

Many DACs, including the AD5370, have a $\overline{\text{CLR}}$ pin that when asserted sets the output to a predefined voltage, usually 0 V. In some cases, the digital-to-analog converter (DAC) can also be set to clear to midscale. For multichannel DACs, the usual solution is to write to all channels with the required clear code. This can take more time than may be desirable. The AD5370 contains software shortcuts that can dramatically reduce the amount of writes required. The technique described in this application note can also be applied to the DACs listed in Table 1.

Table 1. Other DACs to Which Technique Can Be Applied

Part Number	Description
AD5360	16-channel, 16-bit voltage-output DAC
AD5361	16-channel, 14-bit voltage-output DAC
AD5362	8-channel, 16-bit voltage-output DAC
AD5363	8-channel, 14-bit voltage-output DAC
AD5371	40-channel, 14-bit voltage-output DAC
AD5372	32-channel, 16-bit voltage-output DAC
AD5373	32-channel, 14-bit voltage-output DAC

IMPLEMENTATION

Each channel of the AD5370 has two input registers, X1A and X1B. When either of these registers is written to, a calibration calculation is performed based on the contents of the M and C registers. The result is stored in the X2A or X2B register. In a typical application, only the X1A register is used. In this case, the X2A register (and therefore the X2B register) can be used to hold a clear code to which the outputs can be switched to, if necessary. Figure 1 shows how the registers are configured. MUX 1 (see Figure 1) determines whether a write to the data register goes to Register X1A or Register X1B, and the result of the calibration is stored in either Register X2A or Register X2B as appropriate. The MUX 1 multiplexer of each channel is controlled by a single bit in the control register.

The value that is loaded to the DAC register is determined by MUX 2 (see Figure 1). The MUX 2 for each channel can be independently controlled, allowing the X2A or X2B register to be selected as the source for the DAC register on a channel-by-channel basis. A single write operation can also be used to switch all channels between Register X2A and Register X2B, and vice versa. The 40 channels of the AD5370 are arranged as five groups of eight channels. The MUX 2 of each channel in a group is individually controlled by its own single bit in an 8-bit register.

Deglitching the Outputs

During normal operation, the AD5370 triggers a deglitch circuit whenever a DAC is written to. The deglitch circuit ensures a smooth transition between the old value and the new value for all DACs changing within a group. The deglitch circuit is not triggered when the MUX 2 values are changed; therefore, if glitch is a concern, at least one DAC in each group should be written to after the MUX 2 values have been changed. This triggers the deglitch circuit when $\overline{\text{LDAC}}$ is pulsed and the outputs are updated.

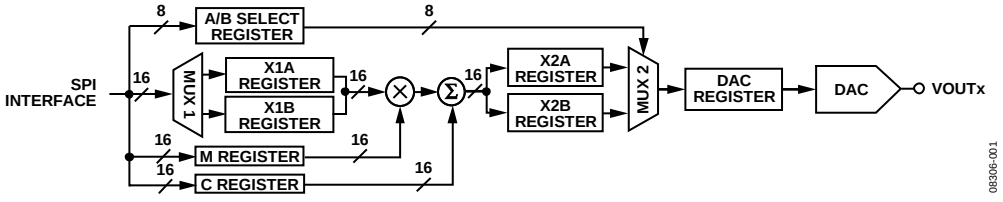

Figure 1. Functional Block Diagram of a Single Channel

EXAMPLE

This example assumes that outputs are to be cleared to 1 V; that the gain (M), offset trim (C), and offset DAC (OFSx) registers of the AD5370 are at their default values; and that a 3 V reference is being used. The flowchart in Figure 2 shows the procedure for initializing the AD5370, as well as the procedures for entering and exiting clear mode. Using this procedure, it is possible to set all 40 channels of the AD5370 to a predetermined value using far less than the 40 write operations that would normally be required.

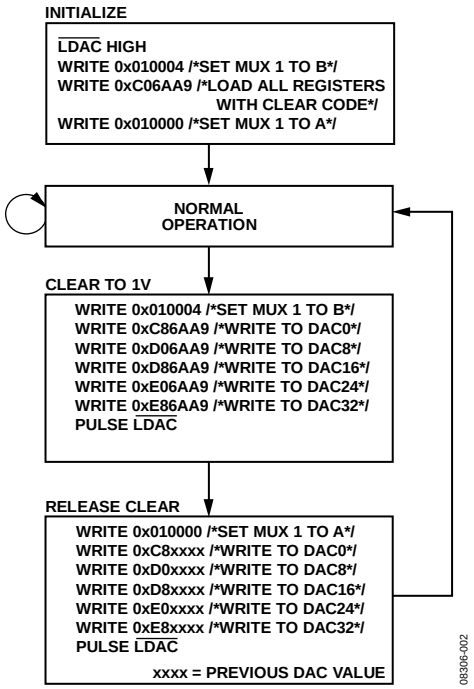

Figure 2. Clear Function Flowchart