ANALOG DEVICES

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APPLICATION NOTE

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Obtaining the Best Performance from the AD7893, 12-Bit Serial A/D Converter

by Albert O'Grady and Mike Byrne

INTRODUCTION

This application note discusses a proper printed circuit layout and contains application hints on how to obtain the best performance from the AD7893. Topics for discussion include the design and layout of a printed circuit board and the advantages and disadvantages of different timing and control sequences. The AD7893 is a fast 12-bit successive approximation A/D which operates from a single +5 V supply and incorporates an on-chip track-and-hold amplifier, on-chip clock and a high speed serial interface. All of these functions are housed in a small 8-pin mini-DIP or 8-pin SOIC. The serial interface allows the AD7893 to connect directly to digital signal processors (ADSP-2101, TMS320C25, etc.) and microcontrollers (8XC51, 68HC11, etc.). The performance of the AD7893, like that of any high resolution ADC, is influenced by surrounding circuitry, board layout and microprocessor interfacing.

The AD7893 uses a successive approximation technique in providing the analog-to-digital function. The conversion time for the A/D is 6 μs, requiring the internal voltage comparator to make a bit decision every 500 ns. In order to achieve 12-bit performance these decisions must be accurate to 1/2 LSB. This amounts to 305 μV for the 0 V to 2.5 V input range and 2.44 mV in the ±10 V analog input range part. To achieve this performance, the circuit designer must be conscious of noise both in the ADC itself and in the preceding analog circuitry. Other major causes for concern are ground loops and digital feedthrough from the interface bus. These are factors that influence any ADC design, and a proper printed circuit board layout that minimizes these effects is essential to achieve 12-bit performance.

PRINTED CIRCUIT BOARD LAYOUT HINTS

The board should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes which can be separated easily. A minimum etch technique is generally found to be the best for ground planes as this gives the best shielding.

Digital and analog grounds planes should be joined only in one place. If the AD7893 is the only device that requires AGND and DGND connection, then the ground planes should be connected at the AGND and DGND pins of the ADC. If the AD7893 is in a system where multiple devices require AGND to DGND connections, the connection should still be made at one point, a star ground point which should be established as close as possible to the AD7893.

Data and address buses on the board should be buffered or latched to isolate the high frequency bus of the processor from the bus of the high resolution converter. These act as a Faraday shield and will increase the signal-to-noise performance of the converters by reducing the amount of high frequency digital coupling.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7893 to avoid noise coupling.

The power supply lines to the AD7893 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals, like clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near analog inputs of devices. Avoid crossovers of digital and analog signals.

Traces for analog inputs should be kept as wide and as short as possible and should be shielded with analog ground where possible. When buffering analog inputs, the buffer should be kept as close to the analog input of the ADC as possible.

Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but not always possible with a double

sided board. In this technique, the component side of the board is dedicated to ground planes, and signals are placed on the solder side.

Good decoupling is vitally important when using high resolution ADCs. All analog supplies should be decoupled with 10 μF tantalum in parallel with 0.1 μF ceramic capacitors to analog ground. To achieve the best from the decoupling components, these must be placed as close to the device as possible—ideally right up against the IC socket. The main aim of a bypassing element is to maximize the charge stored in the bypass loop while simultaneously minimizing the inductance of this loop. Inductance in the loop acts as an impedance to high frequency transients and results in power supply spiking. By keeping the decoupling as close to the device as possible, the loop area is kept as small as possible, thus reducing the possibility of power supply spikes. V_{DD} and V_{SS} supplies of amplifiers should be decoupled again with 10 μF and 0.1 μF to AGND. All logic chips should be decoupled with 0.1 μF disc ceramic capacitors to digital ground.

EVALUATING AD7893 PERFORMANCE

Figure 1 shows the application circuit schematic for the AD7893 circuit board. The design and layout of this board uses the recommendations discussed in "Printed Circuit Board Layout Hints" on the previous page. The circuit schematic shown in Figure 1 differs from that used in the evaluation board (MC/BV-AD7893-EB) available from Analog Devices. The MC/BV-AD7893-EB layout contains some extra circuitry used to evaluate the AD7890, another 12-bit ADC in the AD789X series of ADCs. The same layout and grounding techniques are used on both circuit boards. The board designed from Figure 1 is used specifically for evaluating the AD7893, and the redundant circuitry required for the AD7890 has been omitted. Onboard components include an AD780, a pin programmable +2.5 V or 3 V ultrahigh precision bandgap reference, bus buffers for the serial data lines and an input buffer amplifier to buffer the analog input. Interfacing to this board is through a 9-way D-type connector. External sockets are provided for the conversion start input, analog input and an external reference input option. Figures 13, 14 and 15 at the back of this application note show the silkscreen, component and solder side artworks for the schematic shown in Figure 1. Refer to the section titled "Operating the AD7893 Circuit Board" for more information on setting up and operating this board.

TIMING AND CONTROL FOR OPTIMUM PERFORMANCE OF THE AD7893

Figure 2 shows the control sequence required to obtain optimum performance from the AD7893. In the sequence shown, conversion is initiated on the rising edge of $\overline{\text{CONVST}}$ and new data from this conversion is available in the output register of the AD7893 6 μs later. Once the read operation has taken place, a further 600 ns should be allowed before the next rising edge of $\overline{\text{CONVST}}$ to optimize

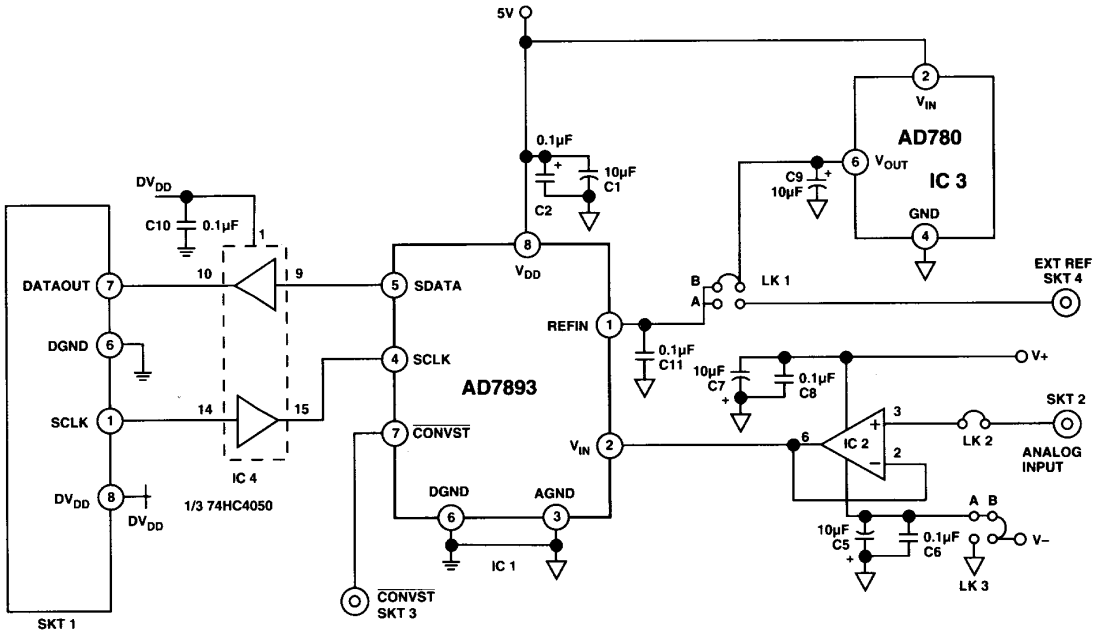

Figure 1. Evaluation Board Circuit Diagram

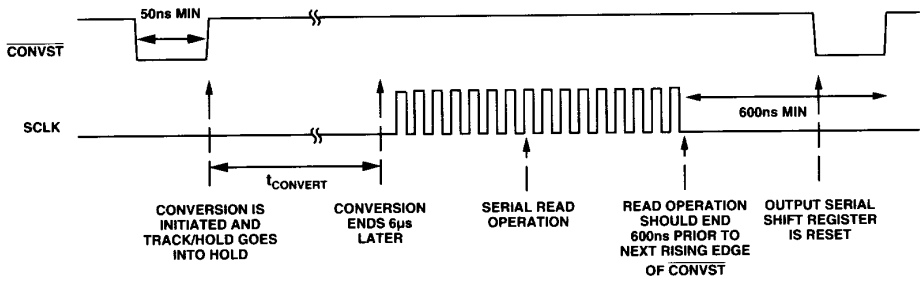

Figure 2. Optimum Control Sequence for the AD7893

the settling of the track/hold amplifier before the next conversion is initiated. Using the maximum serial clock frequency with this sequence gives a maximum throughput rate of 117 kHz. The serial interface to the AD7893 consists of just two wires, a serial clock input (SCLK) and the serial data output (SDATA). Due to the small pin count, there is no status signal provided to indicate end of conversion. Applications that want to achieve optimum performance from the AD7893 will have to ensure that the data read does not occur during conversion or 600 ns prior to the rising edge of $\overline{\text{CONVST}}$. One way to achieve this is to ensure in software that the read operation is not initiated until 6 μs after the rising edge of $\overline{\text{CONVST}}$. This will only be possible if the software knows when the $\overline{\text{CONVST}}$ command is issued.

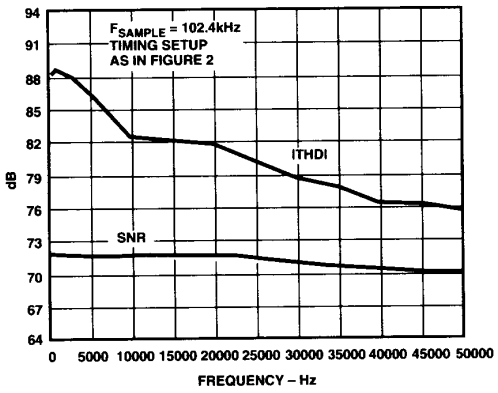

Figure 3. THD & SNR vs. Frequency @ 100 kHz Sampling

Figures 3, 4, 5 and 6 show the performance of the AD7893 when used in the AD7893 circuit board. The timing setup for the experiments is as in Figure 2. The sampling frequency used is 100 kHz and the serial clock frequency used is 8 MHz. Figure 3 shows a plot for THD and SNR versus frequency. These results show that for an input frequency of 10 kHz the SNR is typically 71.5 dB and the THD is –82.5 dB. Figure 4 shows a noise histogram for the same setup as above. The analog input was centered on code 2047 and 8000 conversions were taken from the AD7893. The results show that the code distribution is three counts. The rms noise calculated from this distribution is 0.198 LSBs. Figure 5 shows a typical FFT plot for an input frequency of 10 kHz while Figure 6 shows an FFT for a 50 kHz input. The plots show that the second and third harmonics have increased in amplitude when going from a 10 kHz input to a 50 kHz input. This contributes to the reduction in SNR and THD shown in Figure 3.

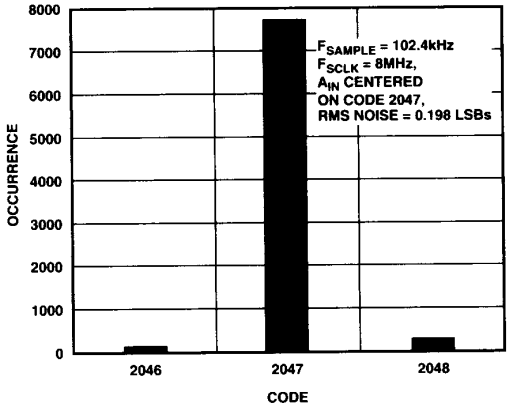

Figure 4. Noise Histogram @ 100 kHz Sampling

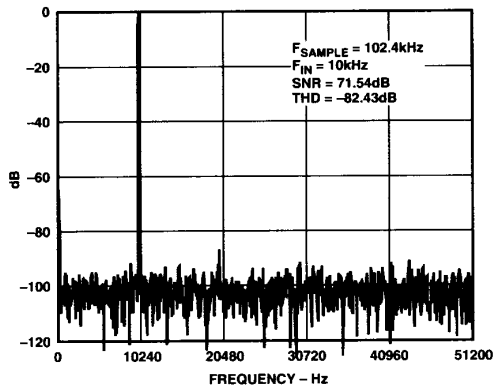

Figure 5. Typical FFT Plot for a 10 kHz Input

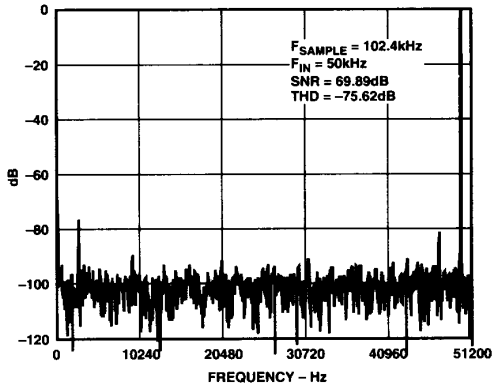

Figure 6. Typical FFT Plot for a 50 kHz Input

READING DURING CONVERSION

The throughput rate of the AD7893 can be increased by reading data during conversion. The track and hold returns to the track mode at the end of conversion and requires 1.5 µs to acquire an input signal to an accuracy level of 12 bits. The conversion time for the ADC is internally timed using a laser-trimmed clock oscillator and requires 6 µs to convert the signal. The minimum throughput time is 7.5 µs (6 µs + 1.5 µs) resulting in a maximum throughput rate of 133 kHz. Figure 7 shows the timing setup when operating the AD7893 in this arrangement. The output register of the AD7893 is normally updated at the end of conversion. However, if a serial read is in progress at this time, the update is deferred until this read is completed. If the read has not been completed before the next falling $\overline{\text{CONVST}}$ edge, the output register will be updated on this edge and the output shift register count reset. To ensure that the track and hold correctly acquires the input signal in applications where a serial read takes place during the conversion time of the ADC, a time of 1.5 µs should be allowed between the last serial clock falling edge and the rising edge of the $\overline{\text{CONVST}}$. When running the AD7893 at its maximum throughput rate, the signal-to-noise ratio will degrade and the code flicker from the part will also increase.

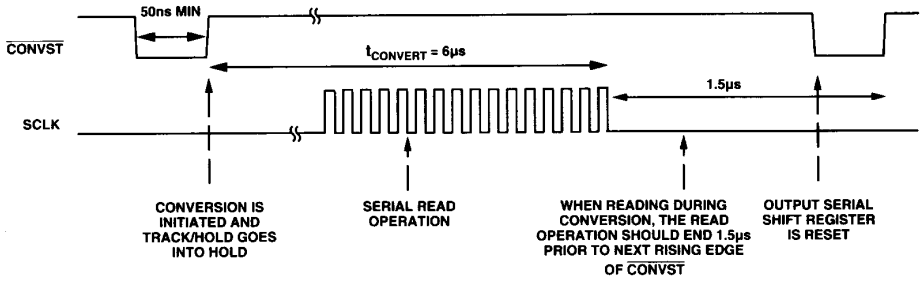

Figure 7. Timing Setup for 133 kHz Throughput

Figures 8, 9, 10 and 11 show the performance of the AD7893 using the circuit as in Figure 1 and using a sampling rate of 133 kHz. The layout used is shown in Figures 14 and 15. The timing setup for the experiments is as in Figure 7. Figure 8 shows a plot for THD and SNR versus frequency. These results show that for an input frequency of 10 kHz the SNR is typically 68.7 dB and the THD is –82.5 dB. The SNR is 3 dB worse in this case where the read occurs during conversion than in the previous case where the read did not occur during conversion. The THD numbers are similar to the optimum timing case (Figure 2), so the decrease in SNR is due to the increase in the noise floor caused by noise being coupled from the serial clock during conversion. Figure 9 shows a noise histogram for the same setup as above. The analog input was centered on code 2047 and 8000 conversions were taken from the AD7893. The results show that the code distribution is three counts. This is similar to that achieved in the previous case (Figure 4), but a larger number of conversions fall into the outer bins. This causes rms noise to increase; the value calculated from this distribution is 0.229 LSBs. This ties in with the results from the SNR versus frequency experiment. Figure 9 shows a typical FFT plot for an input frequency of 10 kHz while Figure 11 shows an FFT for a 65 kHz input. The plots show that the second and third harmonics have increased in amplitude when going from a 10 kHz input to a 65 kHz input. There is also some leakage into the bins around the fundamental frequency. These contribute to the reduction in SNR and THD shown in Figure 8.

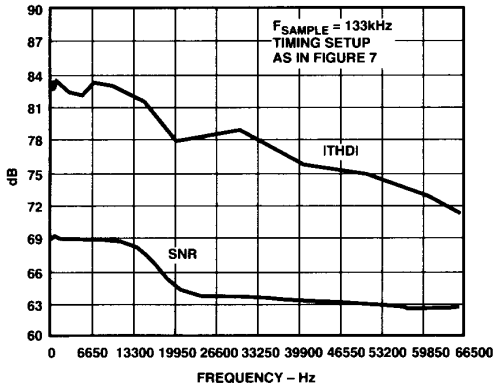

Figure 8. THD & SNR vs. Frequency @ 133 kHz Sampling

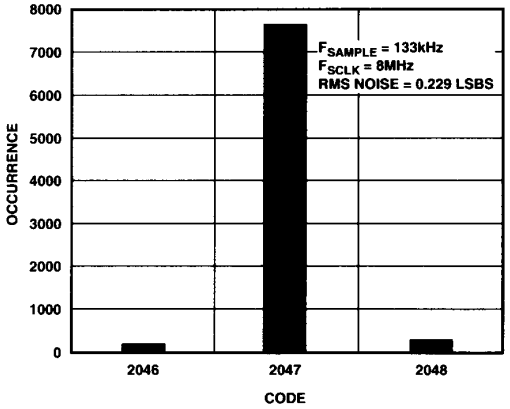

Figure 10. Noise Histogram @ 133 kHz Sampling

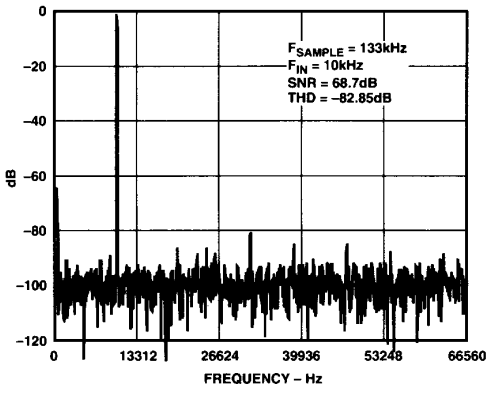

Figure 9. Typical FFT Plot for a 10 kHz Input

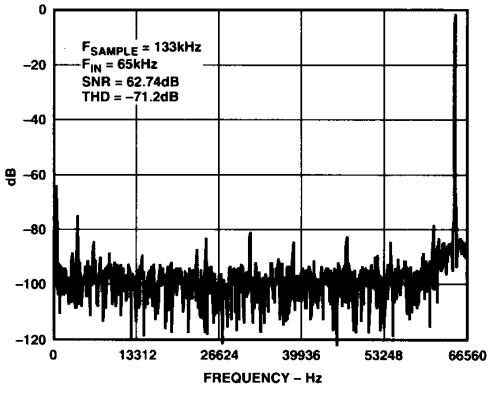

Figure 11. Typical FFT Plot for a 65 kHz Input

OPERATING THE AD7893 CIRCUIT BOARD.

POWER SUPPLIES:

This circuit board has four analog power supply inputs: +5 V, V+, AGND and V–. The +5 V input is used to drive the AD7893 V_{DD} and also supplies the input to the AD780 voltage reference. The V+ and V– are used to power the on-board buffer amplifier. This amplifier may be a single supply amplifier operated from +5 V and GND if the 0 V to 2.5 V version of the AD7893 is being used. An appropriate amplifier for this would be the AD820. When using a single supply amplifier, LK3 should be placed in position A, thus connecting the V_{SS} to AGND, and the V+ should be connected to the +5 V input. When using the ±10 V input range part, an AD711 or AD845 would be an appropriate buffer amplifier. In this case a +15 V supply should be connected to V+ and a –15 V supply connected to the V– input and LK3 placed in position B. There are two digital power supply inputs, DV_{DD} and DGND, which are used to power the digital logic on the board. These supplies can be provided through the D-type connector or through the connection pins labelled on the board.

All supplies are decoupled to ground with 10 µF tantalum and 0.1 µF ceramic disc capacitors. Analog supplies are decoupled to AGND while the digital supplies are decoupled to the DGND plane.

The circuit board uses extensive ground planing to minimize any high frequency noise interference from the on-board clocks or any other sources. Once again, the ground planing for the analog section is kept separate from that for the digital section, and they are joined only at the AD7893 AGND and DGND pins.

SHORTING PLUG OPTIONS

There are three shorting plug options that must be set before using the circuit board. These are outlined below:

LK1 This option is used to select the reference source for the AD7893 REFIN pin.

With this link in position A an external reference applied to SKT4 is routed to the AD7893 REFIN pin.

In position B the AD780 2.5 V reference is selected as the reference for the AD7893.

LK2 This link option is in series with the analoginput from the external socket SKT2. With this link in position the analog input signal applied to SKT2 is routed to the buffer amplifier IC2. If additional signal conditioning is required before the buffer, this link can be removed and the input signal tapped off to the additional circuitry which can be built on the grid area provided.

LK3 This option is used to select the V_{SS} supply for the buffer amplifier used on the evaluation board. When using a single supply amplifier, this link should be in position A; in this position the V_{SS} pin of the amplifier is connected to AGND. If a dual supply amplifier is used, this link should be in position B whereby the V_{SS} of the amplifier is routed from the V– pin.

EVALUATION BOARD INTERFACING

Interfacing to the evaluation board is via a 9-way D-Type connector, SKT1. The pinout for this connector is shown in Figure 12, and its pin designations are given in Table I.

SKT1 PIN DESCRIPTION

SCLK — Serial Clock Input. An external serial clock is applied through this input to obtain serial data from the part. This serial clock is buffered using a 74HC4050 buffer on the evaluation board.

DGND — Digital Ground. This line is connected to the digital ground plane on the evaluation board. It allows the user to provide the digital supply via the connector along with the other digital signals.

DATAOUT — Serial Data Output. Serial data from the part is obtained at this output. This data is buffered by 74HC4050 hex buffer before arriving at the DATAOUT pin of the connector. The serial data is clocked out by the rising edge of SCLK and is valid on the falling edge of SCLK.

DV_{DD} — Digital +5 V Supply. This line is connected to the DV_{DD} supply line on the evaluation board. It allows the user to provide the digital supply via the connector along with the other digital signals.

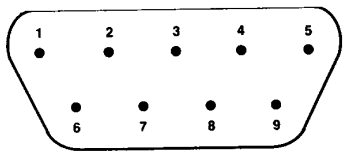

Figure 12. Pin Configuration for SKT1, D-Type Connector

Table I. SKT1 Pin Functions

Pin No.	Mnemonic
1	SCLK
2	N/C
3	N/C
4	N/C
5	N/C
6	DGND
7	DATAOUT
8	DV_{DD}
9	N/C

SOCKETS

There are four sockets relevant to the operation of the AD7893 on this circuit board. The function of these sockets is outlined in Table II.

Table II. Socket Functions

Socket	Function
SKT1	9-Way D-Type Connector
SKT2	Subminiature BNC Sockets for Analog Input
SKT3	Subminiature BNC Socket for $\overline{\text{CONVST}}$ Input
SKT4	Subminiature BNC Socket for External Reference

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as per the required operating mode. Figure 13 shows the silkscreen layout of the board in order to ease setup. When using the AD7893-2 (0 V–2.5 V input range) with a single supply buffer amplifier, the links should be set up as follows: LK 1 should be in position B, LK 2 should be in place and LK 3 should be in position A. With the AD7893-10 (±10 V i/p range) using a buffer amplifier, the following are the recommended link positions: LK1 should be in position B, LK2 should be put in place and LK3 should be in position B.

COMPONENT LIST

Integrated Circuits

IC1	AD7893
IC2	Buffer Amplifier
IC3	AD780 Voltage Reference
IC4	74HC4050 Hex Buffer

Capacitors

C2, C4, C6, C8, C10	0.1 µF Disc Ceramic Capacitors
C1, C3, C5, C7, C9	10 µF Tantalum Capacitors

Links

LK1, LK2, LK3	Shorting Plugs

Sockets

SKT1	9-Way D Type Connector
SKT2 to SKT4	Subminiature BNC Sockets

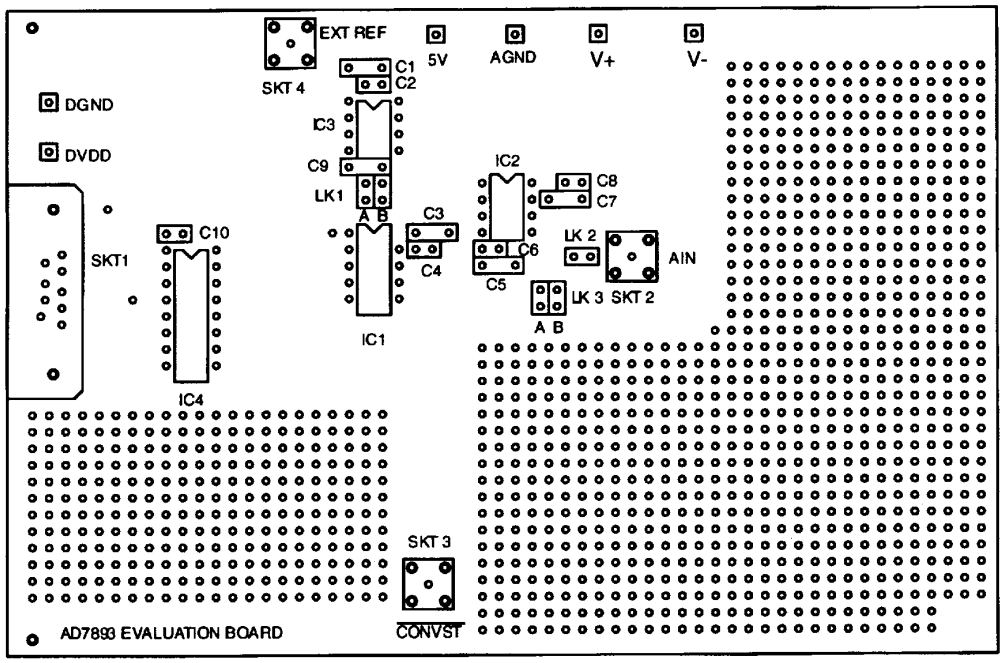

Figure 13. Silkscreen Layout for Circuit Board

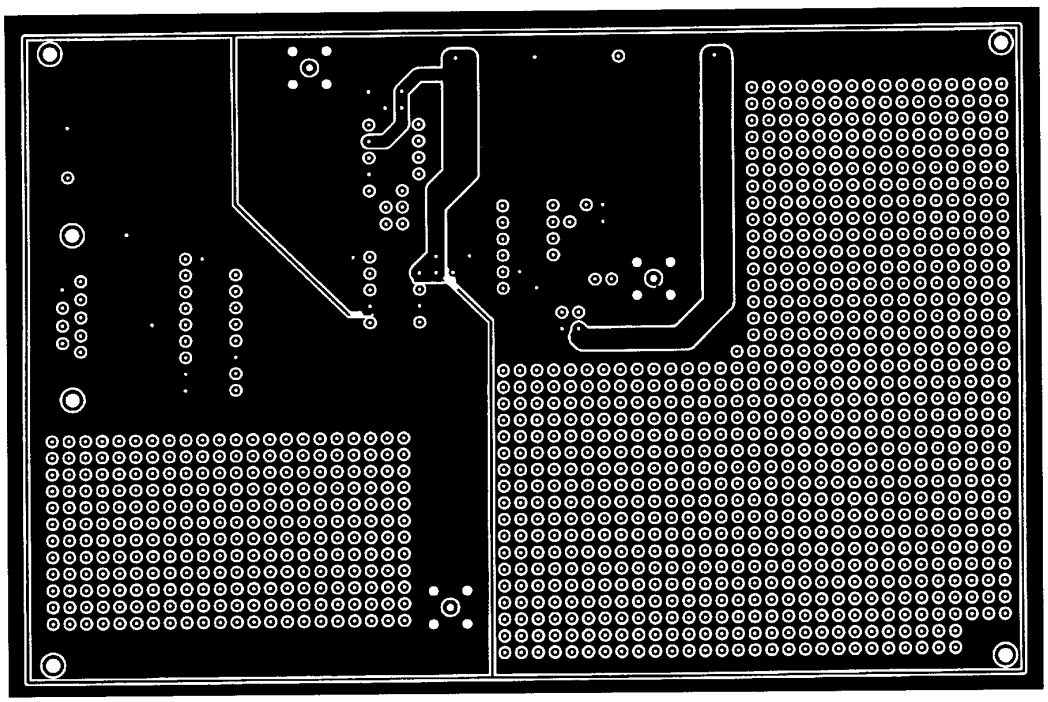

Figure 14. Component Side Layout for the AD7893 Board

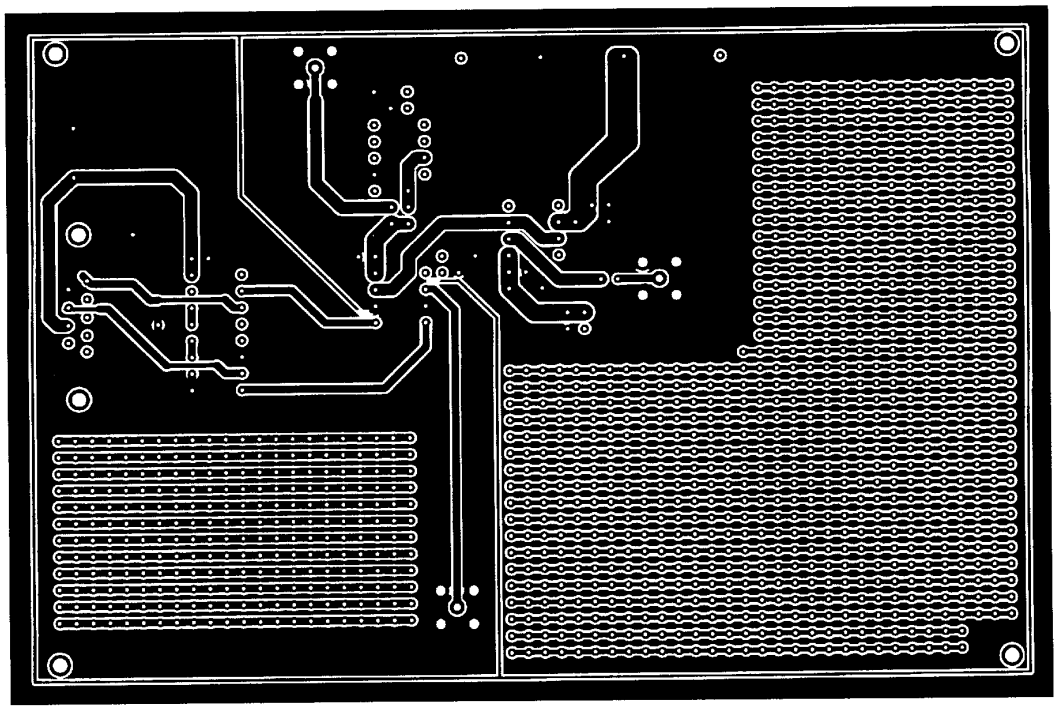

Figure 15. Solder Side Layout for the AD7893 Board

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