ANALOG DEVICES

AN-208
APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

Understanding LOGDACs

INTRODUCTION TO THE ANTILOG D/A CONVERTER

Analog Devices' AD7100 Series LOGDACs are CMOS multiplying DACs characterized by an exponential (antilogarithmic) digital-to-analog transfer function.

Perhaps the easiest way to visualize what a LOGDAC does is to compare it to two well-known circuits—the classic 3-terminal potentiometer and a CMOS multiplying DAC (digitally controlled potentiometer). As shown in Figure 1a through Figure 1c, the transfer function of all three circuits is of the form:

$$V_{OUT} = \alpha V_{IN} \qquad \text{EQN1}$$

WHERE:
α = attenuation factor
$0 \leq \alpha \leq 1$

In each case shown in Figure 1, α is a dimensionless number which can range from 0 (maximum attenuation) to approximately 1 (minimum attenuation). Additionally, each circuit has an analog input (V_{IN}), an analog output (V_{OUT}) and a mechanism for controlling the attenuation factor α.

The above in conjunction with Figure 1a through Figure 1c illustrates the similarity of the pot, M-DAC and LOGDAC functions. How, then does the LOGDAC *DIFFER* from the linear M-DAC?

The answer is resolution. The basic differentiating feature of the LOGDAC versus the linear multiplying DAC is the way resolution is specified.

RESOLUTION OF LOGDACs VERSUS LINEAR DACs

From Figure 1b, the attenuation factor α of a linear DAC is:

$$\alpha = \left(\frac{N}{2^n}\right) \qquad \text{EQN2}$$

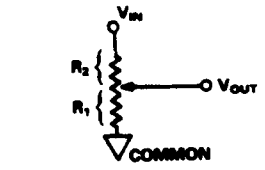
WHERE:
n = Number of digital input bits to the DAC
N = Integer value of DACs digital input

NOTE: Many treatments of multiplying DACs label the attenuation factor "D" where the digital input "D" is:

$$D = \alpha = \left(\frac{N}{2^n}\right) = \frac{\text{Bit 1}}{2^1} + \frac{\text{Bit 2}}{2^2} + \ldots \frac{\text{Bit n}}{2^n}$$

WHERE: Bit 1 through Bit n = 1 or 0
n = Number of bits

Since N was postulated to be an integer, the smallest possible change of N is plus or minus one count. The resolution of α is, therefore, ± 1 part in 2^n or 1 part in full scale. Important to realize is that the voltage resolution of a linear DAC is the same (barring differential nonlinearity effects) at all points on its transfer function.



$V_{OUT} = \left(\frac{R_1}{R_1 + R_2}\right)(V_{IN})$

FORM: $V_{OUT} = \alpha V_{IN}$

WHERE: α = ATTENUATION FACTOR = $\left(\frac{R_1}{R_1 + R_2}\right)$

Figure 1a. Three Terminal Pot

The resolution of a LOGDAC is different, however. The following discussion shall endeavor to show that a LOGDAC's voltage resolution is different at all points on its transfer function, i.e., barring differential nonlinearity effects, the resolution expressed as a *percent of reading* (not percent of full scale) is constant throughout the LOGDACs range.

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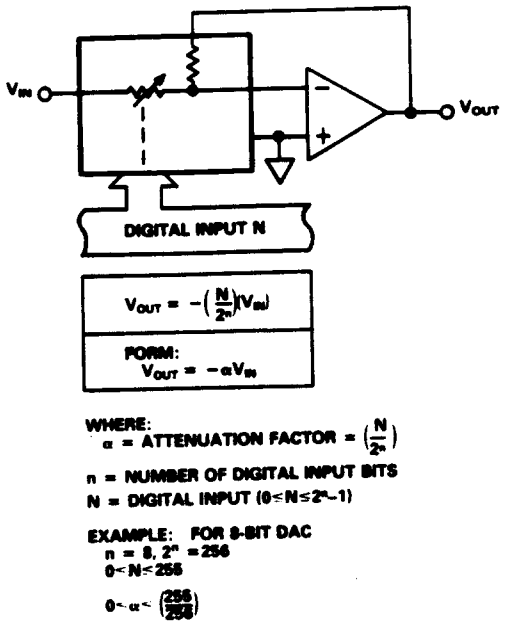

Figure 1b. Linear Multiplying DAC (Digitally Controlled Pot)

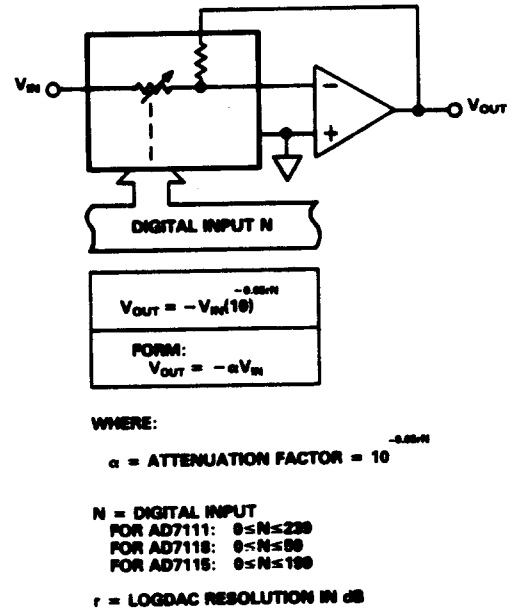

Figure 1c. LOGDAC (Digitally Controlled Pot)

From Figure 1c, the LOGDACs attenuation factor α is an exponential function (antilog) of the basic form:

$$y = a^{-x} \qquad \text{EQN3}$$

If base number 10 is chosen (other base numbers can be used, incidentally), the attenuation factor α for the LOGDAC of Figure 1c becomes:

$$\alpha = 10^{-\left(\frac{rN}{20}\right)} \qquad \text{EQN4}$$

WHERE:

N = Integer value of DACs digital input
- for AD7115: $0 \le N \le 199$
- for AD7111: $0 \le N \le 239$
- for AD7118: $0 \le N \le 59$

r = LOGDAC resolution in dB
- for AD7115: r = 0.1
- for AD7111: r = 0.375
- for AD7118: r = 1.5

Taking the LOG of both sides of EQN4 gives:

$$\text{LOG}_{10}\alpha = -\left(\frac{rN}{20}\right)$$

$$20\text{LOG}_{10}\alpha = -rN$$

$$\therefore \boxed{\alpha_{dB} = -rN} \qquad \text{EQN5}$$

From EQN5, it is readily apparent that a plus one count change of N causes an attendant −(r)dB change in the attenuation factor α (and thus also a −(r)dB change in the DAC's output voltage).

Figure 2 is a graph of the general LOGDAC transfer function for the circuit of Figure 1c. It shows quite simply that increasing the digital input N causes a decrease in the output voltage V_{OUT}. Additionally, it shows the nonlinear relationship of V_{OUT} relative to N. Figure 3 is an expanded section of the transfer function shown in Figure 2. It illustrates the fact that the ratio of any two adjacent LOGDAC output voltage levels is the same throughout the transfer function. To further amplify the significance of this point, consider that a + one count change in the digital input N causes the output voltage to decrease in amplitude by a *fixed ratio relative to where it was before the change.* (At all points on its transfer function . . .) Thus, we have a DAC with *percent of reading* resolution as opposed to the linear DAC which defines resolution in terms of *percent of full scale.*

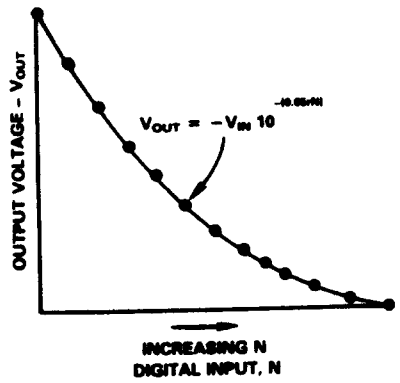

Figure 2. LOGDAC D/A Transfer Characteristic

To summarize, a linear DAC's voltage resolution is fixed throughout its transfer function. However, the LOGDAC

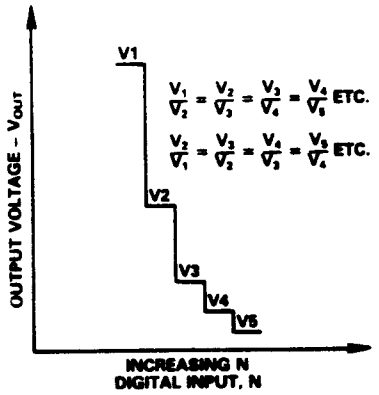

Figure 3. Expanded LOGDAC Transfer Function Illustrating the Concept of % of Reading Resolution

exhibits a continuously variable output voltage resolution throughout its transfer function range. The LOGDAC's voltage resolution is coarsest at or near full scale (0dB) and finest at or near 0 scale (mute). Table I shows the equivalent percent of reading resolution for various Analog Devices LOGDACs.

Model	dB Resolution ($\Delta N = \pm 1$ Count)	% of Reading Resolution ($\Delta N = +1$ Count)	($\Delta N = -1$ Count)
AD7118	±1.5dB	−15.9%	+18.9%
AD7111	±0.375dB	−4.2%	+4.4%
AD7115	±0.1dB	−1.1%	+1.2%

Table I.

BASIC CIRCUIT CONFIGURATIONS

ANTILOG DAC (Exponential with Negative Exponent)

The circuit of Figure 4 generates output voltage levels as determined by the equations:

$$V_{OUT} = -V_{IN}10^{-\left(\frac{rN}{20}\right)} \quad \text{EQN6}$$

and/or

$$V_{OUT} = -V_{IN}e^{-(0.11512rN)} \quad \text{EQN7}$$

WHERE:

r = LOGDAC resolution in dB
- for AD7118: r = 1.5
- for AD7111: r = 0.375
- for AD7115: r = 0.1

N = Integer equivalent of digital input
- for AD7118: 0≤N≤59
- for AD7111: 0≤N≤239
- for AD7115: 0≤N≤199

V_{IN} = ac or dc input voltage (nominal range ± 10V)

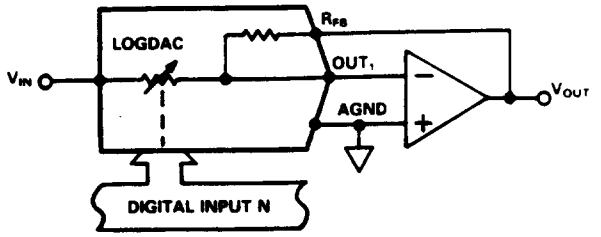

Figure 4. ANTILOG D/A Converter (Negative Exponent)

Features of the circuit of Figure 4 include:

1. It provides dB attenuation of V_{OUT} relative to V_{IN} as determined by the digital word N. (i.e., output range is 0dB to −dB)
2. The circuit provides % of *reading* resolution.
3. The analog input can be voltage or current, ac or dc, positive or negative polarity – i.e., the circuit is basically a CMOS multiplying DAC.

ANTILOG DAC (Exponential with Positive Exponent)

The circuit of Figure 5 is analogous to a multiplying DAC divider circuit. It provides signal gain of V_{OUT} relative to V_{IN} as determined by the equations:

$$V_{OUT} = -V_{IN}10^{+\left(\frac{rN}{20}\right)} \quad \text{EQN8}$$

and/or

$$V_{OUT} = -V_{IN}e^{+(0.11512rN)} \quad \text{EQN9}$$

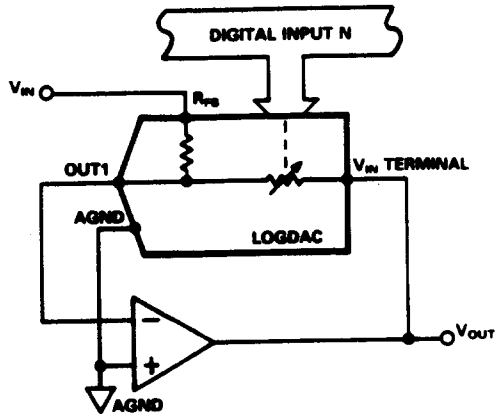

Figure 5. ANTILOG D/A Converter (Positive Exponent)

Basically, the analog input or reference voltage is applied to the on chip feedback resistor (RFB) and the amplifier output is connected to the V_{IN} terminal of the LOGDAC. The LOGDAC then ends up in the amplifier's feedback loop, thus the circuit provides *dB* gain of V_{OUT} relative to V_{IN} as determined by the digital input N (i.e., V_{OUT} range is 0dB to positive dB). As does the negative exponential DAC of Figure 4, this circuit provides % of *reading* resolution.

LOG OR LOG RATIO ADC

The circuit of Figure 6 provides an ADC function while performing a LOG compression. Its transfer function is:

$$N = \left(\frac{1}{-r}\right)\left(20\text{LOG}_{10}\left|\frac{-V_{IN}}{V_{REF}}\right|\right) \qquad \text{EQN10}$$

OR

$$N = \left(\frac{8.68659}{-r}\right)\left(\ln\left|\frac{-V_{IN}}{V_{REF}}\right|\right) \qquad \text{EQN11}$$

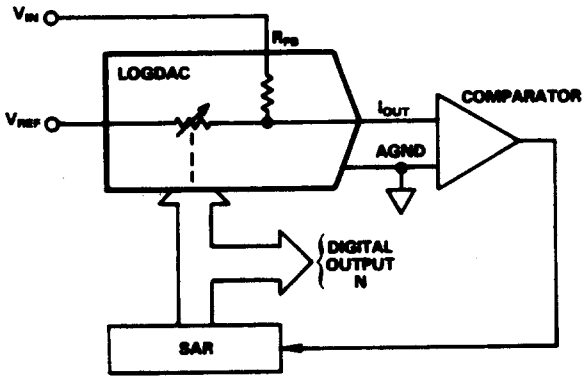

Figure 6. Log or Log Ratio A/D Converter

If the digital answer N (of EQN10) is multiplied by $-r$, the numerical value obtained is the dB value of the absolute value of V_{IN} relative to V_{REF} (answer 0dB to $-$dB).

If the digital answer N (of EQN11) is multiplied by $-r$ 8.68659, the numerical value obtained is the natural log of the absolute value of V_{IN} relative to V_{REF}.

Circuit Constraints:

1. V_{IN} and V_{REF} must be of opposite polarity
2. $V_{IN} \leq V_{REF}$