

Bootstrapped IC Substrate Lowers Distortion in JFET Op Amps

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INTRODUCTION

Among the more popular IC op amps used today are standard process junction isolated FET types (JFETs). These amplifiers typically use a pair of differential P-channel FETs at the input, with remaining stages of bipolar NPN/PNP transistors. Specs typical for the better of these devices are largely good to excellent. For example, the input currents are only a few pA at room temperature, the common-mode rejection is quite good (albeit below that of the best all-bipolar op amps), and they can have excellent dynamics. On the whole, these attributes make for low overall dc errors and generally good ac performance. In terms of total harmonic distortion (THD) performance, it can be as low as 0.001% (10 ppm) over the audio range for some applications.

THE PROBLEM OF NONLINEAR INPUT CAPACITANCE

However, there is one factor which can cause rapid deterioration of JFET op amp THD performance, when operated from high source impedances. This is a phenomenon of distortion increase with increasing input signal rate-of-change, due to nonlinearity of the capacitance seen at the two inputs. Since junction isolated ICs use isolation "pockets" or "wells" to host the subject differential pair of P-channel FETs, there will necessarily exist parasitic capacitance from the three FET terminals to the IC substrate. Logically, the most troublesome of the three terminals is the gate, due to the high source impedances which can potentially be seen externally. A typical input capacitance at the inputs of a JFET IC is 3 pF–5 pF, and is seen from Pins 2 and 3 to the substrate (normally Pin 4).

This parasitic substrate capacitance has a nonlinear behavior as a function of applied CM voltage. Like the C/V characteristics of discrete FETs and bipolar transistors, the capacitance is minimum at higher bias voltages. Thus in an op amp application with a given CM input level, this suggests operating at the highest practical supply voltage within rating to minimize the effect. The

input capacitance varies on an instantaneous basis with the applied ac CM voltage, and with a high impedance source, can generate high levels of distortion.

For JFET amplifier stages which operate as high source impedance followers, the CM input signal variation can give rise to excessive THD. Here, "high impedance" is qualified as 50k or greater, an approximate threshold where this distortion begins to be easily detectable at audio frequencies. For source impedances of 0.1 M Ω to 1 M Ω , the distortion can be as high as several tenths of a percent in the audio band.

The distortion is most easily seen as a 6 dB/octave rise in second harmonic distortion using a fixed level frequency sweep. The exact magnitude will vary with the device in use, and the specific combination of operating level, loading, supply voltages, and relative source impedance(s).

The designer has control over many of these circuit issues, and to some extent they can be optimized. One beneficial step which can lower frequency dependent distortion products is the use of *input impedance compensation*, a technique which ideally balances the source R/C components at the two amplifier inputs.¹ When used, this compensation serves to minimize the nonlinear effects of FET input amplifier common-mode capacitance.

To implement it, an optional feedback resistance " R_{S2} " is used in the circuit, where R_{S2} is simply made equal to the net nominal source impedance, " R_{S1} ". In the Figure 1 example circuit, R_{S1} is a fixed 500k resistor inserted for testing purposes. . . . in a real application, R_{S1} could in fact be an inseparable part of the source. If the source is also capacitive, a compensatory feedback capacitance can be used in addition to R_{S2} . This technique can be effective in terms of lowering distortion due to nonlinear input capacitance.

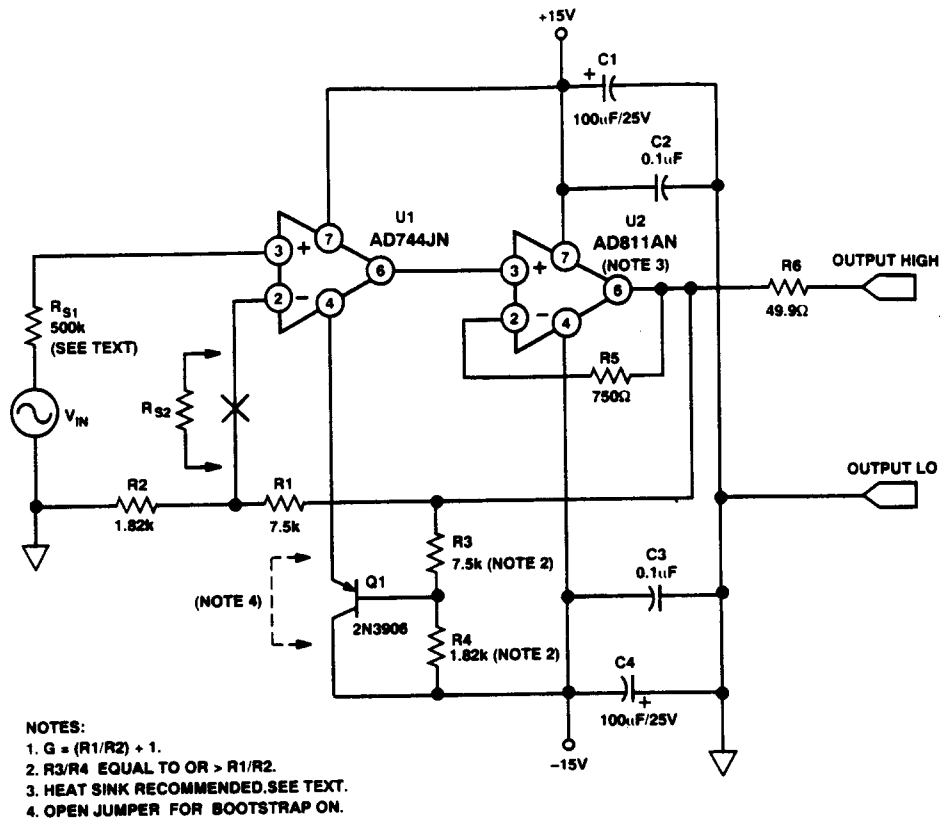


Figure 1.

MINIMIZING NONLINEAR INPUT CAPACITANCE EFFECTS

Unfortunately, there are still situations where it is desirable to operate a noninverting amplifier with unbalanced feedback/source impedances, but yet maintain minimal signal degradation in terms of noise/distortion. For example, the source impedance may simply be unknown. If it is higher than a few hundred k Ω , a JFET IC op amp is desirable from a noise standpoint, because of the low current noise. But, at the same time, it is undesirable from a distortion point of view due to the input C/V nonlinearity.

Figure 1 shows how a high performance JFET input op amp can be used in a circuit that reduces the nonlinear effects of CM input capacitance by bootstrapping the amplifier substrate. In this circuit stage U1 is an AD744, a low distortion JFET input op amp,² which determines the circuit's basic input characteristics. As will be shown, the AD744 is not unlike other JFET devices, and distorts with unbalanced high Z inputs due to nonlinear input C/V. When bootstrapped most effectively, however, the distortion due to input C/V nonlinearity can be reduced below the residual noise level.

With U1 loaded as shown by only the high impedance input (+) of buffer amp U2, it has virtually zero current drive requirements. This factor helps to maximize overall load dependent linearity, as well as to aid the bootstrapping action. Stage U2 provides primarily a high current output, which in this application is an AD811AN,³ a high performance transimpedance amplifier used here as a voltage follower buffer. Designed primarily for video use, the AD811's relevant specs are a slew rate of 2500 V/ μ s, a bandwidth of 120 MHz, and 100 mA of output current. These factors enhance this circuit by providing both high and linear load drive capability, for loads of 600 Ω and below.

Because the buffer amplifier U2 eliminates the output stage current variations in U1, the bootstrap transistor Q1 can more effectively deliver bootstrap correction voltage to Pin 4 of U1. U1 is operated in a near ideal fashion with regard to loading, a factor which enhances linearity.

DESIGN FACTORS

The design as shown in Figure 1 operates at an overall voltage gain "G" set by R1 and R2 just as in a conventional noninverting amplifier, or:

$$G = \frac{R1}{R2} + 1 \quad (1)$$

As is noted from the figure, there is also a separate resistor divider from the output of U2 to the V-rail, R3/R4. This divider feeds back a portion of the buffered U1 output signal from U2 to the negative supply pin of U1, Pin 4. With the two feedback dividers R1/R2 and R3/R4 matched in ratio, this has the net effect of driving the U1 substrate with a signal equal to that at the (+) input. As a result of reducing the voltage across the input capacitance, it is then effectively reduced. Note that for overall stability, the feedback via R3-R4 must be less than that of R1-R2. This will be so if this inequality is satisfied:

$$\frac{R3}{R4} \geq \frac{R1}{R2} \quad (2)$$

It should be noted that this bootstrap technique is most effective at gains of 5 or more, because the R3/R4 divider tends to reduce the U1 supply voltage, and thus limits dynamic range. In the design process the standard gain expression is used for G, then R3/R4 are selected to satisfy Equation 2. Here, with G equal to 5.12, R3/R4 are simply selected for a ratio similar to this.

PERFORMANCE

With these design and device selection factors, the bootstrapped composite amplifier performance is remarkable considering its modest complexity. The following tests operated the Figure 1 circuit at ± 15 V supplies and a 500 k Ω source for R_{S1}, and no compensation was used at R_{S2}.

For reference, the THD of a similar but nonbootstrapped circuit (i.e., Q1 jumpered) was about 0.1% at 10 kHz at a 3 V rms output level from U2, varying from a low of 0.01% at 1 kHz to as high as 0.2% at 20 kHz. At a fixed signal frequency of 10 kHz, Photo 1 shows this second harmonic distortion, at a level of 0.1%. The upper trace is the U2 output, while the lower trace is the distortion analyzer output set to a resolution of 0.3% full scale.

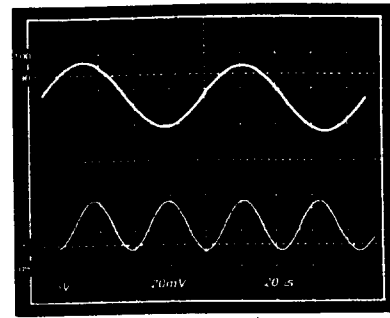


Photo 1. Output Signal (Top) and Distortion Components (Bottom, 0.3% Full Scale). Conditions: $V_S \pm 15$ V, Figure 1 Circuit, Without Bootstrapping, 3 V rms Out.

In contrast, Photo 2 shows the distortion under bootstrapped conditions, with a resolution of 0.03% full scale for the lower trace. In this case the harmonic distortion has essentially disappeared into the residual noise, indicating the potency of the bootstrap circuit.

UNBUFFERED BOOTSTRAP

It is worthwhile to note that the basic principle of this bootstrap will still operate to some degree without buffer amplifier U2, that is with U1 driving the load direct. However, the distortion null will not be as deep as it is shown in Photo 2, and it will also vary with loading.

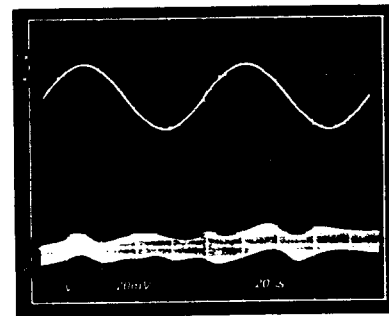


Photo 2. Output Signal (Top) and Distortion/Noise Components (Bottom, 0.03% Full Scale). Conditions: $V_S \pm 15$ V, Figure 1 Circuit, With Bootstrapping, 3 V rms Out.

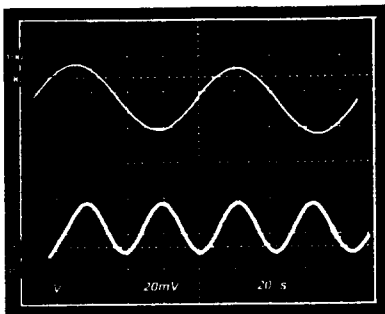


Photo 3. Output Signal (Top) and Distortion Components (Bottom, 0.1% Full Scale). Conditions: $V_S \pm 15\text{ V}$, Unbuffered U1 in Figure 1 Circuit, With Bootstrapping, 3 V rms Out.

Photo 3 shows this condition, where U1 drives the bootstrap divider directly, and the THD measures 0.03%, using a scale factor of 0.1% in the lower trace. For this example, this represents about a 10 dB distortion reduction over the same circuit conditions without the bootstrap.

The deterioration of distortion null is because U1 is called upon to deliver output current, which must pass through Q1. The V_{BE} of bootstrap transistor Q1 will then change with U1 load current, degrading the bootstrap tracking of the input drive to U1. The circuit selection choice is a trade-off between simplicity and less performance for the unbuffered case, versus the complexity of an additional IC, but much greater overall performance for the fully optimized Figure 1 version.

APPLICATION TIPS

For other operating hints, maximum output will be a function of the power supplies, and will be 7 V rms or more with the $\pm 15\text{ V}$ supplies used here. For supply voltages of $\pm 12\text{ V}$ or more a clip on heat sink is recommended when the AD811AN is used for U2 (Aavid 5801). For low impedance loads, the supplies should be well bypassed with large electrolytics, returned to the load common point.

Finally, it should be noted that the general principles of the nonlinear C/V input characteristic distortion mechanism apply to virtually all JFET input IC op amps available today, independent of their source. Bipolar input op amps built on junction isolated processes can also be subject to the phenomenon, and may also benefit from bootstrapping. However they are not as likely to be used with large source impedances where the distortion magnitudes become a serious problem, as is true in the case of JFET op amps.

References

- ¹Analog Devices AD743 data sheet.
- ²Analog Devices AD744 data sheet, Figures 16 and 20.
- ³Dave Whitney and Walt Jung, "Applying a High-Performance Video Operational Amplifier," *Analog Dialogue*, Vol. 26-1.