ANALOG DEVICES

AN-210
APPLICATION NOTE

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Adding Additional Input Channels to the AD7773/AD7775

by John Wynne

The AD7773 and AD7775 accept differential input signals through the differential input pins, $V_{IN}(+)$ and $V_{IN}(-)$. However, a special mode exists which disconnects the output of the rectifier from the $C_{INT}(+)$ pin and allows single-ended input signals to be applied via the $C_{INT}(+)$ pin. Locations CR7, CR8 and CR9 of the 10-bit wide Control Register are decoded to provide a number of different functions and modes of operation within the AD7773 and AD7775. CR7 determines whether a signal will be acquired via the synchronous detector's differential inputs or direct from the $C_{INT}(+)$ pin. $\overline{CR7}$ is ANDed with the internally generated integrate signal INT to make or break the signal path from the rectifier output to the $C_{INT}(+)$ pin. With CR7 low the rectifier output drives the external integrating capacitor on the C_{INT} pins, and all input signals are acquired through the $V_{IN}(+)$ and $V_{IN}(-)$ differential input pins. With CR7 high the synchronous detector stage is bypassed, and all input signals are now acquired through the single-ended $C_{INT}(+)$ pin. Table I shows the different options/modes available and their respective addresses.

Table I. Functional Address Decoding for the AD7773 and AD7775

CR9	CR8	CR7	Function
0	0	X	Soft Reset
0	1	X	Power Down
1	0	0	Not Allowed
1	0	1	Calibration Mode
1	1	0	Normal Mode
1	1	1	Bypass Mode

X = Don't Care

Bypass Mode: In this mode the synchronous detector, rectifier and integrator are bypassed and the single-ended input signals to be captured are now applied via the $C_{INT}(+)$ pin, the C_{INT} capacitor having been removed. To select the bypass mode locations, CR7, CR8 and CR9 of the control register are loaded with logic highs. A simplified timing diagram of the channel operating in the bypass mode is shown in Figure 1.

When CTRL goes high at the start of a signal capture, the input begins to be tracked by one of the four T/H amplifiers. On the falling edge of CTRL, the tracking T/H amplifier is put in the hold mode, and the voltage on its hold capacitor remains held for subsequent A/D conversion. Unlike the synchronous detector mode the discharge switch, SW3, remains open between successive CTRL signals. When the number of bypass signals captured equals the preprogrammed number expected, the capture sequence ends and the held voltages are sequentially applied to the ADC and converted. From here on, channel operation is identical to the Synchronous Detector mode as described in the AD7773/AD7775 data sheet. Note that locations SR1–SR4 of the Status Register now convey no meaningful information and should be ignored for Bypass Detector operation.

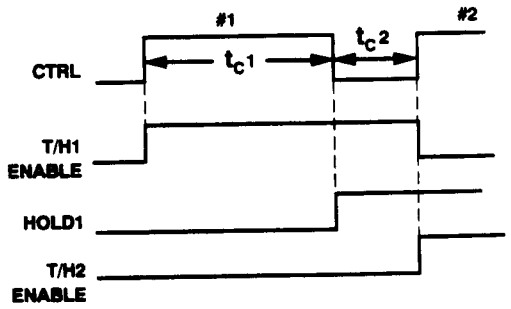

Figure 1. Channel Timing Wafeforms in Bypass Mode

There are a number of considerations which should be followed when changing between modes. The first is that no mode change be attempted before the burst capture and conversion sequence is complete, i.e., not until location SR0 of the Status Register returns low. This will avoid any inadvertent corruption of a conversion in progress. The second consideration involves the delay between writing to the Control Register and starting a new burst capture sequence. This time is defined under the Demodulator Timing Characteristics as the $\overline{WR}$ rising edge to CTRL rising edge and is specified as

00 ns minimum. It is required to ensure that the correct onditions have been set up internal to the device.

A final consideration involves allowing sufficient time or the integrating capacitor, C_{INT}, to discharge when ging from the Bypass mode to one of the other ating modes. This is necessary since C_{INT} is not lischarged by the internal discharge switch, SW3, either etween successive CTRL pulses or even on completion f the burst capture sequence. A discharge time of 00 ns—equivalent to t_C2, the CTRL Low time in Figure 1 -is adequate after transferring out of the Bypass mode. his discharge time and the previous set up time of 00 ns must be added together to arrive at a final overall lelay of 500 ns.

Adding Extra Channels

Figure 2 shows a recommended circuit for adding one extra input channel to the AD7773 and AD7775. Figure 3 shows the recommended circuit for multiple input channels. Op amps A1 and A2 can be an OP-292 from Analog Devices, a dual op amp designed for single +5 V operation. Op amp A3 is a transconductance amplifier such as the CA3080 from RCA. This amplifier must be gated OFF via its bias input pin when the Bypass mode is not selected. The analog input voltage signal(s) to both circuits is expected to range from 0 V to 1.2 V.

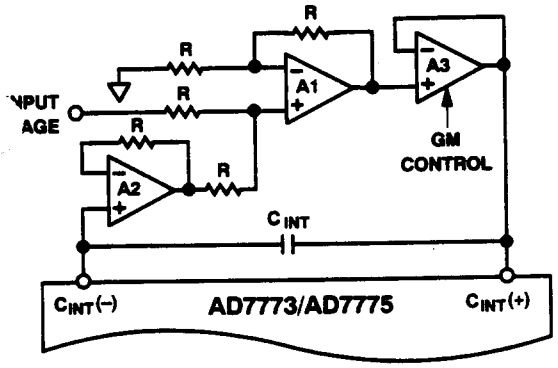

Figure 2. Adding One Additional Input Channel to the AD7773 and AD7775

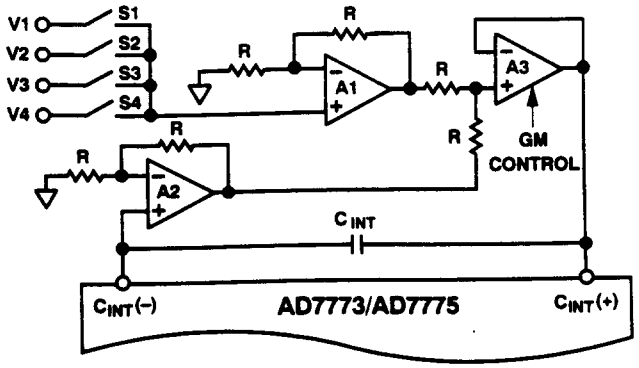

Figure 3. Adding Four Additional Input Channels to the AD7773 and AD7775