Recovering the DIR PLL Operation on the ADAV801 and ADAV803
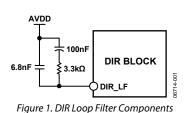## by Xavier Eckel

INTRODUCTION

The ADAV801 and ADAV803 are stereo codecs intended for applications such as DVD or CD recorders that require high performance. Throughout the application note, ADAV80x refers to the ADAV801 and ADAV803 codecs. One of the features of the ADAV80x is that it contains an integrated S/PDIF receiver. The receiver uses two pins, DIRIN and DIR_LF. DIRIN accepts the S/PDIF input stream. DIR_LF is a loop filter pin, required by the internal PLL, which is used to recover the clock from the S/PDIF data stream.

This application note describes a problem that can occur when the S/PDIF connector is disconnected and reconnected several times successively. The problem can also happen when a nonstandard S/PDIF signal is sent to the DIRIN pin. A solution to this problem is then presented. Finally, an approach to detect when the problem is happening with a microcontroller is proposed.

INITIAL CONDITIONS

Figure 1 presents the recommended components used to form the loop filter connected to the DIR_LF pin. An increase of the loop filter bandwidth results in better jitter performance of the recovered clock. However, it also reduces the stability and locking capability of the PLL. Therefore, those components have been chosen as a trade-off between locking stability and jitter performance.

Figure 1. DIR Loop Filter Components

The configuration of the ADAV80x does not really matter. The only common setting is that the S/PDIF receiver is being used. For the sake of the example, consider a simple configuration where the signal received by the S/PDIF receiver is sent to the DAC. Figure 2 illustrates this configuration.
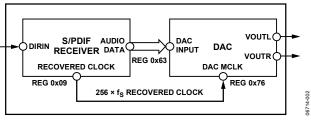

Figure 2. Configuration Example

Table 1 describes the register settings for this configuration. All the other registers are left to their default values.

Table 1. Configuration Example Register Settings

Register Name	Register Address	Register Value	Description
Receiver Configuration 1 Register	0x09	0x26	Recovered clock = 256 × f_S
Datapath Control Register 2	0x63	0x09	DAC source = DIR
DAC Control Register 1	0x64	0x03	DAC outputs unmuted
Internal Clocking Control Register 1	0x76	0xA0	DAC clock source = recovered clock (256 × f_S)

DESCRIPTION OF THE PROBLEM

It has been observed that the DIR PLL can unlock and stop operating properly when the S/PDIF connector is disconnected and reconnected several times successively. This problem is more frequent when a lower cost S/PDIF connector than the one on the ADAV80x evaluation board is used. Therefore, the use of the Toshiba TORX173 S/PDIF connector is recommended.

The fact that the DIR PLL stops operating properly can be observed on the DIR_LF pin. When no signal is provided to the DIRIN pin or when the DIR PLL doesn't lock, the voltage at the DIR_LF pin is 3.3 V. When a signal is provided to the DIRIN pin and the DIR PLL locks, then the voltage at DIR_LF is somewhere between 1.5 V and 2 V. This voltage depends on the sample rate of the input data. However, when the DIR PLL stops operating properly, the voltage at DIR_LF is 0 V whether a signal is provided to the DIRIN pin or not.

SOLUTION TO THE PROBLEM

There is a software solution to recover the DIR PLL operation. Bit 5 (S/PDIF_SOFT_RESETB) in the VCO Test Register (Address 0x7F) enables the reset of the S/PDIF section. Resetting the S/PDIF section makes the DIR PLL lock again.

Table 2 summarizes the two successive writes that need to be done to achieve the reset of the S/PDIF section.

The VCO Test Register is not described in the ADAV80x data sheet.

Table 2. Reset of the S/PDIF Section

Register Name	Register Address	Register Value	Description
VCO Test Register	0x7F	0x00	Resets the S/PDIF section
		0x20	Takes the S/PDIF section out of reset

DETECTION OF THE PROBLEM

Using the NoStream and Lock bits of Register 0x18 (Receiver Error Register) to generate an interrupt could be a way to detect when the DIR PLL is not operating properly.

When set properly, these bits make the ZEROL/INT pin go high when the DIR PLL locks or unlocks, or when there is no stream present at the S/PDIF receiver. The pin goes back to low when Register 0x18 is read. However, when the DIR PLL stops operating properly, the ZEROL/INT pin remains high no matter how many times Register 0x18 is read. This could be used to detect the DIR PLL problem.

Table 3 describes the different writes that must be achieved to make the Lock and NoStream bits generate interrupts.

The interrupt generated by the Lock and NoStream bits of Register 0x18 makes the RxERROR bit equal to 1, which makes the ZEROL/INT go high.

Table 3. Register Settings for Generating Interrupts

Register Name	Register Address	Register Value	Description
DAC Control Register 4	0x67	0x40	Sets the ZEROL/INT pin to function as an interrupt pin
Interrupt Status Mask Register	0x1D	0x01	Sets the RxERROR bit of Register 0x1C to generate an interrupt when it is equal to 1
Receiver Error Mask Register	0x19	0x05	Sets the Lock and NoStream bits of Register 0x18 to generate an interrupt when the DIR PLL locks or unlocks, or when there is no stream

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