

## Measuring a Loudspeaker Impedance Profile Using the AD5933

by Sean Brennan

### INTRODUCTION

This application note describes the circuit architecture and details required to measure the impedance profile of a commercial loudspeaker using the AD5933 impedance-to-digital converter. By evaluating the acoustic properties of loudspeakers through an impedance measurement from 1960 to 1970, two Australian pioneers, N. Thiele and R. Small, defined the Thiele-Small parameters. Thiele and Small analyzed the electro-mechanical behavior of a speaker voice coil, magnet, and cone interacting with the cone suspension and the air in and outside sealed enclosures. To this day, these findings continue to be regarded by manufacturers and hobbyists as a standard for designing high fidelity speaker cabinets and crossover networks<sup>1</sup>, as well as for testing the final driver networks. Measuring the impedance of a commercial loudspeaker typically involves using various tools

ranging from simple lab equipment (for example, signal generators, oscilloscopes, and digital voltmeters) to PC sound cards and expensive audio network analyzers. A fundamental problem exists: the impedance test equipment remains separate from the audio system driving the loudspeaker.

This application note describes a circuit architecture using the AD5933 that allows the system designer to measure the impedance profile of the loudspeaker and integrate this circuitry into the audio signal chain. This offers many benefits. Upon system power-up, for example, the circuitry provides the ability to measure the impedance profile and thus the acoustic properties of the loudspeaker, enabling direct comparison to a factory-calibrated profile stored nearby. Any changes in the impedance profile are detected and further diagnostics are carried out, preventing premature damage.

<sup>1</sup> For more information, see Chapter 8 (Page 101), "Speaker Crossovers," by Hank Zumbahlen, in the *Systems Application Guide*. Published by Analog Devices, Inc., 1993, ISBN 0-916550-13-3.

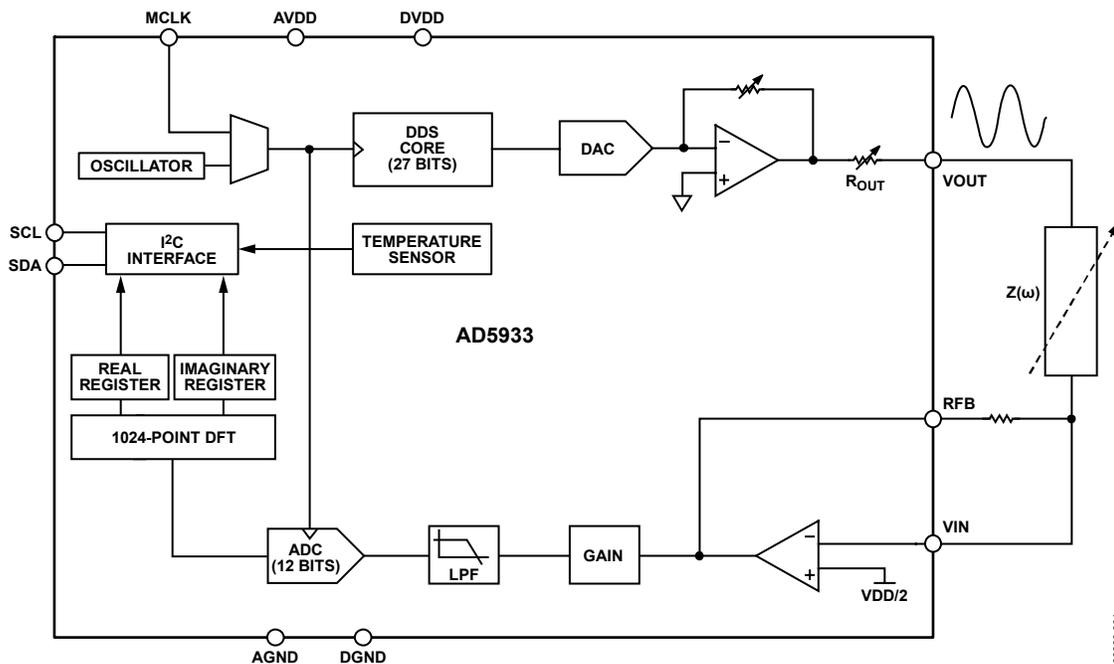


Figure 1. AD5933 Functional Block Diagram

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## OPERATION AND CALIBRATION

As shown in Figure 1, the AD5933 is a high precision, impedance converter system that combines an on-board frequency generator with a 12-bit, 1 MSPS, analog-to-digital converter (ADC). The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on-board ADC, and a discrete Fourier transform (DFT) is processed by an on-board DSP engine. The DFT algorithm returns a real (R) and imaginary (I) data-word at each output frequency. The magnitude of the impedance and relative phase of the impedance at each frequency point along the sweep are easily calculated using the following two equations:

$$\text{Magnitude} = \sqrt{R^2 + I^2} \quad (1)$$

$$\text{Phase} = \text{Tan}^{-1}(I / R) \quad (2)$$

The system requires calibration using a precision (preferably noninductive) resistor substituted for the impedance to be measured and a scaling factor is calculated for subsequent measurements. The AD5933 can measure an impedance value between 100  $\Omega$  to 10 M $\Omega$  to a system accuracy of 0.5% for excitation frequencies between 1 kHz to 100 kHz. A typical loudspeaker has a common-mode impedance of 4  $\Omega$  to 6  $\Omega$  or less and rises up to 30  $\Omega$  to 50  $\Omega$  at the peak frequency. The peak frequency can occur as low as 20 Hz. Therefore, external circuit components are required to analyze the loudspeaker impedance profile at such low frequencies and impedance levels. The following section explains the proposed circuit architecture to measure such a profile and compare the results to a commercial test unit.

### LOUDSPEAKER IMPEDANCE MODEL AND PROFILE

To understand the subsequent measurement, a simplified electrical model of a loudspeaker is shown in Figure 2.

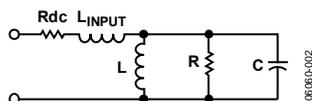


Figure 2. Loudspeaker Impedance Model

The circuit in Figure 2 has a dc resistance placed in series with a lossy parallel resonant circuit made up of L, R, and C, which models the dynamic impedance of the speaker over the frequency range of interest.

- Rdc is the dc resistance of the loudspeaker measured with a digital ohmmeter. The dc resistance is often referred to as the DCR in a speaker/subwoofer data sheet. The dc resistance measurement is usually less than the driver's nominal impedance. Rdc is typically less than the specified loudspeaker impedance and the novice loudspeaker enthusiast may be fearful that the driver amplifier will be overloaded. However, because the inductance (L) of a speaker increases with an increase in frequency, it is

unlikely that the driver amplifier actually sees the dc resistance as its load.

- L is the voice coil inductance measured in millihenries (mH). Typically, the industry standard is to measure the voice coil inductance at 1000 Hz. As frequencies increase above 0 Hz, there is a rise in impedance above the Rdc value. This is because the voice coil acts as an inductor. Consequently, the overall impedance of a loudspeaker is not constant impedance, but can be represented as a dynamic profile that changes with input frequency (see Figure 3). Maximum impedance (Zmax) of the loudspeaker occurs at the resonant frequency (Fs) of the loudspeaker. See Figure 4.
- Fs is the resonant frequency of a loudspeaker. The impedance of a loudspeaker is a maximum at Fs. The resonant frequency is the point at which the total mass of the moving parts of the loudspeaker become balanced with the force of the speaker suspension when in motion. The resonant frequency information is important to prevent an enclosure from ringing. In general, the mass of the moving parts and the stiffness of the speaker suspension are the key elements that affect the resonant frequency. A vented enclosure (bass reflex) is tuned to Fs so that the two work in unison. As a rule, a speaker with a lower Fs is better for low-frequency reproduction than a speaker with a higher Fs.
- R represents the mechanical resistance of a driver's suspension losses.

Therefore, to obtain the Thiele-Small parameters, the resulting impedance peak and crossover frequencies must be accurately determined.

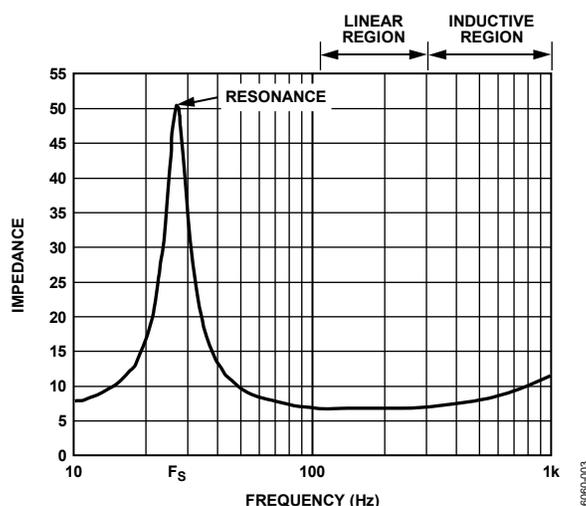


Figure 3. Typical Loudspeaker Impedance Profile

Figure 3 shows a typical impedance curve for a loudspeaker.

There are three distinct characteristics to note in Figure 3. Resonance causes a large increase in the loudspeaker impedance and, as the input frequency increases, the inductance of the voice coil causes the loudspeaker impedance to rise again. In Figure 3, resonance is  $\approx 28$  Hz, and the linear region ranges from approximately 100 Hz to 350 Hz. At the resonant frequency, the loudspeaker impedance is modeled as pure resistance. In addition, as the input frequency increases approaching resonance frequency ( $F_s$ ), the impedance profile is inductive. Beyond the resonant frequency, as impedance falls, the impedance profile is capacitive in nature.

Within the linear region of Figure 3, the impedance is mainly resistive, but at slightly below the speaker's nominal impedance.

In the inductive region, where the inductance of the speaker voice coil becomes significant, the speaker impedance starts to increase again and is progressively more inductive as the frequency rises.

## CIRCUIT DETAILS

Figure 4 shows the circuit block diagram used to measure the impedance profile of a commercial loudspeaker. The circuit consists of three major blocks.

One major block is a modified Howland current source and gain stage connected to the output of the AD5933 with a commercial loudspeaker connected in the feedback loop of the external gain stage.

Another block is a clock-dividing circuit, which scales down the master clock/crystal frequency supplied to the AD5933, enabling the impedance profile to be analyzed across the bandwidth of interest (10 Hz to 20 kHz). Clock scaling is required by the AD5933 to analyze frequencies below 10 kHz.

The third block is the AD5933 impedance-to-digital converter.

The following sections explain the circuit details of the Howland current source and clock-dividing circuitry. For more information, refer to the AD5933 data sheet.

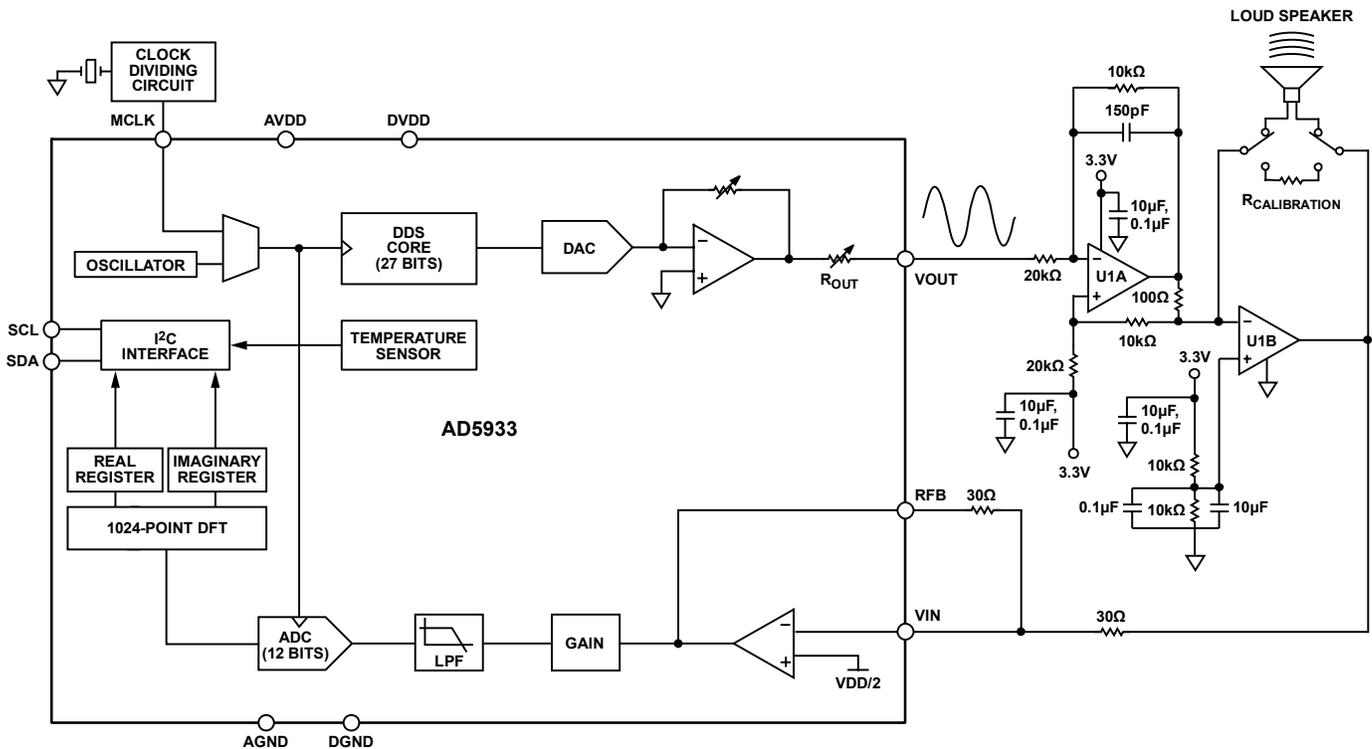


Figure 4. Loudspeaker Impedance Measurement Circuit

## HOWLAND CURRENT SOURCE

The classic Howland constant current source is shown in Figure 5. Using suitable external components around the operational amplifier, the output current through the load impedance ( $Z_{LOAD}$ ) is independent of the absolute impedance of the load and only depends on the amplitude of the input voltage ( $V_{INPUT}$ ).

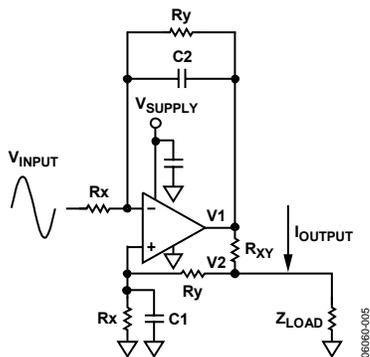


Figure 5. A Typical Howland Current Source

Using simple circuit analysis and the traditional equations for the gain of an op amp at both negative and the positive input terminals, the voltage at the op amp output pin can be written as:

$$V_1 = \frac{-R_y}{R_x} \times V_{INPUT} + V_2 \left( \frac{R_x}{R_x + R_y} \right) \times \left( 1 + \frac{R_y}{R_x} \right) \quad (3)$$

Rearranging Equation 1, it can be shown that

$$V_1 - V_2 = \frac{-R_y}{R_x} \times V_{INPUT} \quad (4)$$

Finally, the current through Resistor  $R_{XY}$  is given by

$$I_{OUTPUT} = \frac{V_1 - V_2}{R_{XY}} = \frac{-R_y}{R_x \times R_{XY}} \times V_{INPUT} \quad (5)$$

For the circuit in Figure 5 to function correctly, the circuit designer must ensure that the value of  $R_y$  is always much greater than  $R_{XY}$ . Consequently, through a suitable choice of resistors ( $R_y$  and  $R_{XY}$ ) the direction of the current  $I_{OUTPUT}$  can be assumed to flow through the load in accordance with the current divider rule. Equation 5 gives the magnitude of the output current.

Because the Howland circuit uses both positive and negative feedback, the circuit designer must ensure that the circuit output remains stable during and after power sequencing and over all required load conditions. The circuit designer should include a suitable sized Capacitor  $C_2$  to provide a single dominant pole in the negative feedback circuit to prevent sustained oscillations.

In the absence of an output load, when the power supply ( $V_{supply}$ ) is first applied to the circuit shown in Figure 5 (open circuit output conditions), the positive feedback may equal the negative feedback. The inclusion of a suitable Capacitor  $C_1$  ensures that the positive feedback is always less than the negative feedback under such conditions.

## MODIFIED HOWLAND CURRENT SOURCE

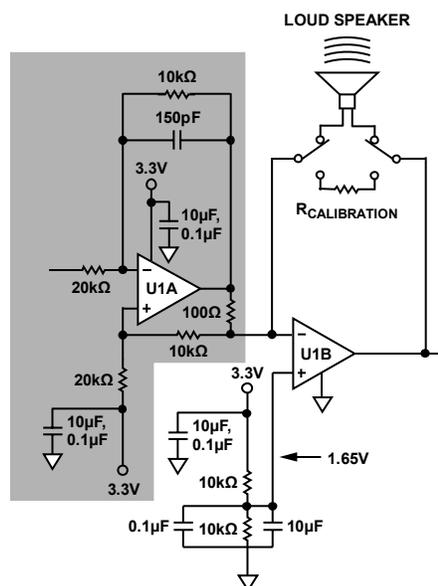


Figure 6. Modified Howland Current Source  
(U1A, U1B = AD8532AR Rail-to-Rail Single-Supply Amplifier)

The highlighted section of Figure 6 shows the modified Howland current source used in the final circuit. Because of the limitation of a single supply, coupled with the fact that the receive side of the AD5933 is internally hard biased at  $V_{DD}/2$ , it is necessary to bias the excitation signal through the loudspeaker at the same value to get the best dynamic range through the system. This is achieved by biasing the noninverting input of U1B at 1.65 V (that is,  $V_{DD}/2$ ). The high open-loop gain of the op amp and the application of feedback causes the output of the Howland current source always to be at the same voltage. Therefore, the output of the Howland current source is always at 1.65 V.

Next, the 20 kΩ resistor is connected to the 3.3 V supply and decoupled to ground. The 10 kΩ resistor in the feedback loop of U1A causes the noninverting input of U1A to be at 2.2 V ( $V_{DD} = 3.3$  V). This is necessary to allow the excitation current to always flow through the speaker over the entire 2 V p-p voltage swing biased about 1.65 V (Range 1 of the AD5933 as described in the device data sheet).

Using the superposition theorem, and considering the bias at the output and input terminals around the U1A amplifier, it can be shown that for a 2 V p-p input signal, the maximum/minimum voltage swing at the output of U1A is 2.975 V/1.975 V, respectively.

Therefore, there is always current flowing into the 100 Ω resistor and into the loudspeaker. This is required so that the impedance profile is a smooth, continuous profile like that shown in Figure 3.

The resulting current (10 mA p-p) from the Howland current source, which flows through the 100 Ω resistor and into the loudspeaker impedance, develops an output voltage on the U1B output ( $\approx 10$  mV per ohm of measured impedance—about U1B)

which is proportional to the loudspeaker impedance. This voltage is connected to the AD5933 through the unity gain ( $R_{fb} = R_{in} = 30 \text{ k}\Omega$ ) current-to-voltage (I-to-V) amplifier and PGA before being sampled by the ADC. When the PGA is set to  $\times 5$ , the ADC sees a 1.5 V p-p signal.

It is recommended to configure the AD5933 I-to-V gain and the PGA gain such that the signal presented to the ADC uses the dynamic range of the ADC without causing saturation over the entire range of the loudspeaker impedance.

### AD5933 DFT DETAILS

The AD5933 method of determining the impedance (see the AD5933 data sheet for impedance calculation details) involves the use of the DFT. The DFT offers many benefits to the user including:

- Excellent dc rejection
- Error averaging
- Phase information

The conventional DFT method assumes a sequence of periodic data samples  $x(n)$  which allows the user to determine the spectral content of the corresponding continuous signal. Internally, these samples come from the on-board 12-bit ADC of the receive side. The method employed by the AD5933 differs from the conventional DFT in that only a single frequency bin is transformed, rather than a fundamental and harmonics—it is, in fact, a single-point DFT as explained in the following section.

#### Single-Point DFT

With the conventional DFT, a sequence of input samples  $x(n)$  are correlated with samples from a phasor. The frequency of this phasor is at integer multiples of a fundamental frequency given by  $f_s/N^1$ . The correlation is performed for each frequency multiple; if the resulting correlation of the phasor (consisting of both a sine and a cosine at that multiple frequency) is nonzero, there is energy in the input signal at that particular frequency bin. If no energy is found in a bin, there can be no energy at that test frequency. The single-point DFT implemented by the AD5933 ensures by design that the analysis frequency provided by the on-board DDS core is always the same. Therefore, the AD5933 is only analyzing energy at one particular frequency that is determined by the sweep parameters preprogrammed by the user.

The single-point DFT calculated at each frequency point is given by Equation 6.

$$X(f) = \sum_{n=0}^{1023} (x(n)(\cos(n) - j\sin(n))) \quad (6)$$

where:

$X(f)$  is the power in the signal at the Frequency Point  $f$ .

$x(n)$  is the ADC output.

$\cos(n)$  and  $\sin(n)$  are the sampled test vectors provided by the DDS core at the  $f$  frequency.

The multiplication is accumulated over 1024 samples for each frequency point. The result is stored in two 16-bit registers representing the real and imaginary components of the result. The data is stored in twos complement format.

#### Leakage Considerations

If the input signal to the receive side does not have an exact integral number of cycles over the N-point sample interval, there is not a smooth transition from the end of one period to the start of the next. Because the on-board ADC is sampling the receive signal for a finite time, the AD5933 is, in effect, multiplying the input sequence by a rectangular window.

The continuous Fourier transform of a rectangular function is the classic sinc function ( $\sin(\pi x)/x$ ). If the input signal to the receive side of the AD5933 contains spectral components at exactly integer multiples of the fundamental analysis frequency, then these side lobes are zero at bin frequencies and do not show up in the DFT output. If, however, the input signal contains components that do not fall exactly on these bin frequencies, then the sinc functions side lobes contain energy at the bin frequencies. It is the high frequency components inherent in the discontinuities of nonperiodic sampling that cause these side lobes to exist.

Therefore, an obvious problem exists. The DFT performed by the AD5933 only produces a correct result when the ADC output sequence  $x(n)$  contains energy precisely at the analysis frequencies that are integral multiples of the fundamental frequency. If the input signal has a component at some intermediate frequency between these frequency bins, this input signal shows up to some degree in all of the N output frequency bins of the DFT. In a conventional DFT, this can have the undesirable effect of masking out weaker signals that are present and close to stronger ones in the input signal. This is called spectral leakage.

The method employed by the AD5933 for reducing the effects of spectral leakage is the application of a windowing on the ADC output data. Windowing has the effect of reducing the energy contained in the side lobes of the sinc function. When the receive side input signal does not contain an integer number of cycles within the sample interval, the ADC output has spectral leakage as previously described.

<sup>1</sup>  $f_s$  is the analog-to-digital sampling frequency.

**Example**

In the AD5933 single-point DFT that is performed, the sampling frequency ( $f_s = \text{MCLK}/16$ ) is determined by the master clock frequency applied at MCLK. If a 16 MHz clock oscillator is applied to MCLK pin of the AD5933, the ADC sampling frequency is 1 MHz. The ADC samples and converts 1024 points ( $N = 1024$ ) and provides these samples to the MAC unit to perform the DFT. This gives bin frequencies at integer multiples of ~1 kHz. Thus, for accurate DFT outputs, the input signal should be restricted to 1 kHz multiples —the resolution of the DFT is said to be 1 kHz. Therefore, the AD5933 can only accurately determine components in a signal that are 1 kHz apart, with no error. This also implies that the minimum frequency that the AD5933 can excite and analyze is 1 kHz. In practice, this is slightly higher due to finite timing, jitter, and component non-idealities that exist in real analog design.

The AD5933 uses a Hanning window, which offers good side-lobe rejection and, because of its symmetrical properties, is relatively efficient to implement in a digital engine.

There are two ways to improve the resolution of the DFT performed by the AD5933. First, assuming the user keeps the sample frequency of the ADC fixed by not changing the MCLK frequency, increasing the number of points taken by the on-board ADC increases the resolution. For example, sampling 2048 points, in result, increases the resolution to 500 Hz. Therefore, it is possible to accurately determine components in a signal that are 500 Hz apart, with no error. This takes 2 ms. Note that the number of points that the ADC samples is fixed by design.

Second, assuming that the number of points that the ADC samples of the receive signal is fixed at  $N = 1024$ , scaling the frequency at MCLK scales the sampling rate of the ADC according to Equation 7:

$$f_s = \frac{f_{\text{MCLK}}}{16} \tag{7}$$

Scaling the sampling frequency increases the span of the sample window, creating coherent sampling required for accurate results.

The Clock Divider Circuitry section details a clock dividing circuit used to scale the system clock at the MCK pin, enabling the AD5933 to analyze excitation frequencies below 10 kHz.

**CLOCK DIVIDER CIRCUITRY**

The impedance profile of a loudspeaker, as shown in Figure 3, ranges from 10 Hz to 20 kHz (typically). Therefore, to capture the entire impedance profile of the loudspeaker, the AD5933 must be able to analyze frequencies below 10 kHz. The user must scale the master clock frequency to allow the AD5933 DFT to analyze these frequencies. Figure 7 shows an example circuit that divides a master clock frequency by 2 (that is, it performs successive binary division).

The circuit uses a standard 4-pin, DIL, metal can, crystal oscillator as the reference frequency. Because the majority of oscillators are CMOS type (5 V) and the MCLK input of the AD5933 running at 3.3 V requires TTL (3.3 V) input, a few simple additions were made to the circuit. A capacitor, C1, (0.033  $\mu\text{F}$ ) was placed between the output of the NAND gate and the input of the first flip-flop. The capacitor removes the dc bias from the TTL oscillator, because the logic levels are not correct for TTL when the 5 V is reduced to 3.3 V. Next, the NAND gate U5A has a feedback resistor of 680 k, which acts as a sensitive amplifier to make the output logic levels swing from 0 V to 3.3 V for reliable switching of the first flip-flop, U1A. Alternatively, a logic-level translator like the ADG3231 can be used to translate the oscillator output logic levels. It is important that the rising and falling edges of the clock connected to Pin 8 (MCLK) of the AD5933 have a good clean transition ( $\text{tr}/\text{tf} \approx 6 \text{ ns}$ ) with small amounts of jitter. The frequency stability of any external crystal used should be 100 ppm. The measured duty cycle of the crystal oscillator used was 45% to 55%. The five dual flip-flops produce a 10-bit binary counter, allowing the AD5933 to be driven from 12 MHz to 11.718 kHz (divide by 1 to 1024). An alternative solution to the circuit in Figure 7 is to replace the five dual flip-flops with an AD9834 acting as a binary clock divider with an external high-speed comparator (ADCMP37x/ADCMP60x) on the output to produce a digitally controlled clock.

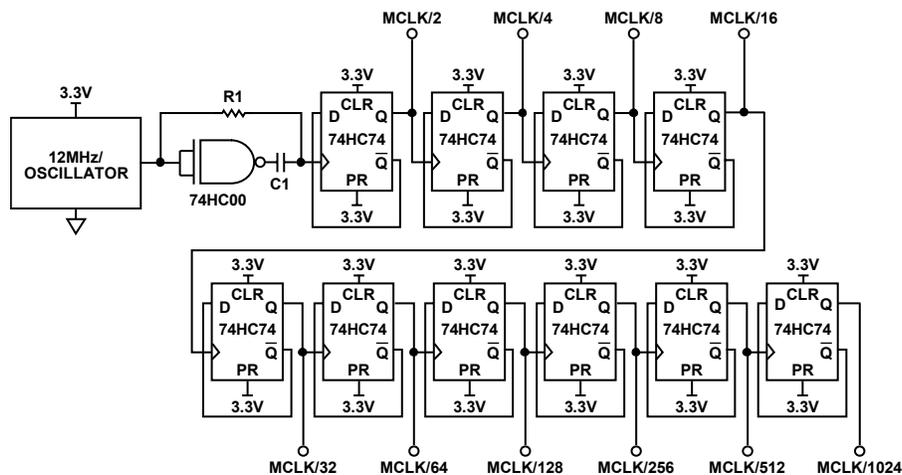


Figure 7. Master Clock Dividing Circuitry

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## LOUDSPEAKER IMPEDANCE MEASUREMENT

The circuit shown in Figure 4 was developed and used in the measurement of the loudspeaker impedance profile. The transmit side of the AD5933, used as an audio frequency oscillator, drives the modified Howland constant current source at Pin 6. The AD5933 integrated circuit impedance converter combines an internal direct digital synthesis (DDS) frequency generator and analog-to-digital converter (ADC) to form a self-contained impedance measurement system. A frequency sweep is performed by the AD5933 to gather magnitude and phase data at frequencies defined by the user. The impedance to be analyzed is placed between the frequency generator transmit stage and the I-to-V receive stage. The receive signal is passed through a programmable gain amplifier (PGA), filtered and then delivered to the 12-bit ADC. After the receive signal is digitized by the ADC, a discrete Fourier transform (DFT) is performed on the data.

A nearby microcontroller communicates to the AD5933 via the I<sup>2</sup>C<sup>®</sup> interface, allowing the user to program the AD5933 sweep parameters (start frequency, frequency step size, and number of points), configure the control register, and adjust the excitation amplitude and PGA setting, as well as read back the measured data from the AD5933 for the final impedance calculation. Once the AD5933 is correctly programmed, only a single bit in the status register must be polled after each point in the user-defined sweep to see if valid data is available to read from the AD5933 (see the AD5933 data sheet for more details).

### SYSTEM CALIBRATION

However, prior to a valid impedance measurement, the AD5933 system must undergo a calibration process. The calibration process simply requires the substitution of a known precision metal film resistor be substituted for the impedance to be measured and a scaling factor (gain factor) is calculated for subsequent measurements. The gain factor calculation is given by the following formula:

$$\text{Gain Factor} = \frac{\text{Calibration Resistor}}{\sqrt{(R^2 + I^2)}} \quad (8)$$

where  $R$  and  $I$  are the contents of the real and imaginary register (Register 0x94 to Register 0x97) at a chosen calibration point.

The gain factor is calculated by dividing a suitable known precision resistor by the magnitude of the real and imaginary data returned at a suitable frequency point in the sweep. Both the real and imaginary component are stored in two 16-bit registers which must be read after each ADC conversion and before the next frequency point in the sweep where the contents of the two registers are refreshed with new data.

The resonant impedance of a commercial loudspeaker is typically 25  $\Omega$  to 30  $\Omega$  (depending upon loudspeaker construction), as shown in Figure 3. Therefore, the calibration resistor was chosen to have a value of 27.4  $\Omega$ .

The system phase is calculated in degrees at each sweep point by the same real and imaginary data points using the formula  $\text{Phase} = \text{Tan}^{-1}(I/R)$ . The user must evaluate the quadrant in which the phase angle lies. To get the correct angle, the user must add 180 degrees in Quadrant 2 and Quadrant 3 and 360 degrees in Quadrant 4.

### LOUDSPEAKER IMPEDANCE AND PHASE CALCULATION

Once the calibration process is finished, the loudspeaker replaces the calibration resistor. After the user issues a start frequency sweep command to the control register, the AD5933 automatically sequences through the user-defined frequency sweep. The frequency sweep is calculated by contents of the three registers (start frequency, frequency step, and number of increments register). Finally, the loudspeaker impedance at each frequency point is calculated by the microprocessor communicating to the AD5933. This is accomplished by multiplying the gain factor by the magnitude of the complex code returned at each frequency by the AD5933.

$$Z_{\text{LOUDSPEAKER}} = \text{Gain Factor} \times \sqrt{(R^2 + I^2)} \quad (9)$$

where  $R$  and  $I$  are the contents of the real and imaginary register (Register 0x94 to Register 0x97) at a chosen calibration point.

The phase of the loudspeaker is calculated at each sweep point by subtracting the speaker phase from the calibration phase.

$$\theta_{\text{LOUDSPEAKER}} = \theta_{\text{CALIBRATION}} - \theta_{\text{SWEEP}} \quad (10)$$

## SYSTEM CLOCK SETTINGS

As explained in the AD5933 DFT Details section, the frequency of the clock applied to MCLK must be divided in order for the AD5933 to analyze excitation frequencies lower than 10 kHz accurately. Table 1 outlines the programmed sweep range and the corresponding clock frequencies applied to the MCLK pin of the AD5933 used in the test to cover the 20 kHz to 10 Hz bandwidth.

The circuit shown in Figure 7 provides the AD5933 clock frequencies for each subrange by binary division of a 12 MHz crystal oscillator. As the start frequency is reduced by a factor of 2, the corresponding master clock frequency is halved.

Table 2 outlines the programmed sweep parameters (start frequency, frequency increment, and number of increments) used in the test to cover the 20 kHz to 10 Hz bandwidth. As shown in Figure 3, the peak impedance typically occurs between 20 Hz to 40 Hz and so it is necessary to have a small frequency increment in this region of the loudspeaker impedance profile to capture the sudden change in impedance at resonance. As frequency increases from the resonant point, it is not necessary to measure such small changes in frequency for the remainder of the impedance profile. Increasing the step size reduces the required test time and increases the span of impedance profile measured for a fixed number of increments.

The frequency step size was set to 1/10th of the start frequency in every sweep. Therefore, as the start frequency for the sweep increased, the frequency step size increased proportionally.

The AD5933 number of settling time cycle register was set at 15 output cycles throughout the experiment, and the number of increments was set to 99 points.

**Table 1. AD5933 MCLK Values vs. Sweep Range**

	AD5933 Sweep Range	Clock Frequency Applied to MCLK Pin
1	20 kHz to 10 kHz	12 MHz
2	10 kHz to 5 kHz	6 MHz
3	5 kHz to 2.5 kHz	3 MHz
4	2.5 kHz to 1.25 kHz	1.5 MHz
5	1.25 kHz to 625 Hz	750 kHz
6	625 Hz to 312.5 Hz	375 kHz
7	312.5 Hz to 156.25 Hz	187.5 kHz
8	156.25 Hz to 78.125 Hz	93.75 kHz
9	78.125 Hz to 39.125 Hz	46.875 kHz
10	39.125 Hz to 19.53 Hz	23.437 kHz
11	19.53 Hz to 9.76 Hz	11.71 kHz

<sup>1</sup> The AD5933 frequency sweep is determined by the contents of the start frequency, frequency increment, and number of increments register programmed by the user via the I<sup>2</sup>C interface. See the AD5933 data sheet for more details on performing a frequency sweep.

Table 3 outlines the AD5933 sweep parameters for the four sweeps required to span a frequency of 20 kHz to 1.25 Hz.

**Table 2. AD5933 Programmed Sweep Register Values**

	AD5933 Sweep Range	Programmed Start Frequency	Programmed Frequency Increment	Programmed No. of Increments
1	20 kHz to 10 kHz	10 kHz	100 Hz	99
2	10 kHz to 5 kHz	5 kHz	50 Hz	99
3	5 kHz to 2.5 kHz	2.5 kHz	25 Hz	99
4	2.5 kHz to 1.25 kHz	1.25 kHz	12.5 Hz	99
5	1.25 kHz to 625 Hz	625 Hz	62.5 Hz	99
6	625 Hz to 312.5 Hz	312.5 Hz	31.5 Hz	99
7	312.5 Hz to 156.25 Hz	156.25 Hz	15.625 Hz	99
8	156.25 Hz to 78.125 Hz	78.125 Hz	7.8125 Hz	99
9	78.125 Hz to 39.12 Hz	39.125 Hz	3.9125 Hz	99
10	39.125 Hz to 9.53 Hz	19.53 Hz	1.953 Hz	99
11	19.53 Hz to 9.76 Hz	9.76 Hz	0.976 Hz	99

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As outlined in the AD5933 data sheet, the start frequency is a 24-bit word that is programmed to the on-board RAM at Address 0x82, Address 0x83, and Address 0x84 (see the AD5933 data sheet register map). The required code loaded to the start frequency register is the result of Equation 10, based on the master clock frequency and the required start frequency output from the DDS:

$$\text{Start Frequency Code} = \left( \frac{\text{Required Output Start Frequency}}{\left( \frac{\text{MCLK}}{4} \right)} \right) \times 2^{27} \quad (11)$$

For example, looking at the first row of Table 3, if the user requires the sweep to begin at 10 kHz and has a 12 MHz clock signal connected to MCLK, the code that needs to be programmed is given by

$$\text{Start Frequency Code} = \left( \frac{10 \text{ kHz}}{\left( \frac{12 \text{ MHz}}{4} \right)} \right) \times 2^{27} \equiv 06D3A0 \text{ hexadecimal} \quad (12)$$

The user programs 0x06 to Register 0x82, 0xD3 to Register 0x83, and 0xA0 to Register 0x84.

Similarly, the frequency increment register is a 24-bit word that is programmed to the on-board RAM at Address 0x85, Address 0x86, and Address 0x87 (see the AD5933 data sheet register map). The required code loaded to the frequency increment register is the result of the formula shown in the Equation below, based on the master clock frequency and the required increment frequency output from the DDS.

$$\text{Frequency Increment Code} = \left( \frac{\text{Required Frequency Increment}}{\left( \frac{\text{MCLK}}{4} \right)} \right) \times 2^{27} \quad (13)$$

For example, if the user requires the sweep to have a resolution of 100 Hz and has a 12 MHz clock signal connected to MCLK, the code that needs to be programmed is given by

$$\text{Frequency Increment Code} = \left( \frac{100 \text{ Hz}}{\left( \frac{12 \text{ MHz}}{4} \right)} \right) \equiv 00117 \text{ hexadecimal} \quad (14)$$

The user programs 0x00 to Register 0x85, 0x11 to Register 0x86, and 0x79 to Register 0x87.

The third parameter used to define the frequency sweep is the number of increments register. This is a 9-bit word that represents the number of frequency points in the sweep. The number is programmed to the on-board RAM at Address 0x88 and Address 0x89 (see the AD5933 data sheet register map). The maximum number of points that can be programmed is 511. For example, if the sweep needs 99 points, the user programs 0x00 to Register 0x88 and 0x63 to Register 0x89.

Table 3 shows the required sweep codes and the various clock frequencies on which the codes are based. Because the master clock and the start frequency/frequency increment values scale equally by 2 in the binary division algorithm implemented, the start frequency code, the frequency increment code, and the number of increment codes are equal for each sweep. This means that the user only has to write to these three registers once for the entire test. However, to ensure an equal division by 2 each time, the user must ensure that the circuit in Figure 7 produces a clean clock signal at each output, that the reference clock is stable, and that jitter is minimized.

**Table 3. AD5933 Required Sweep Codes for Frequency Range 20 kHz to 1.25 kHz**

Programmed Start Frequency/ Required Start Frequency Code	Programmed Frequency Increment/ Required Frequency Increment Code	Programmed No. of Increments/ Required No. of Increments Code	Clock Frequency Applied to MCLK
10 kHz 0x06D3A0	100 Hz 0x001179	99 0x0063	12 MHz
5 kHz 0x06D3A0	50 Hz 0x001179	99 0x0063	6 MHz
2.5 kHz 0x06D3A0	25 Hz 0x001179	99 0x0063	3 MHz
1.25 kHz 0x06D3A0	12.5 Hz 0x001179	99 0x0063	1.5 MHz

## RESULTS

The system in Figure 4 was calibrated with a precision value  $27.4 \Omega$  resistor and a gain factor was calculated at each frequency point in the sweep using the sweep codes and clock frequencies as outlined in Table 3. The values were stored in memory in a nearby microcontroller. The calibration resistor was replaced by a commercial 5 1/4 inch commercial loudspeaker and the sweep was repeated. The impedance was calculated at each frequency point by multiplying the gain factor by the corresponding code at each frequency, as shown in Equation 7 and Equation 8. The final impedance profile as measured by the AD5933 is shown in Figure 8.

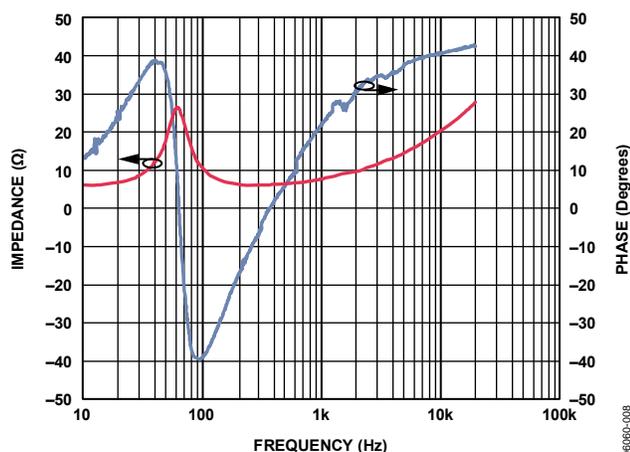


Figure 8. Loudspeaker Impedance and Phase Results as Measured by the AD5933

The same experiment was measured and repeated using the same loudspeaker. This time, however, a commercial USB-based loudspeaker impedance test unit was used. This unit required a similar calibration process at each frequency with a  $27.4 \Omega$  resistor, prior to making the final impedance measurement. The results of the measurement are shown in Figure 9.

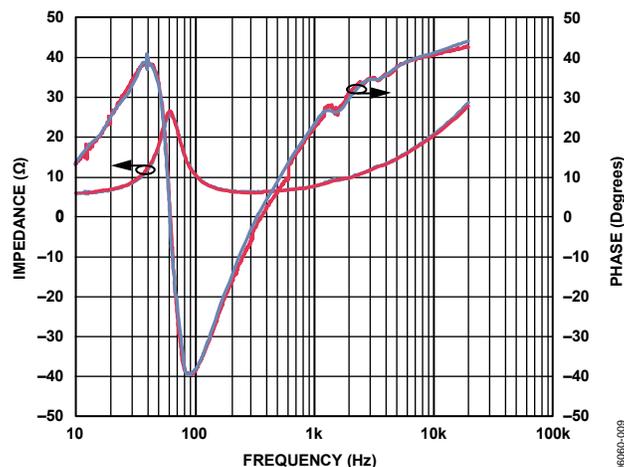


Figure 9. Loudspeaker Impedance and Phase Results as Measured by the AD5933 vs. a Commercial Loudspeaker Impedance Test Unit

## CONCLUSION

The AD5933 provides a highly accurate and low cost solution to loudspeaker impedance measurement compared to expensive commercial devices. Along with the AD5933, only a few external components are required to incorporate the simple test circuitry into the audio chain at the expense of minimum board space.

The impedance profile can be evaluated upon system power-up with minimal effort, providing a simple means of characterizing the loudspeaker acoustics and examining the effects of the loudspeaker enclosure so that aging and damage changes can be identified.

**AN-843**

## NOTES

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