

AD9779A/AD9788: Guaranteeing PLL Lock Over Temperature

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The AD9779A and AD9788 TxDAC® families implement an internal wideband clock multiplier solution with very low phase noise. The low phase noise is accomplished in part by switching optimal reactive elements into the VCO of the clock multiplier. The operating frequency of the VCO is broken up into 63 bands, where the value of the reactive components is optimized for each band. The lock ranges of each band shift over temperature. The center frequency of each band increases as the temperature decreases and the center frequency decreases as the temperatures increases.

For any given input frequency, there are two to four optimal bands. An optimal band is one that stays in lock over the entire temperature range, -40°C to +85°C. The optimal bands may not be the same for every part due to process variations. Picking one band for the lifetime of the part does not work. Therefore, a

PLL automatic band select feature is included in this part. When the PLL automatic band select mode (PLL auto mode) is enabled, the auto mode finds a band whose control voltage is at the center of the whole range at the current temperature point. Once the PLL auto mode concludes, this band, which is optimal for the current temperature, can be read back via the SPI. For optimal PLL performance over temperature, the following PLL settings should be used:

Table 1. PLL Settings

PLL SPI Control	Optimal Setting
PLL Loop Bandwidth	15
PLL VCO AGC Gain	3
PLL Bias	3

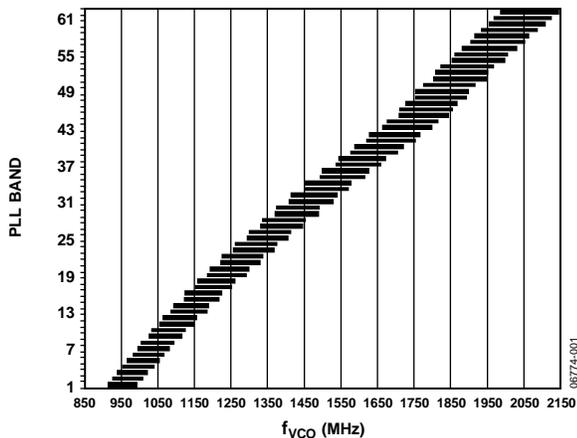


Figure 1. Typical Lock Ranges at 25°C

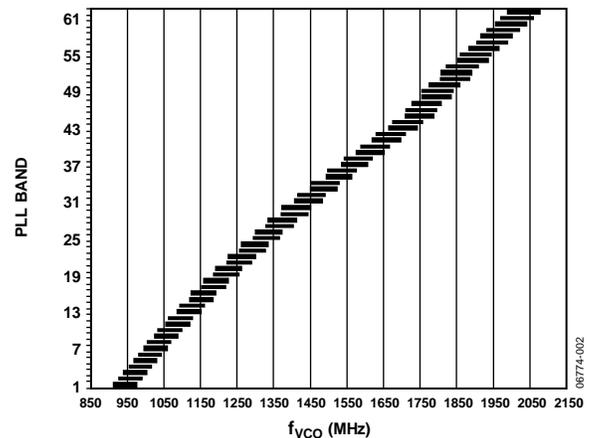


Figure 2. Typical Lock Ranges Over Temperature

There are two methods that results in guaranteed PLL lock over temperature over all parts.

METHOD 1—FACTORY CALIBRATION

The simplest solution to guarantee lock over temperature is to calibrate each system in a temperature controlled environment:

1. At room temperature (approximately $25^{\circ}\text{C} \pm 10^{\circ}\text{C}$), put the part into PLL auto mode by setting the PLL band to 63.
2. Wait for the PLL_LOCK pin or the PLL lock indicator in the SPI to go high (occurs within 5 ms).
3. Read back the 5-bit PLL band.
4. Store this value in nonvolatile memory.
5. Whenever the system starts up, load this 5-bit value into the PLL band setting via the SPI.

METHOD 2—TEMPERATURE SENSING

If factory calibration is not possible, the other solution to guarantee lock for all parts over temperature requires a temperature sensor. As mentioned previously, the PLL auto mode finds the best band for the current temperature of the device. If a part is guaranteed to start up around 25°C , then the band selected by the PLL auto mode will hold over the entire temperature range. However, if the part starts up at the temperature extremes, the band selected by the PLL auto mode may not hold at the other temperature extreme. To solve this problem, follow this procedure on system startup:

1. Set the PLL band to 63 to enable PLL auto mode.
2. Wait for the PLL_LOCK pin or the PLL lock indicator in the SPI to go high (occurs within 5 ms).
3. Read back the 5-bit PLL band.
4. Based on the temperature when the PLL auto mode is performed, set the PLL band as follows:

If the Optimal Band is in the Range of 0 to 31 (Lower VCO Frequency)

Table 2. Setting Optimal PLL Band, When Band is in the Lower Range (0 to 31)

If System Startup Temperature Is:	Set PLL Band as Follows:
-40°C to -10°C	Set PLL Band = Readback Band + 2
-10°C to $+15^{\circ}\text{C}$	Set PLL Band = Readback Band + 1
15°C to 55°C	Set PLL Band = Readback Band
55°C to 85°C	Set PLL Band = Readback Band - 1

If the Optimal Band is in the Range of 32 to 62 (Higher VCO Frequency)

Table 3. Setting Optimal PLL Band, When Band is in the Higher Range (32 to 62)

If System Startup Temperature Is:	Set PLL Band as Follows:
-40°C to -30°C	Set PLL Band = Readback Band + 3
-30°C to -10°C	Set PLL Band = Readback Band + 2
-10°C to $+15^{\circ}\text{C}$	Set PLL Band = Readback Band + 1
15°C to 55°C	Set PLL Band = Readback Band
55°C to 85°C	Set PLL Band = Readback Band - 1