

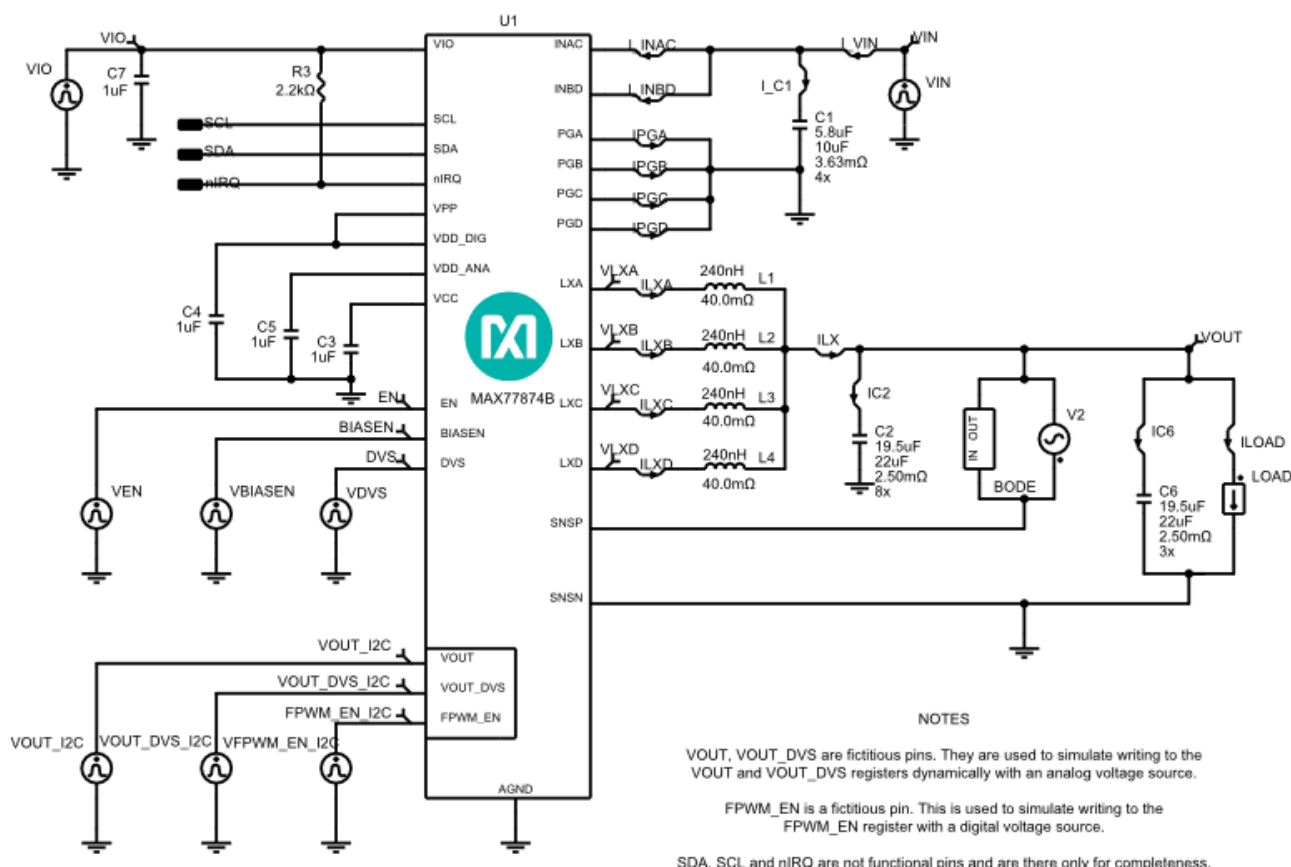
Initial Design

1.0

Design Requirements

Parameter	Value
Part Number	MAX77874B
Min. Input Voltage	3.3V
Max. Input Voltage	4.2V
Typ. Input Voltage	3.6V
Input Voltage Ripple	1%
Output Voltage	0.9V
DVS Output	1V
Output Current	11A
Output Voltage Ripple	1%
Load Step Start Current	3A
Load Step Current	11A
Load Step Edge Rate	5A/us
Output Voltage Load Step Over/Undershoot	5%
Performance Priority	Balance Efficiency and Size
BOM Priority	Cost
Mode of Operation	Forced PWM
Output Active Discharge Enable	0 = 100Ω discharge resistance is disabled when EN is low.
Step-Down Regulator Bias Enable	0 = REF, BIAS, etc. off when buck is disabled. Startup delay is 50μs (typ).
Slew Rate Selection	10 = Sets startup/softstop slew rate = 20mV/μs and DVS slew rate = 20mV/μs
Ambient Temperature	25°C

Schematic



BOM

Ref	Qty	Part Number	Manufacturer	Description
U1	1	MAX77874	Maxim Integrated	16A High-Performance Quad-Phase Buck Regulator for Multicore CPU and GPU Processors
C1	4	GRM188R61E106MA73	Murata	Cap Ceramic 10uF 25V 0603 85C
C2	8	GRM187R61A226ME15D	Murata	Cap Ceramic 22uF 10V 0603 85C
C3	1	LMK212B7105KD-T	Taiyo Yuden	Cap Ceramic 1uF 10V X7R 10% Pad SMD 0805 125°C T/R
C4	1	LMK212B7105KD-T	Taiyo Yuden	Cap Ceramic 1uF 10V X7R 10% Pad SMD 0805 125°C T/R
C5	1	LMK212B7105KD-T	Taiyo Yuden	Cap Ceramic 1uF 10V X7R 10% Pad SMD 0805 125°C T/R
C6	3	GRM187R61A226ME15D	Murata	Cap Ceramic 22uF 10V 0603 85C
C7	1	LMK212B7105KD-T	Taiyo Yuden	Cap Ceramic 1uF 10V X7R 10% Pad SMD 0805 125°C T/R
L1	1	VLS201610CX-R24M	TDK	Inductor 240nH 20% 32mOhm 4.35A Isat 3.62A Irms

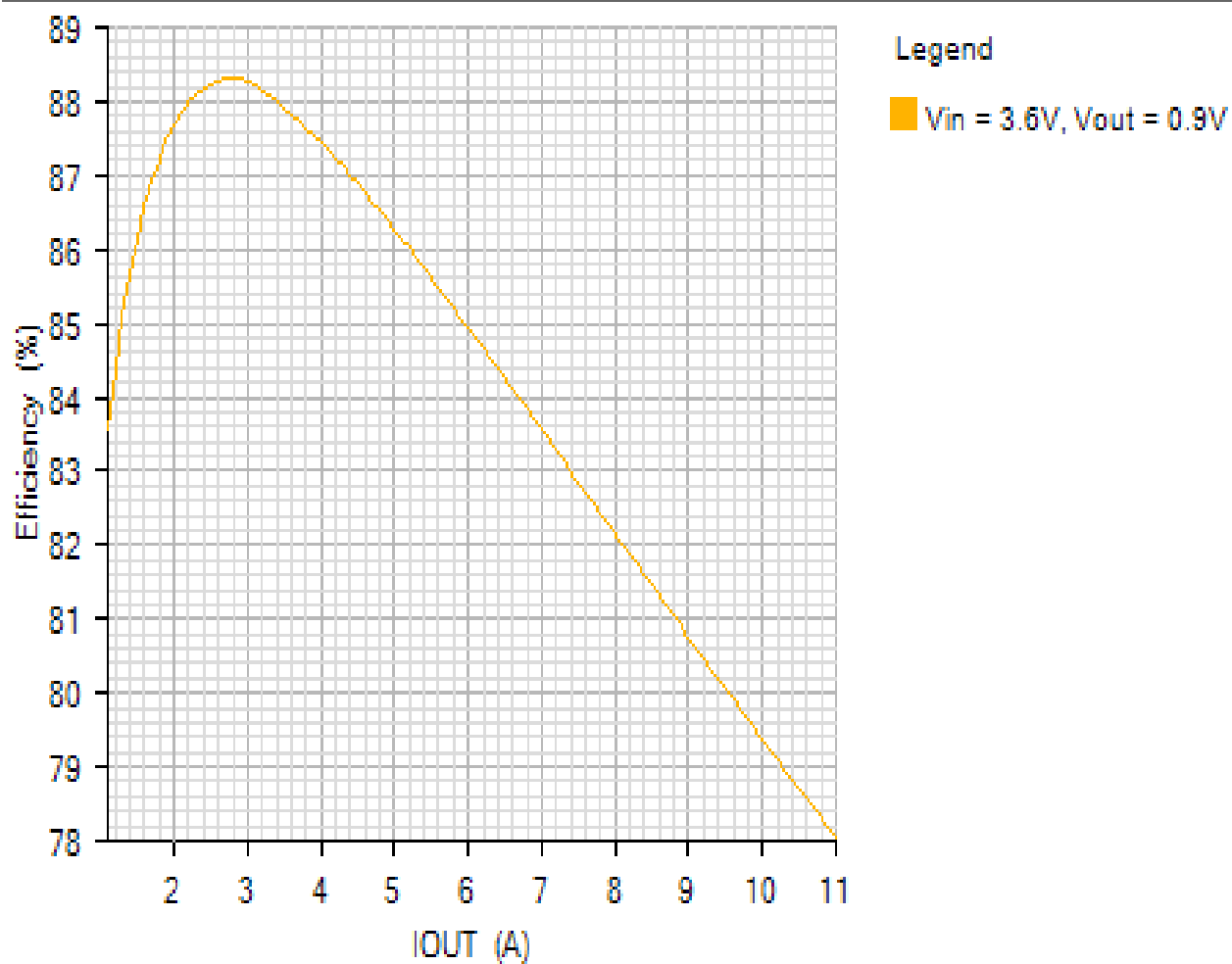
L2	1	VLS201610CX-R24M	TDK	Inductor 240nH 20% 32mOhm 4.35A Isat 3.62A Irms
L3	1	VLS201610CX-R24M	TDK	Inductor 240nH 20% 32mOhm 4.35A Isat 3.62A Irms
L4	1	VLS201610CX-R24M	TDK	Inductor 240nH 20% 32mOhm 4.35A Isat 3.62A Irms
R3	1	ERJ3GEYJ222V	Panasonic	Res Thick Film 0603 2.2K Ohm 5% 0.1W(1/10W) ±200ppm/°C Pad SMD Automotive T/R

Simulation Results

Efficiency - Sun Nov 18 2018 17:19:56

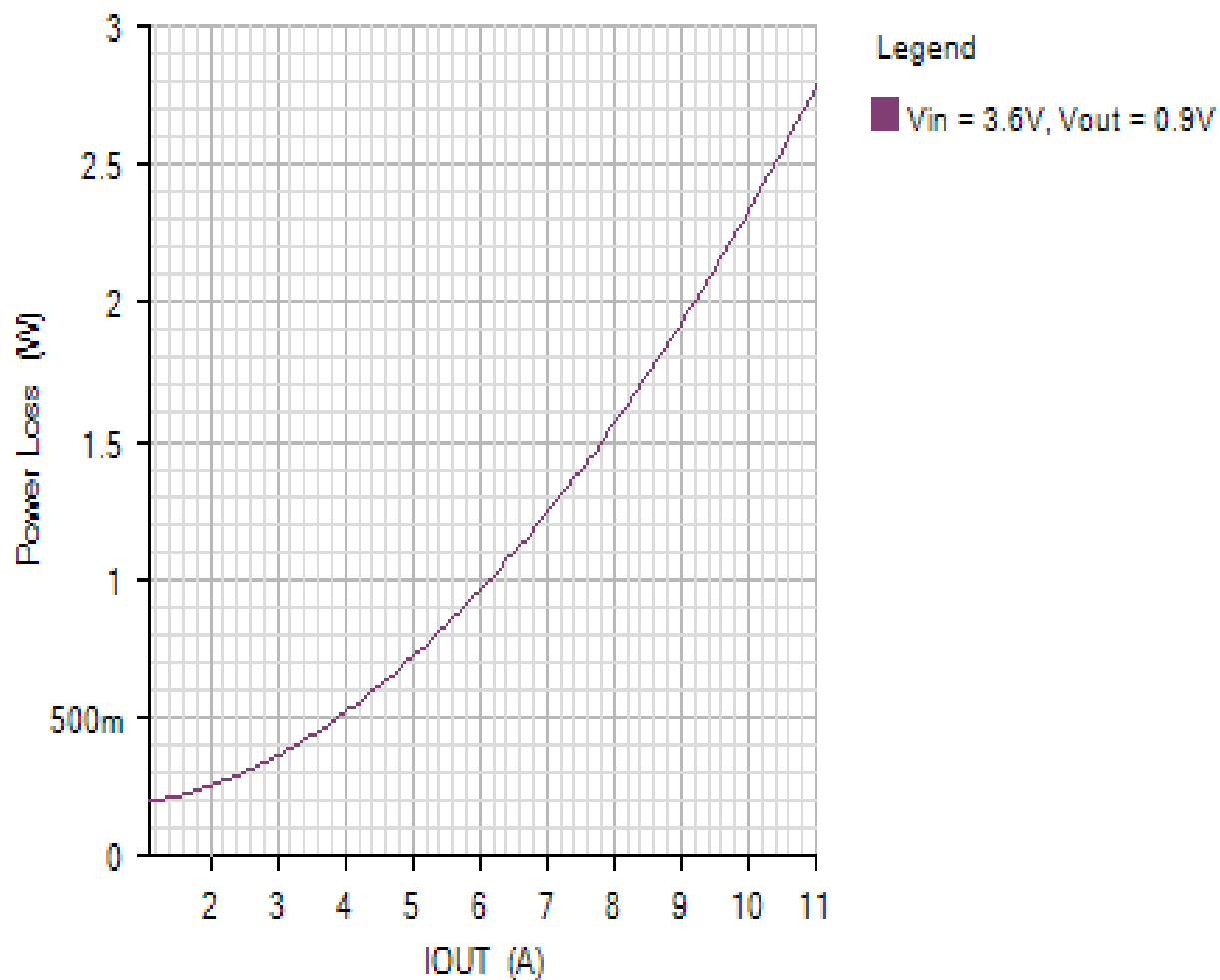
EFFICIENCY_PLOT

Default

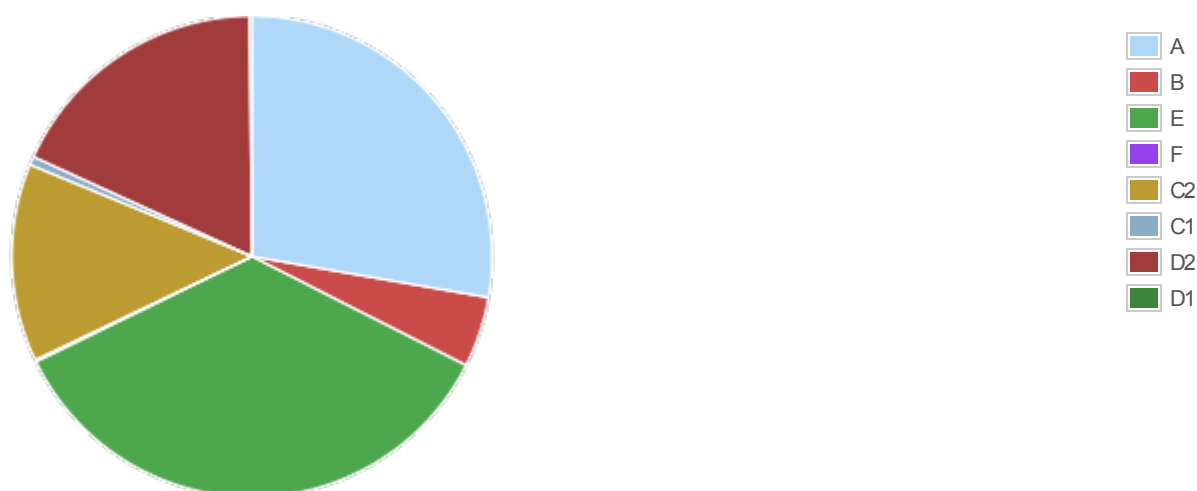


POWER_LOSS_PLOT

Default



Losses



Component

Loss (W)

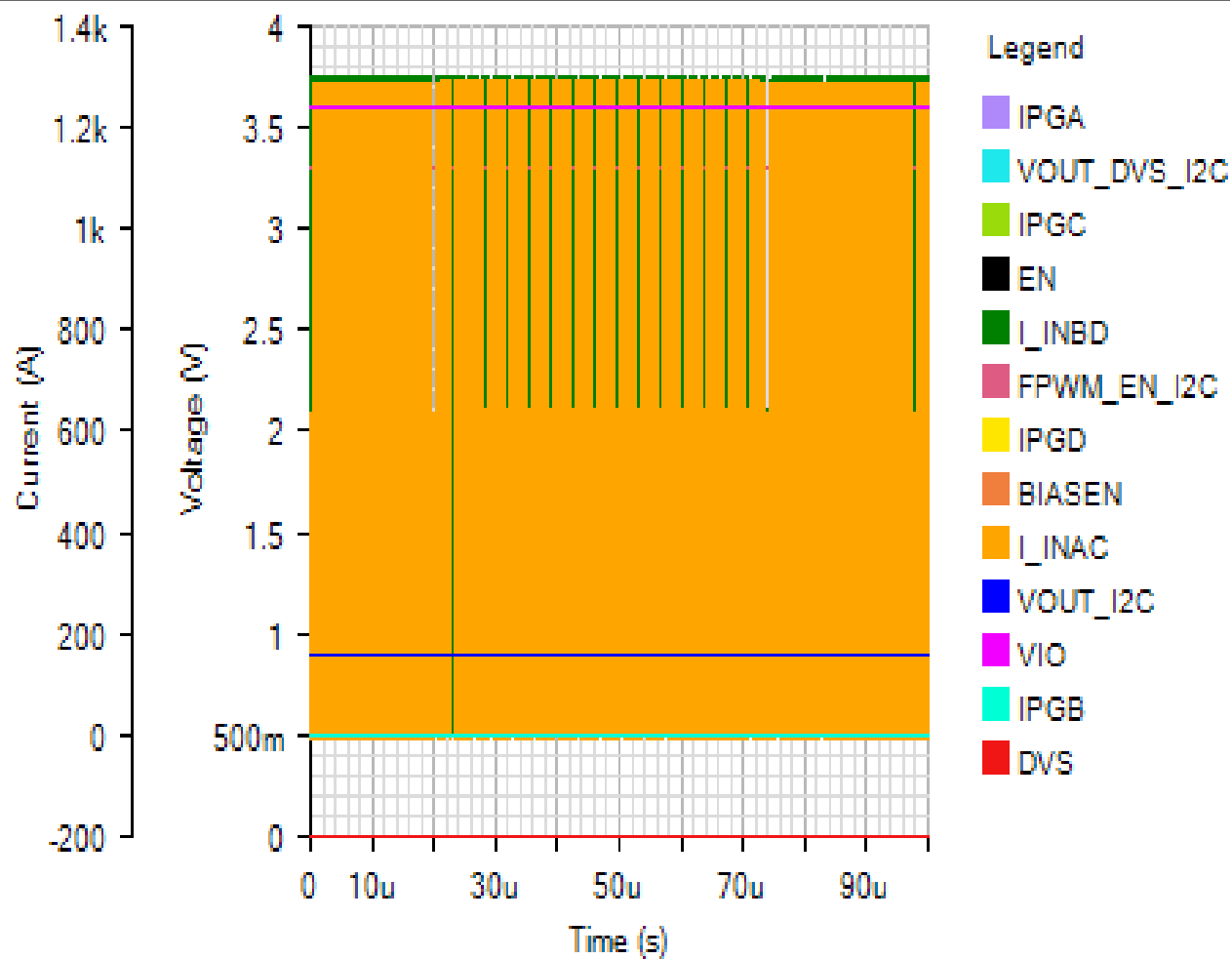
% of total

Component	Loss (W)	% of total
A	0.772729	27.7
B	0.132	4.7
E	0.983965	35.3
F	0.0036	0.1
C2	0.37091	13.3
C1	0.015923	0.6
D2	0.502274	18
D1	0.00485	0.2
Total	2.786252	100

Load Step - Sun Nov 18 2018 17:19:56

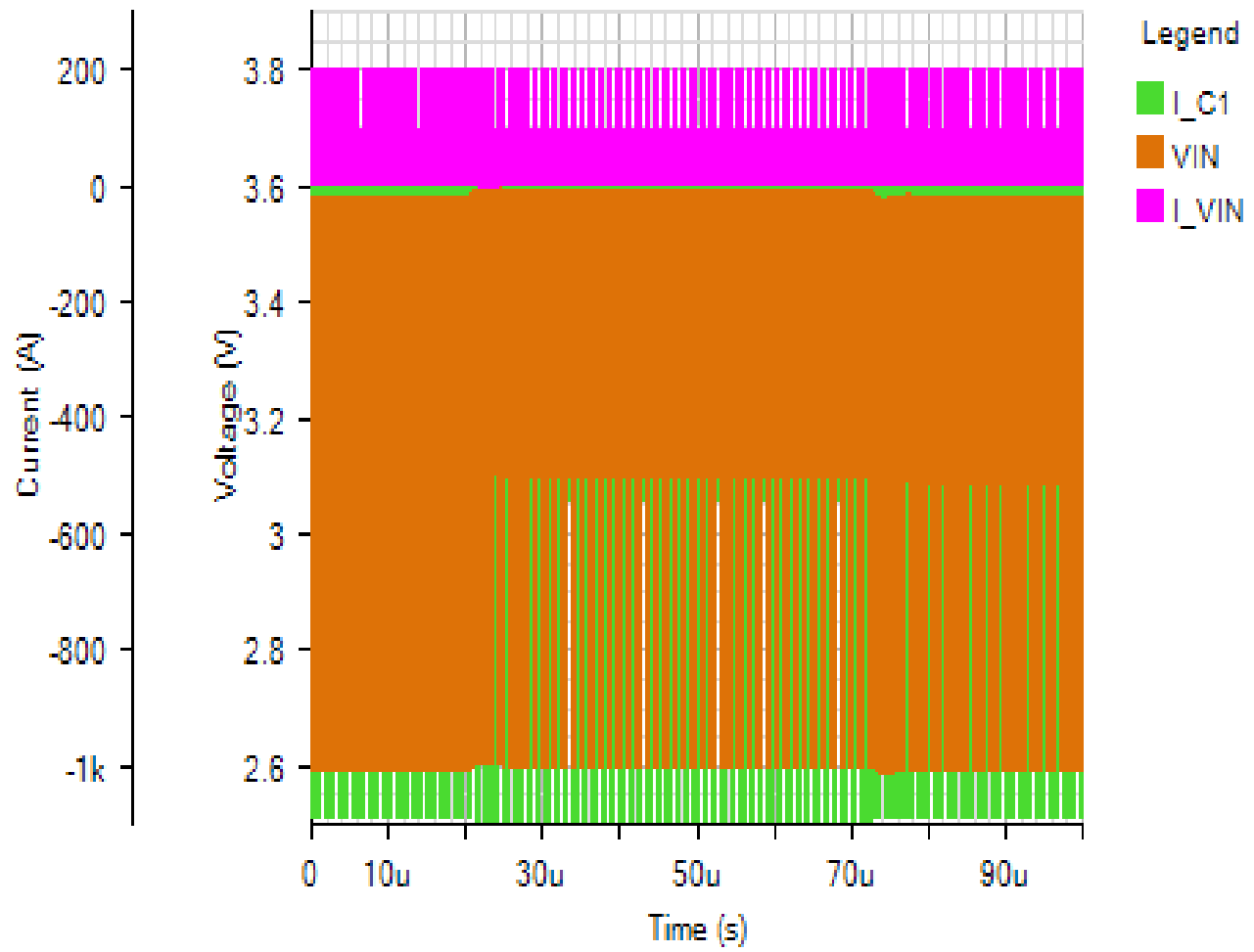
IC

Default



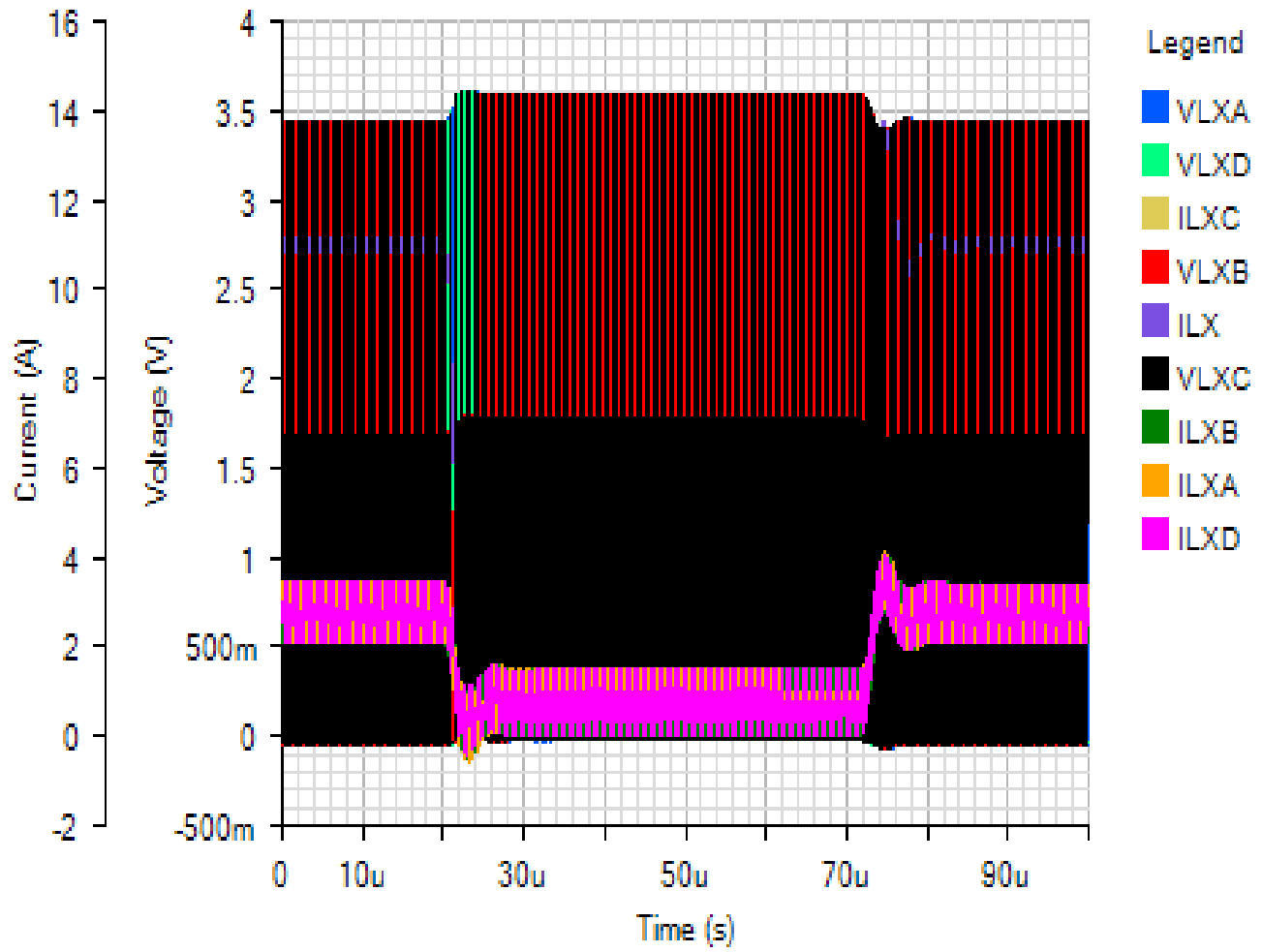
INPUT

Default



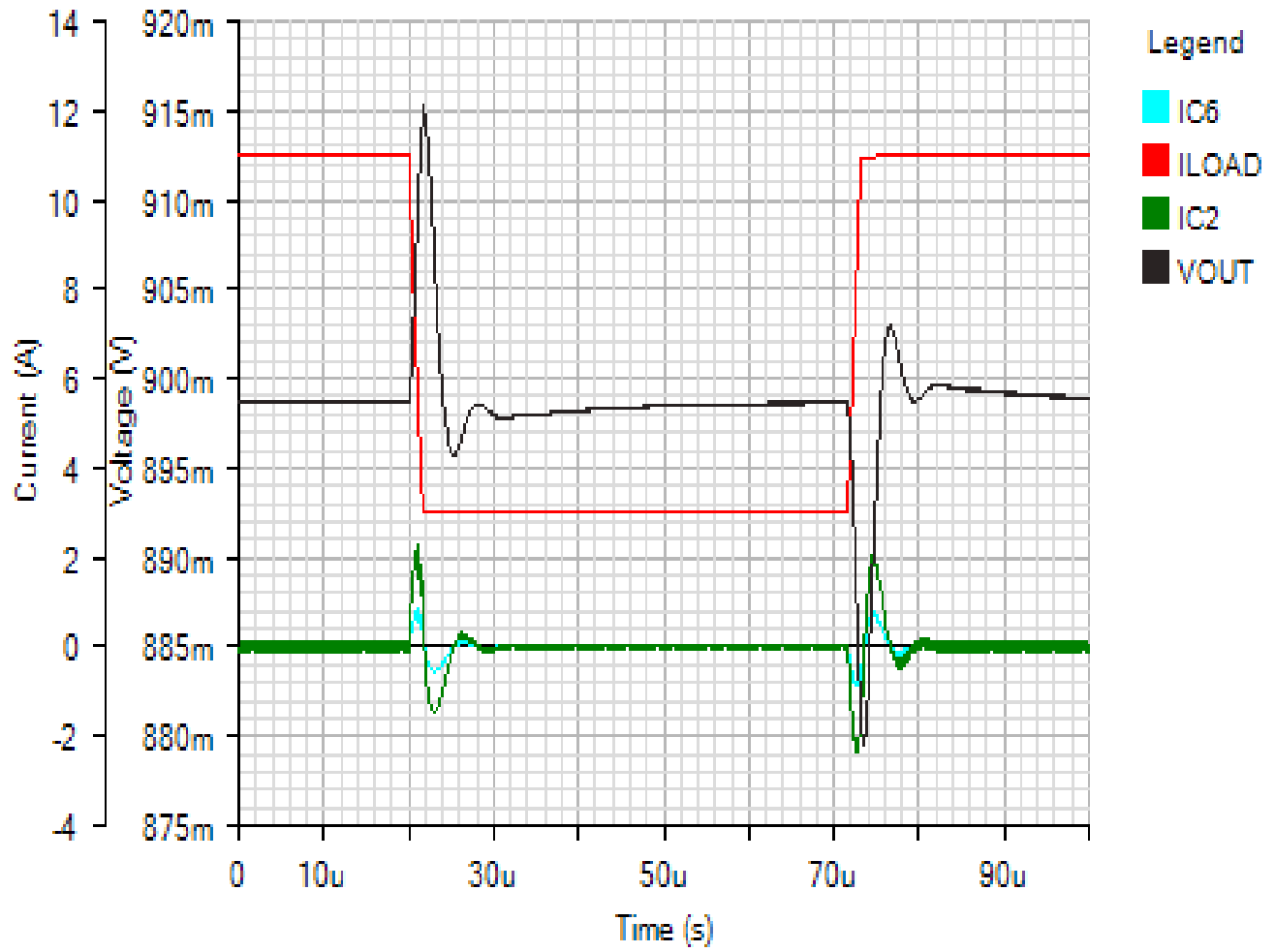
SWITCHING

Default



OUTPUT

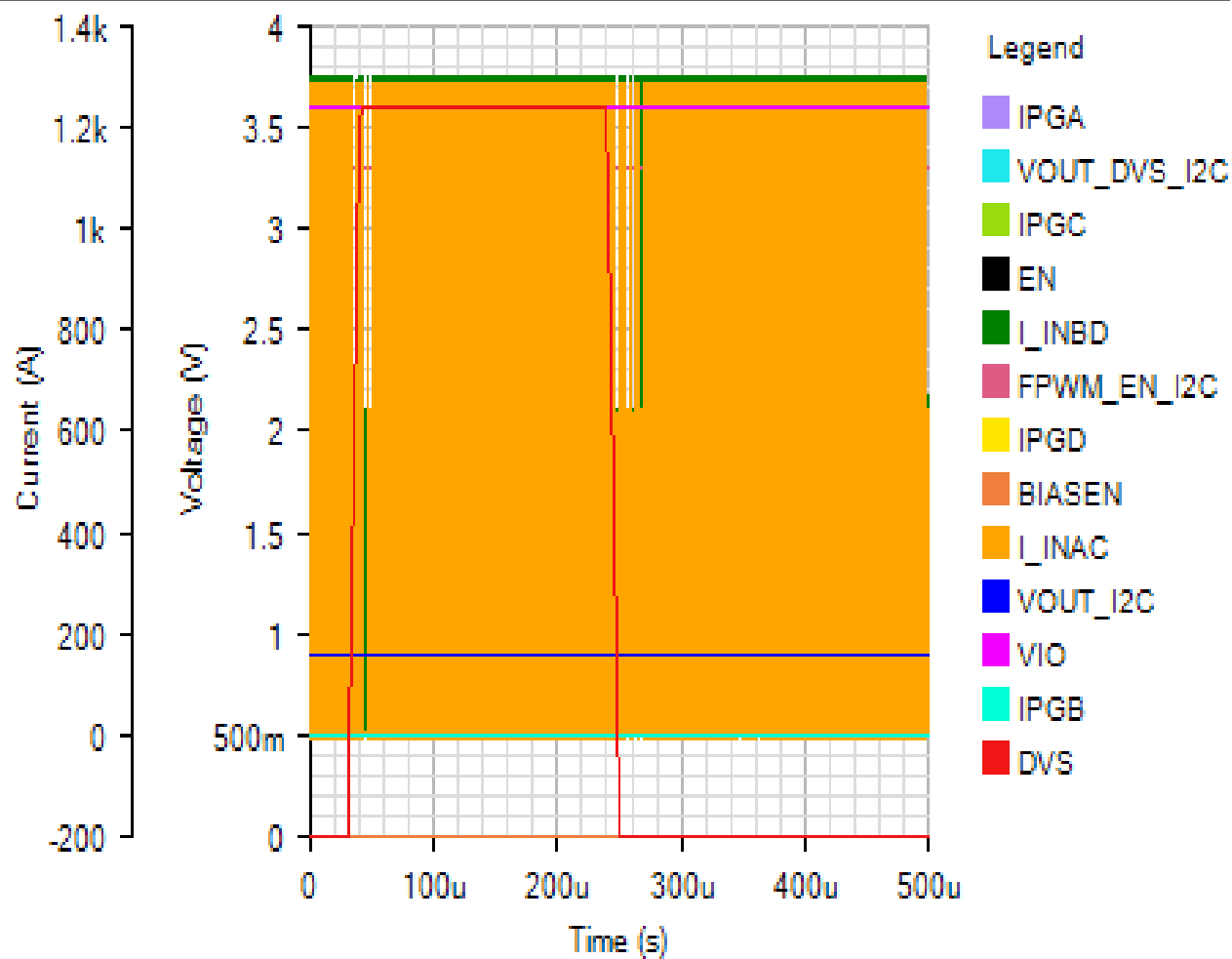
Default



Output Voltage Change - Sun Nov 18 2018 17:19:56

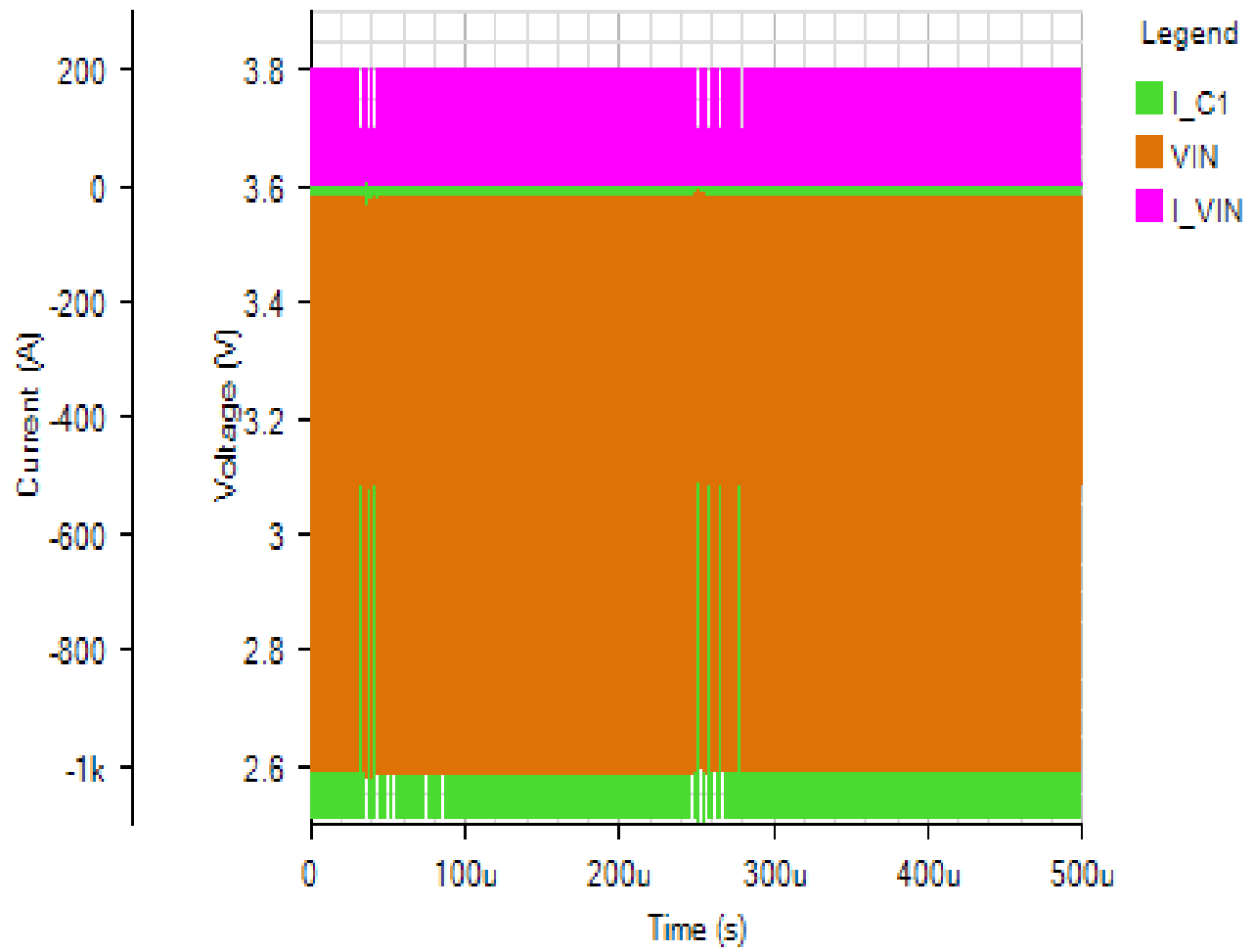
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Default



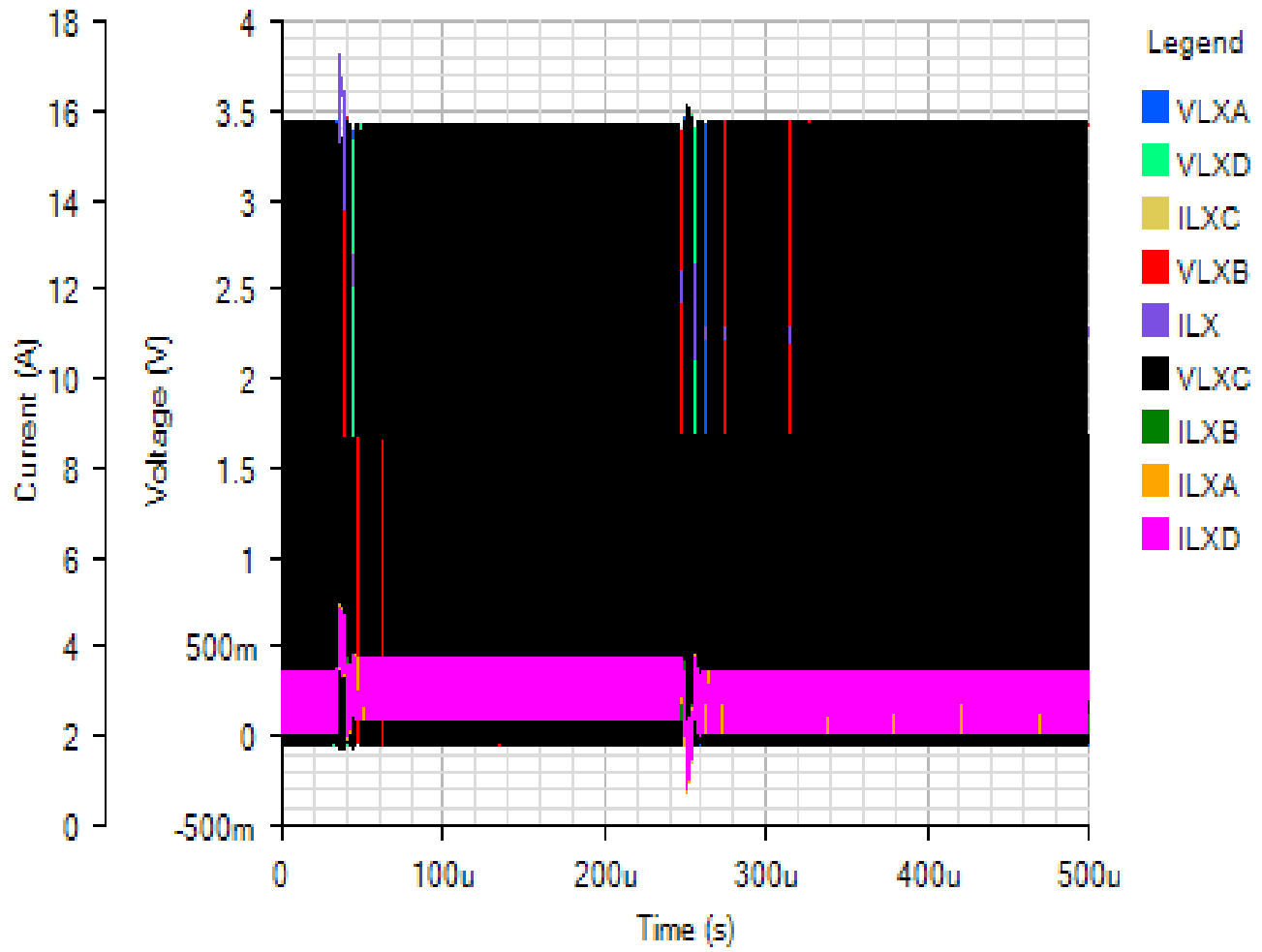
INPUT

Default



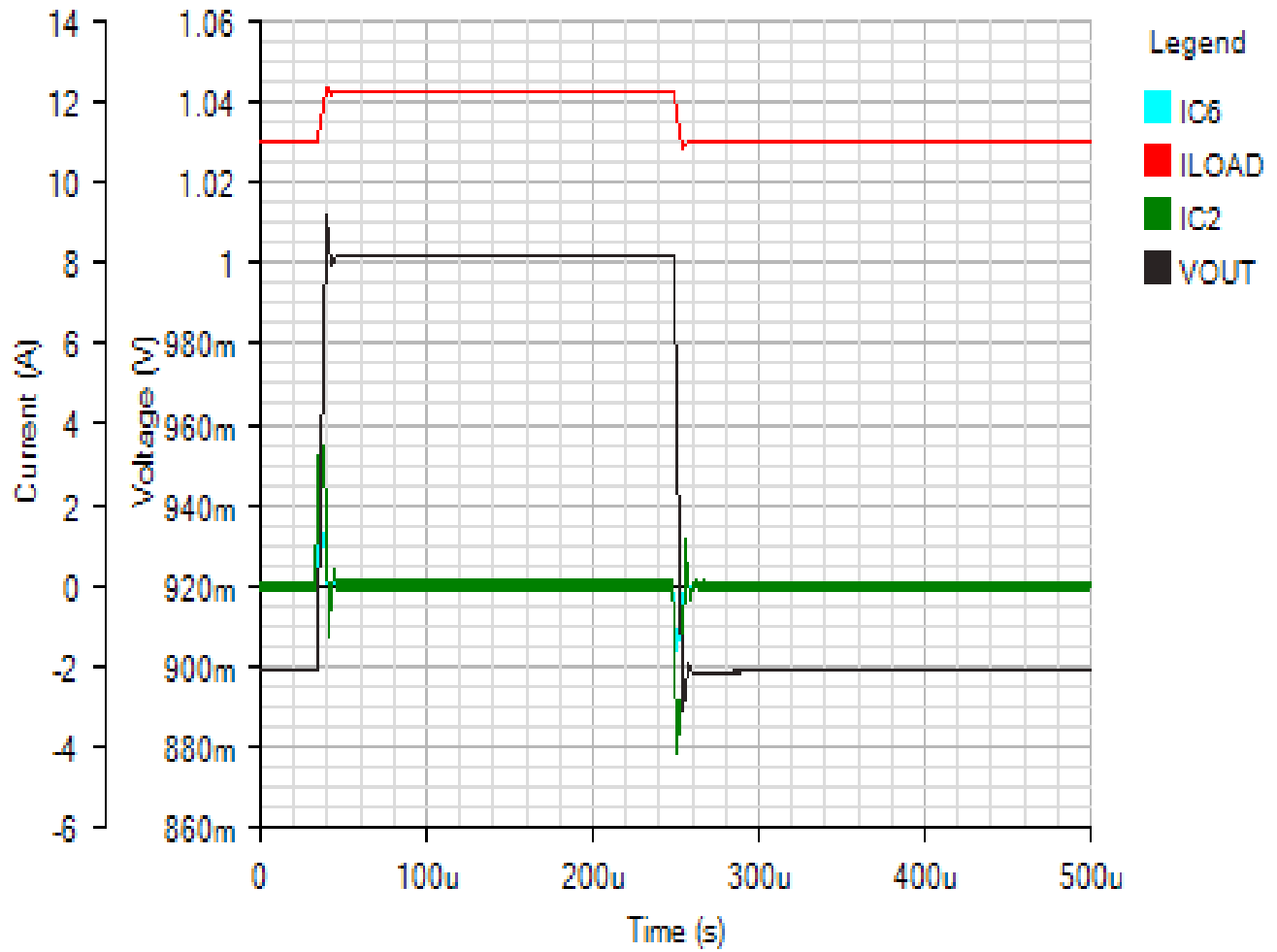
SWITCHING

Default
















OUTPUT

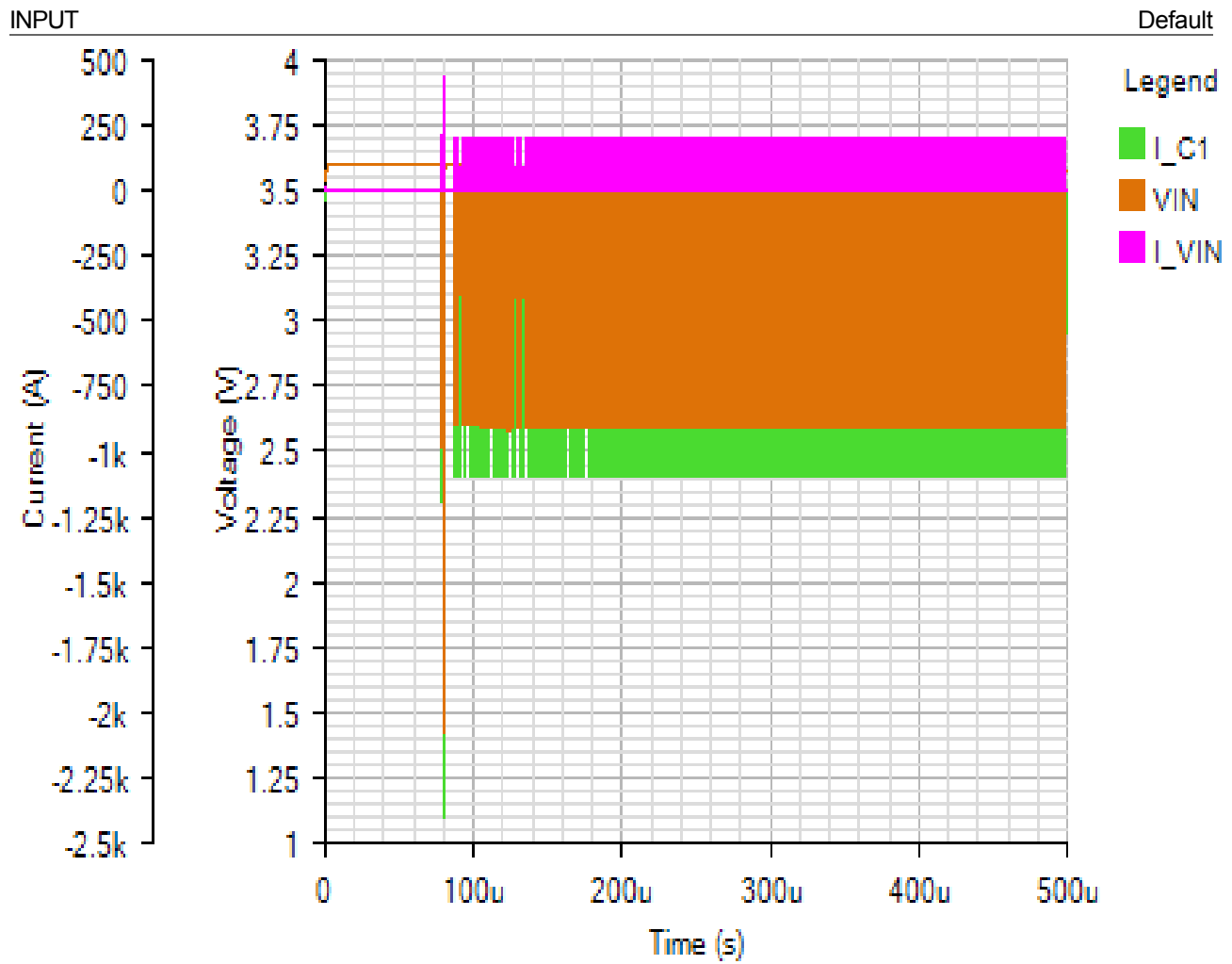
Default



IC

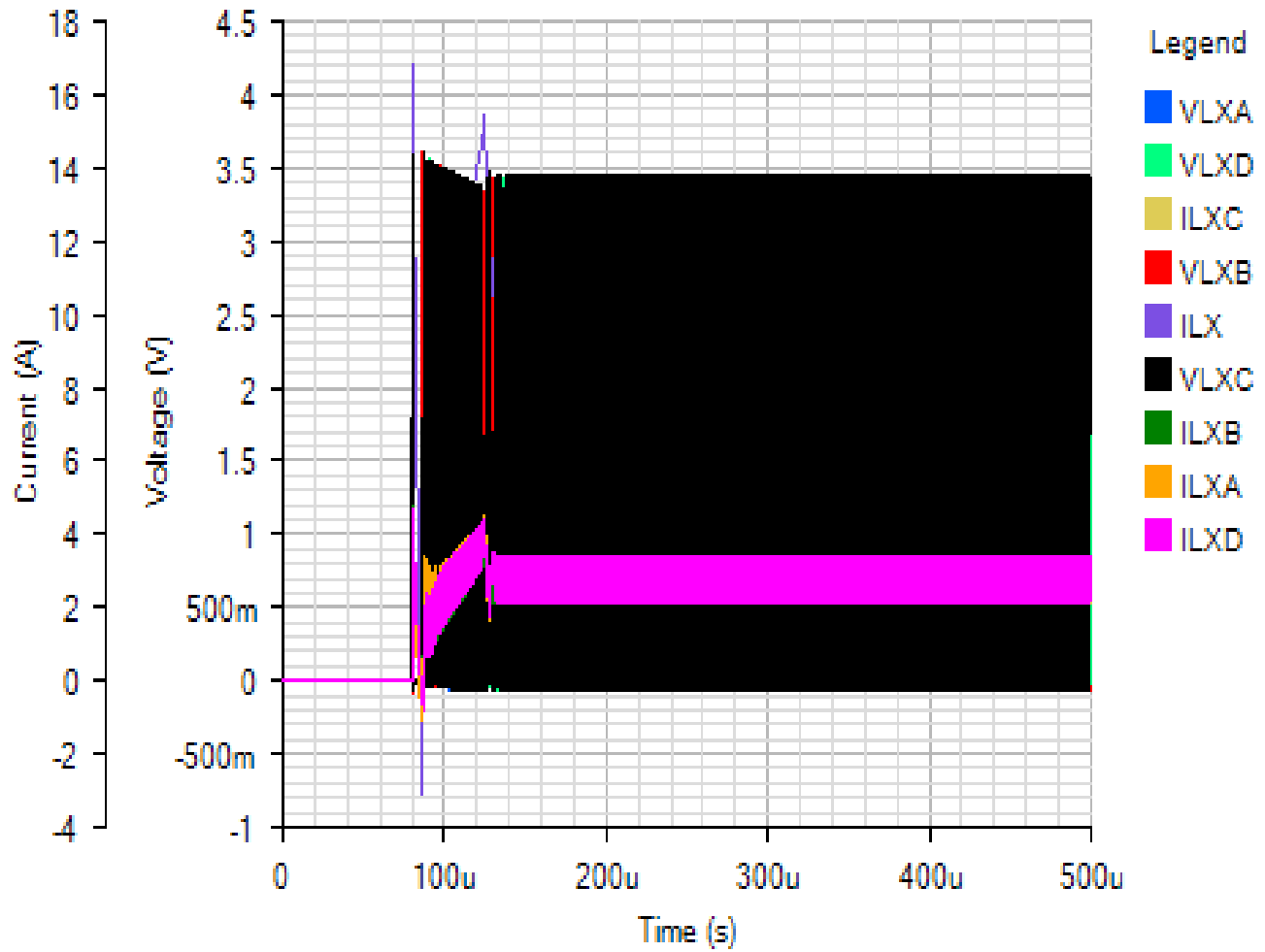
The timing diagram displays two waveforms over a 500 ns period. The left y-axis represents Current (A) from -200 to 1.6k, and the right y-axis represents Voltage (V) from -500m to 4. The x-axis is Time (s) from 0 to 500u. A red trace shows a current pulse peaking at approximately 1.3k A around 100 ns. A green trace shows a voltage pulse peaking at approximately 3.3 V around 100 ns. Both pulses are followed by a sharp drop to zero. Horizontal reference lines are present at 1 A (red), 0.5 A (blue), 1 V (cyan), 0.5 V (magenta), and 0 V (black).

-  IPGA
-  VOUT_DVS_I2C
-  IPGC
-  EN
-  I_INBD
-  FPWM_EN_I2C
-  IPGD
-  BIASEN
-  I_INAC
-  VOUT_I2C
-  VIO
-  IPGB
-  DVS



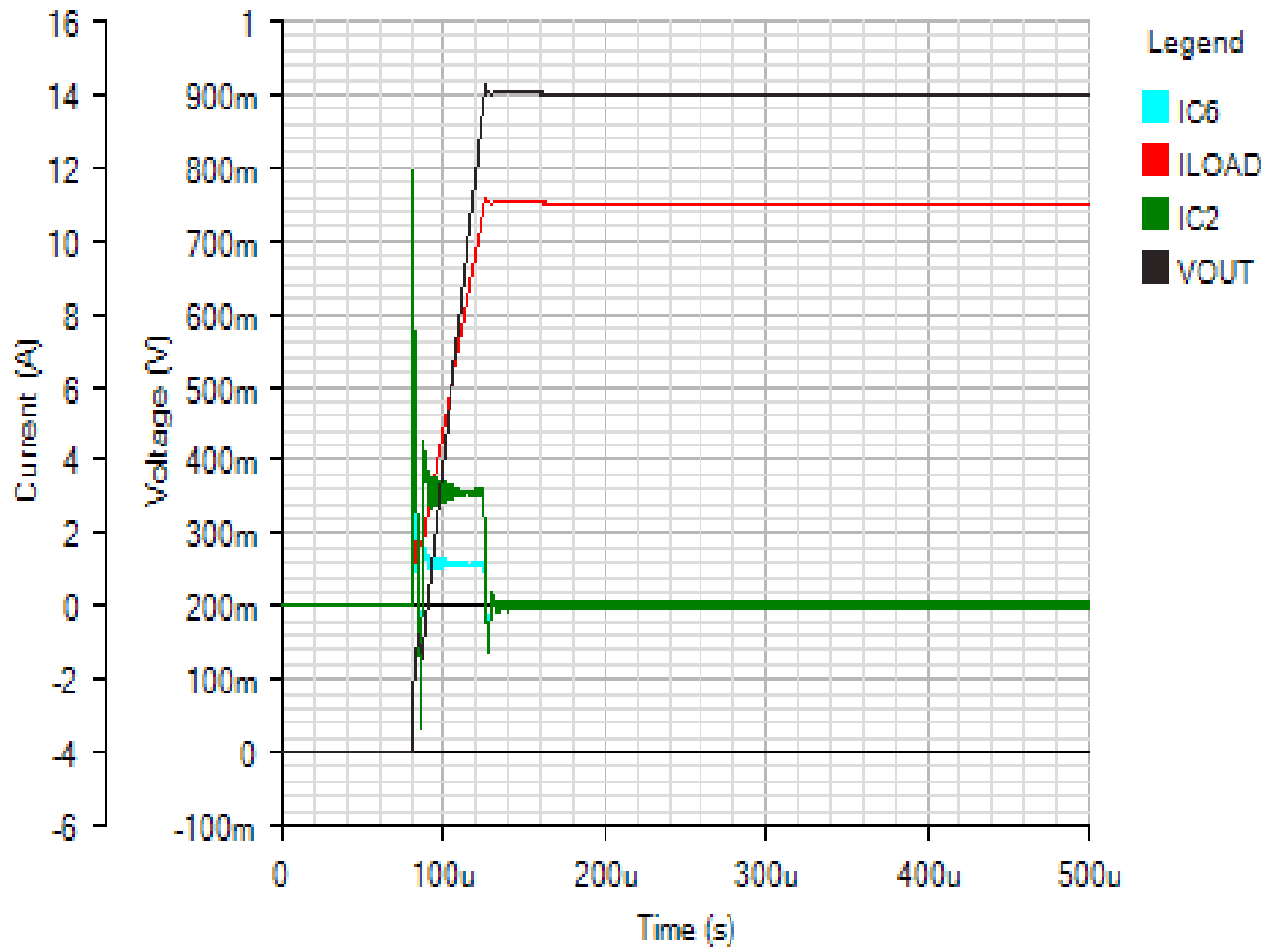
SWITCHING

Default



OUTPUT

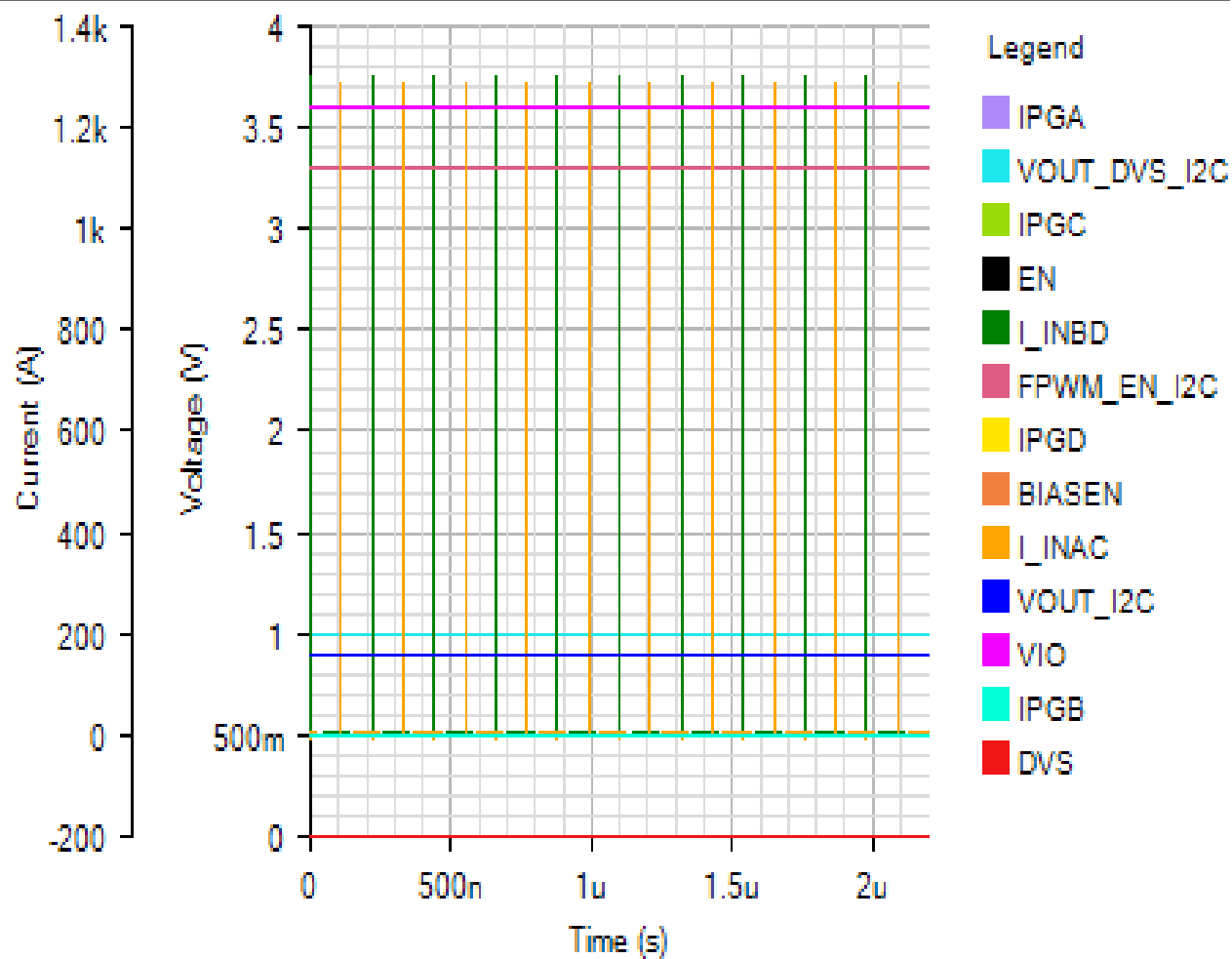
Default



Steady State - Sun Nov 18 2018 17:19:56

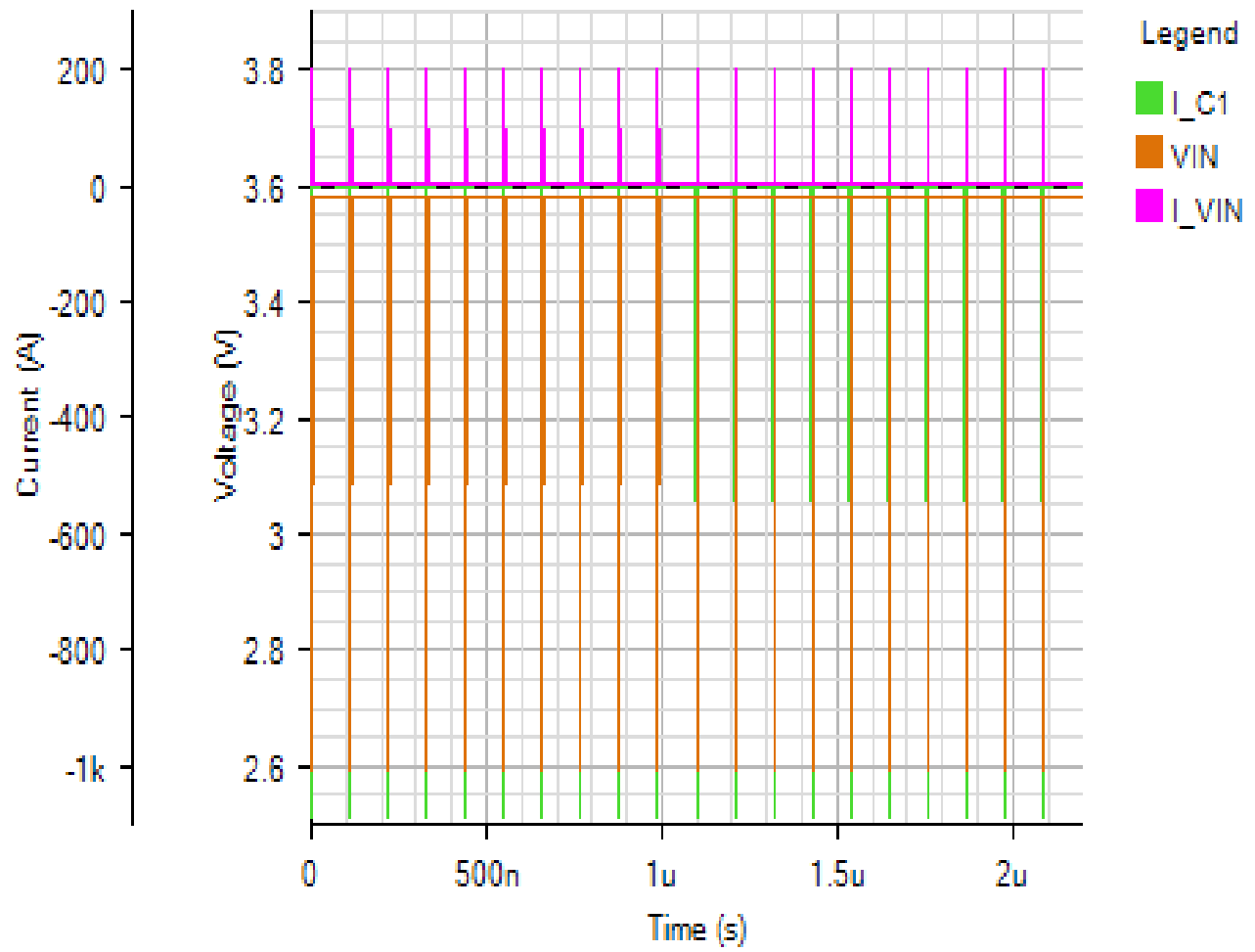
IC

Default



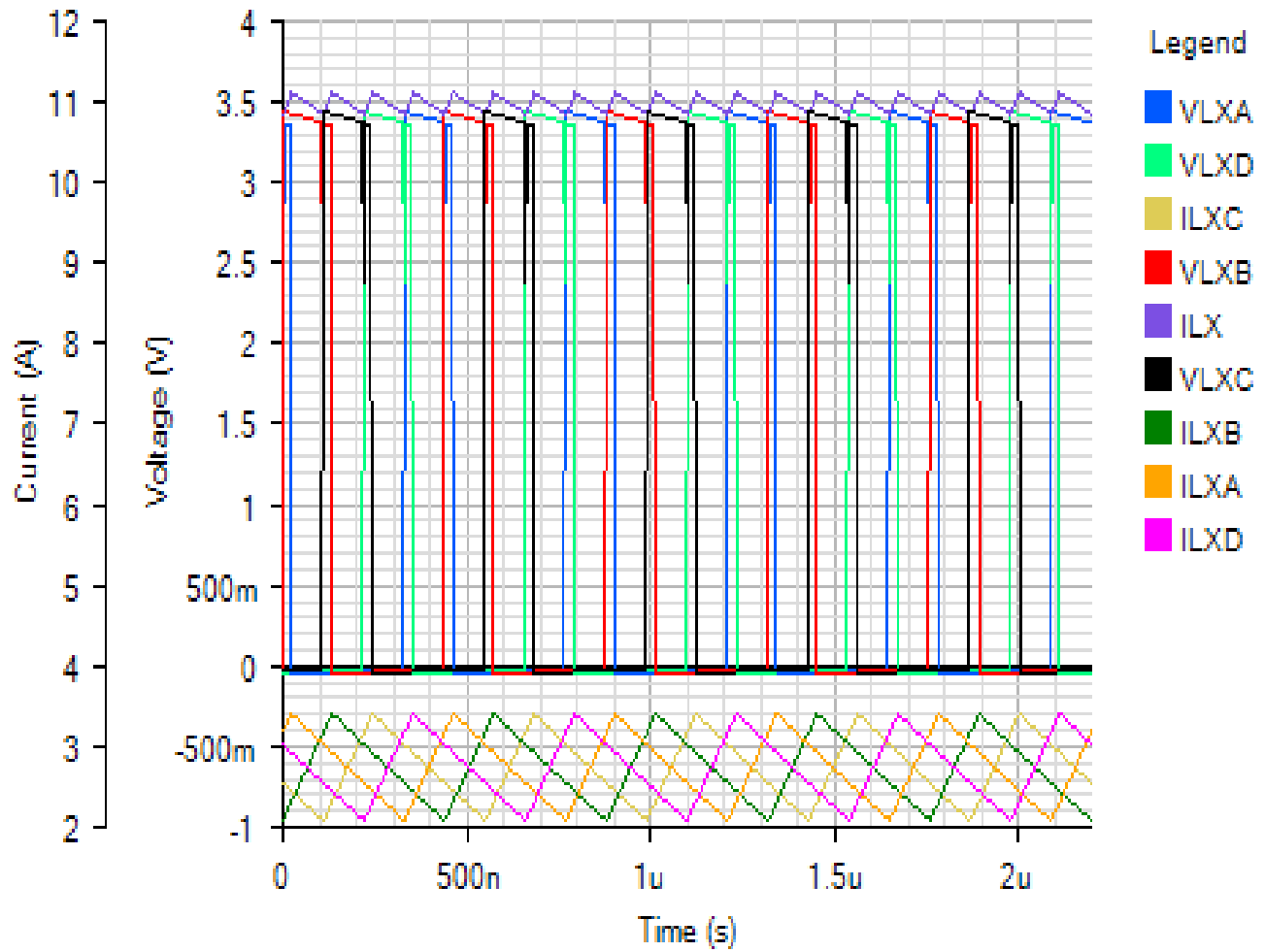
INPUT

Default



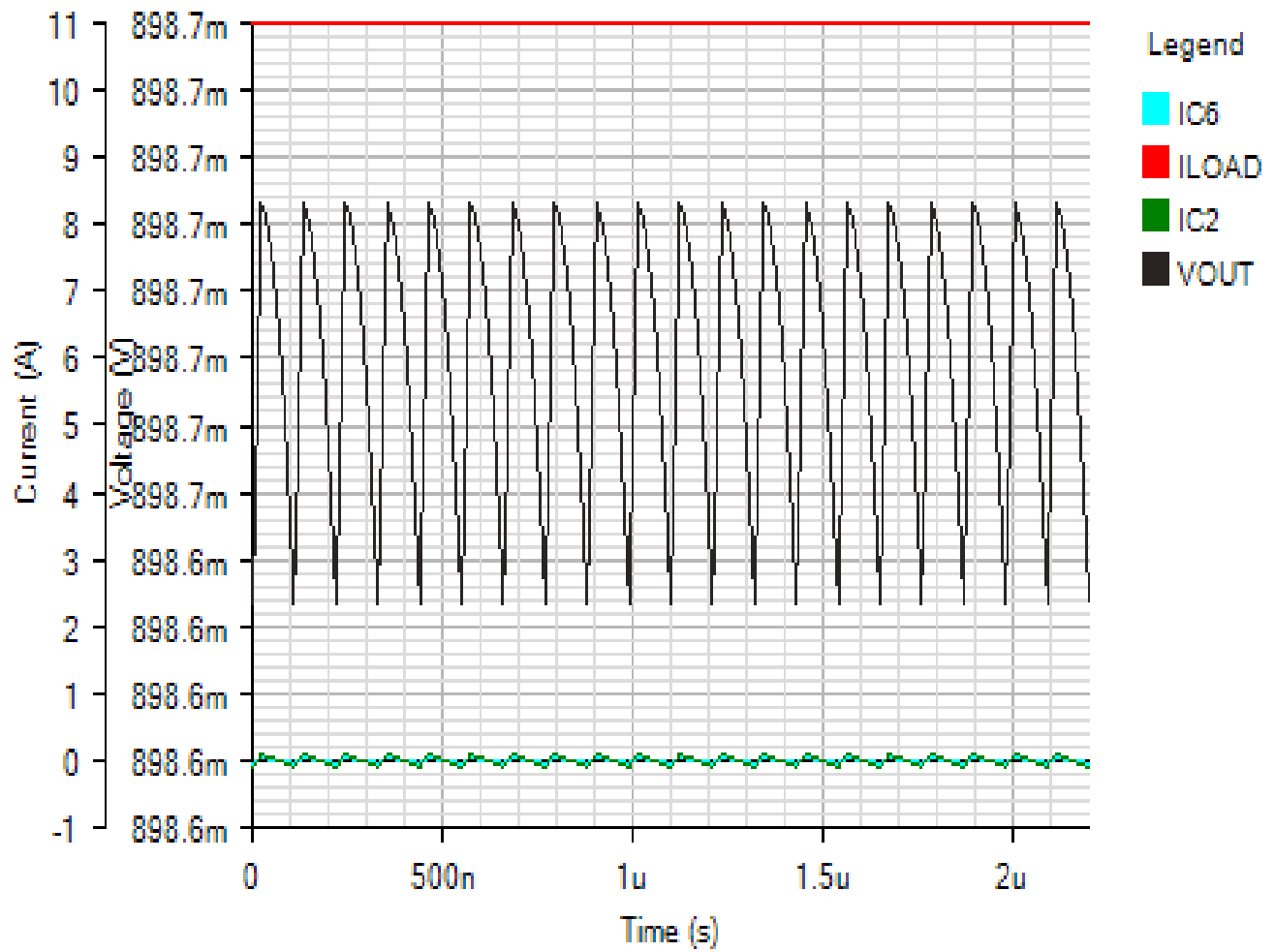
SWITCHING

Default



OUTPUT

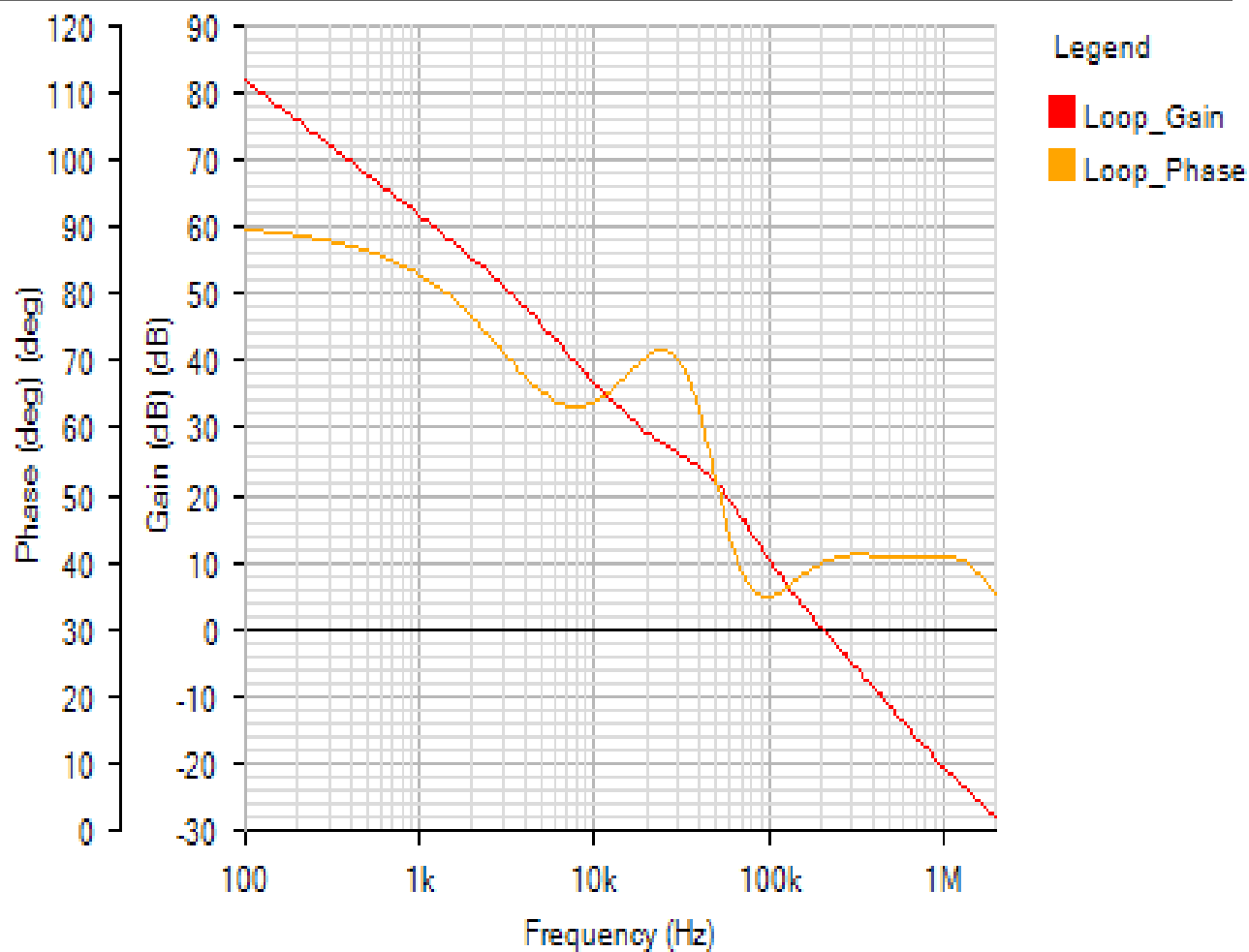
Default



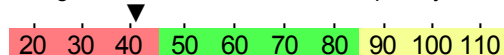
AC Loop - Sun Nov 18 2018 17:19:56

BODE

Default



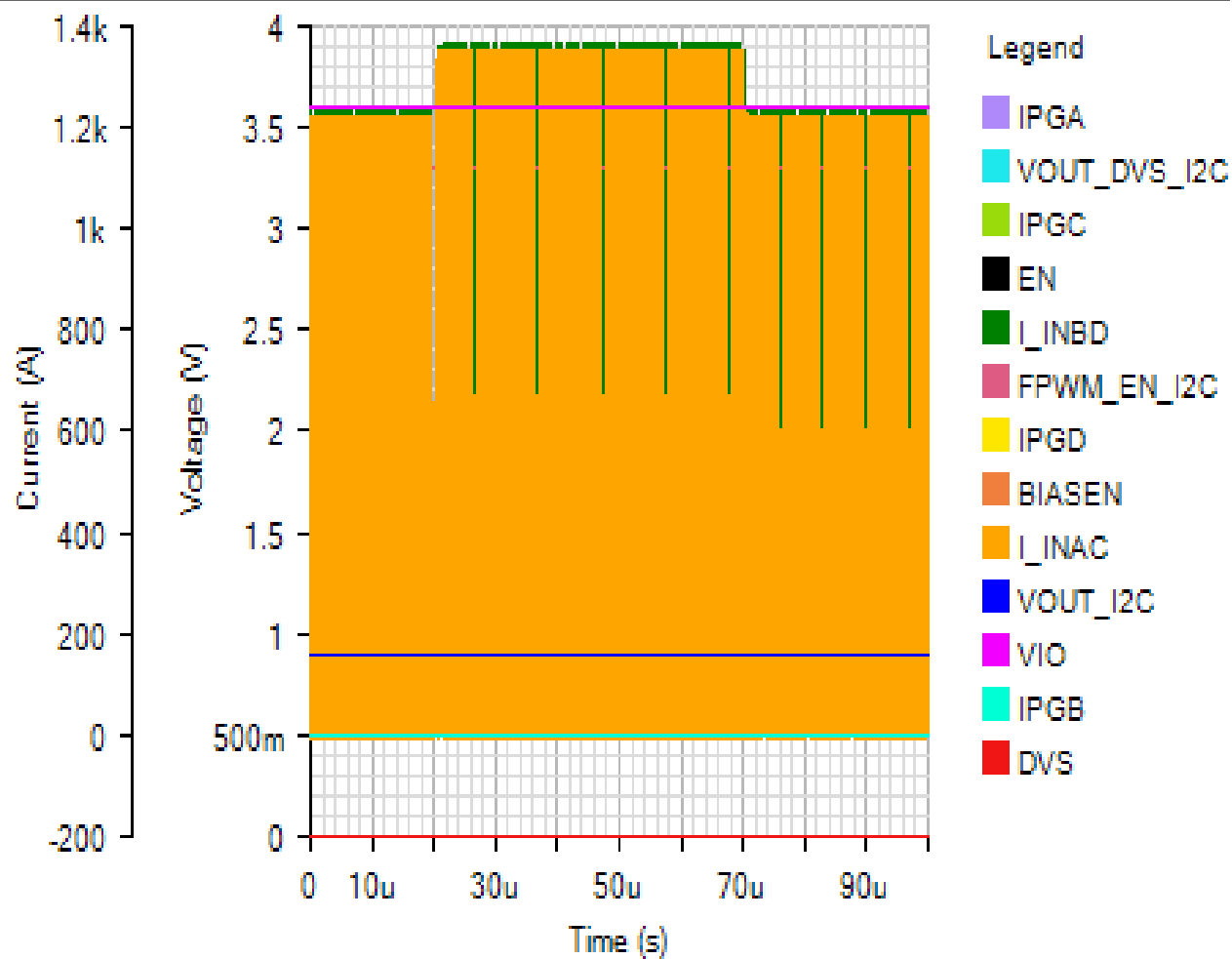
Phase Margin: 40.04° at a crossover frequency of 206.3kHz

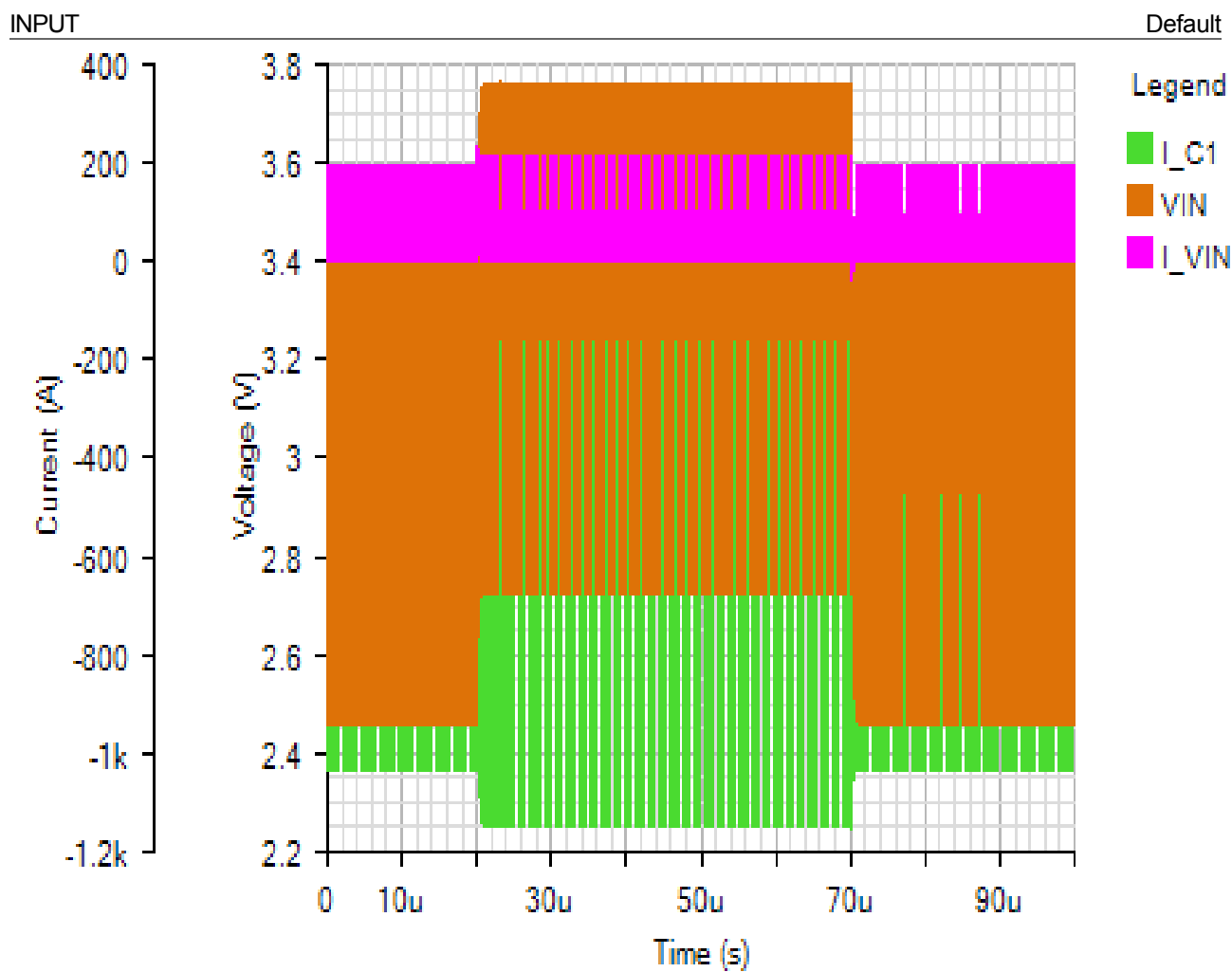


Line Transient - Sun Nov 18 2018 17:19:56

IC

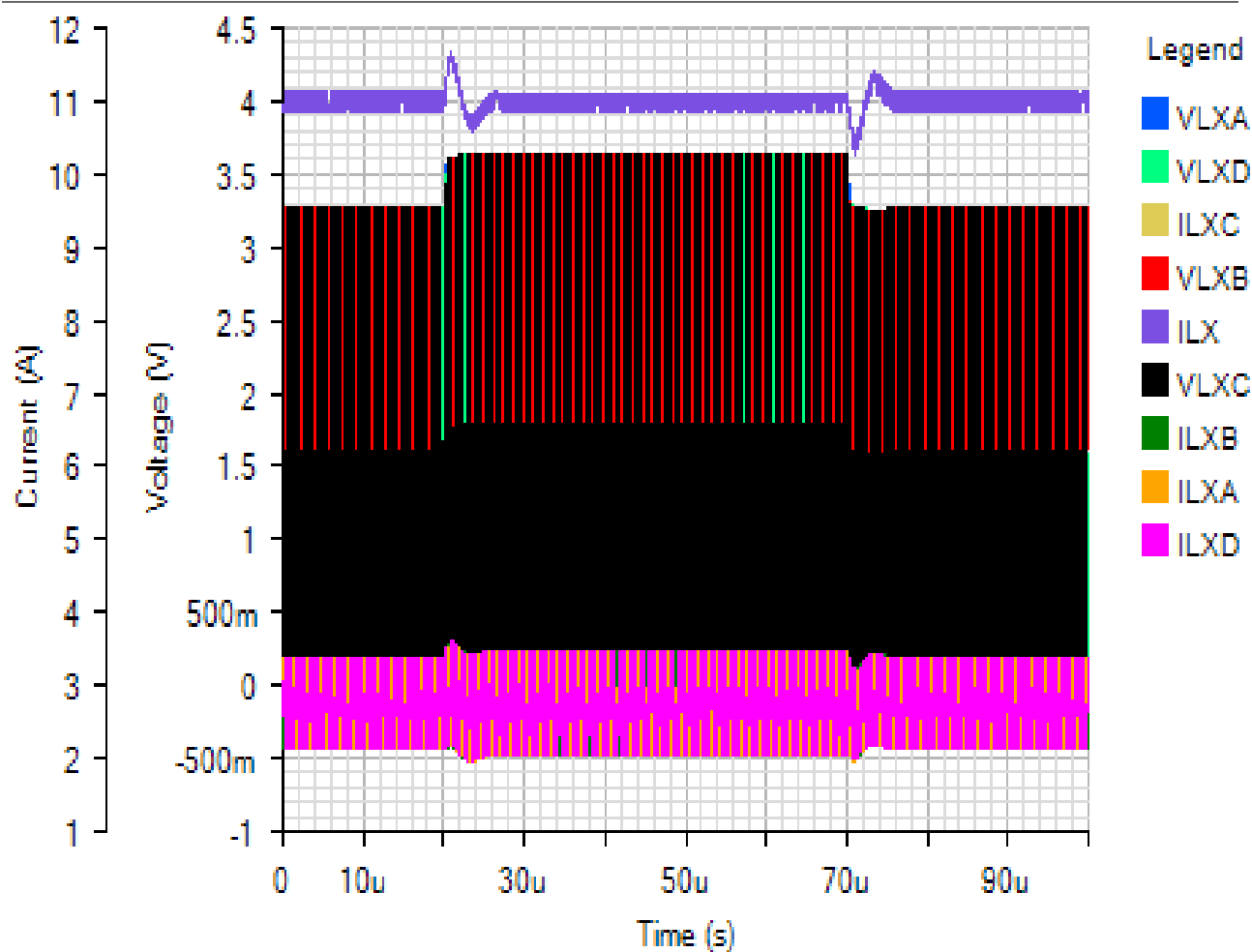
Default





SWITCHING

Default



OUTPUT

Default

