

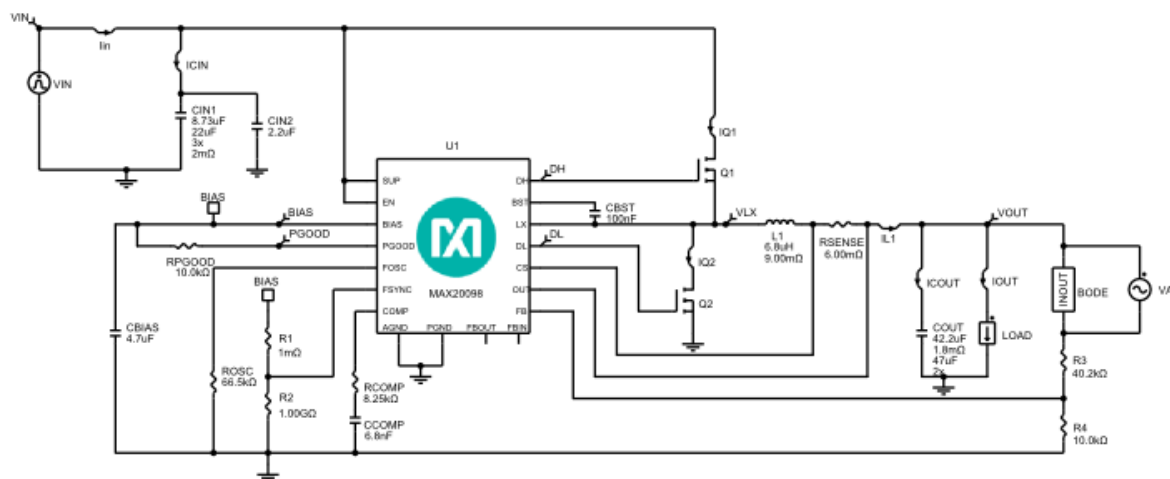
Initial Design

1.0

Design Requirements

Parameter	Value
Minimum Input Voltage	12V
Maximum Input Voltage	16V
Nominal Input Voltage	14V
Input Voltage Ripple	2.5%
Output Configuration	External Resistive Divider
Output Voltage	5V
Output Current	7A
Enable Forced Switchover ?	Yes
Output Voltage Ripple	1%
Load Step Current	3.5A
Load Step Start Current	7A
Output Voltage Load Step Over/Undershoot	5%
Load Step Edge Rate	1A/us
Performance Priority	Design for High Efficiency
BOM Priority	Cost
Mode of Operation	Forced-PWM Mode
Switching Frequency	0.4MHz
Ambient Temperature	25°C
Inductor Current Ratio	0.3
Enable High Power Design ?	No

Schematic



MODES OF OPERATION

FPWM Mode - FSYNC pin tied HIGH

SKIP Mode - FSYNC pin tied LOW

For External Clock-Synchronized operation, connect an external pulse source to FSYNC

Note 1 : When Skip mode is selected, AC Loop simulation may fail if the Load Current and/or the Duty Cycle is low enough to engage Skip mode, because Skip mode is hysteretic and there is no AC Loop to measure.

Note 2 : FBOUT and FBIN are fictitious pins that are needed for AC analysis measurements for internal preset configuration. These are not present in the actual IC.

Note 3 : For output voltages between 3.2V and 5.5V with the switcher option OR for input voltages less than 5V, using the default FETs (ON Semi NVMF55C456NL) is strongly recommended. These FETs have been found to yield the best performance under these conditions. To choose alternate FETs in the EE-Sim online design tool, click on the Help button for guidance.

BOM

Ref	Qty	Part Number	Manufacturer	Description
U1	1	MAX20098	User-Defined	IC
CBIAS	1	CL31B475KOHNNNE	Samsung Electro-Mechanics	Cap Ceramic 4.7uF 16V X7R 10% Pad SMD 1206 125°C T/R
CBST	1	CC0402KRX7R8BB104	Yageo	Cap Ceramic 0.1uF 25V X7R 10% Pad SMD 0402 125°C T/R
CCOMP	1	04023C682KAT2A	AVX	Cap Ceramic 0.0068uF 25V X7R 10% Pad SMD 0402 125°C T/R
CIN1	3	GRM32ER71E226ME15	Murata	Cap Ceramic 22uF 25V 1210 125C
CIN2	1	C3216X7S2A225K160AB	TDK	Cap Ceramic 2.2uF 100V X7S 10% Pad SMD 1206 125°C T/R
COUT	2	C1210C476K8R2C	Kemet	Cap Ceramic 47uF 10V 1210 125C
L1	1	DO5040H-682MLB	Coilcraft	Inductor 6.8uH 20% 8.1mOhm 23A Isat 9.6A Irms
Q1	1	NVMF55C456NL	ON Semiconductor	Trans MOSFET N-CH 40VDS 6mOhm@4.5V 5.4mOhm@6V 8.2nC 4nC 1.6nF 0.59nF 175°C 87A 55W 2.7°C/W 1.75mm 36mm^2 SO-8FL Trans MOSFET N-CH 40VDS

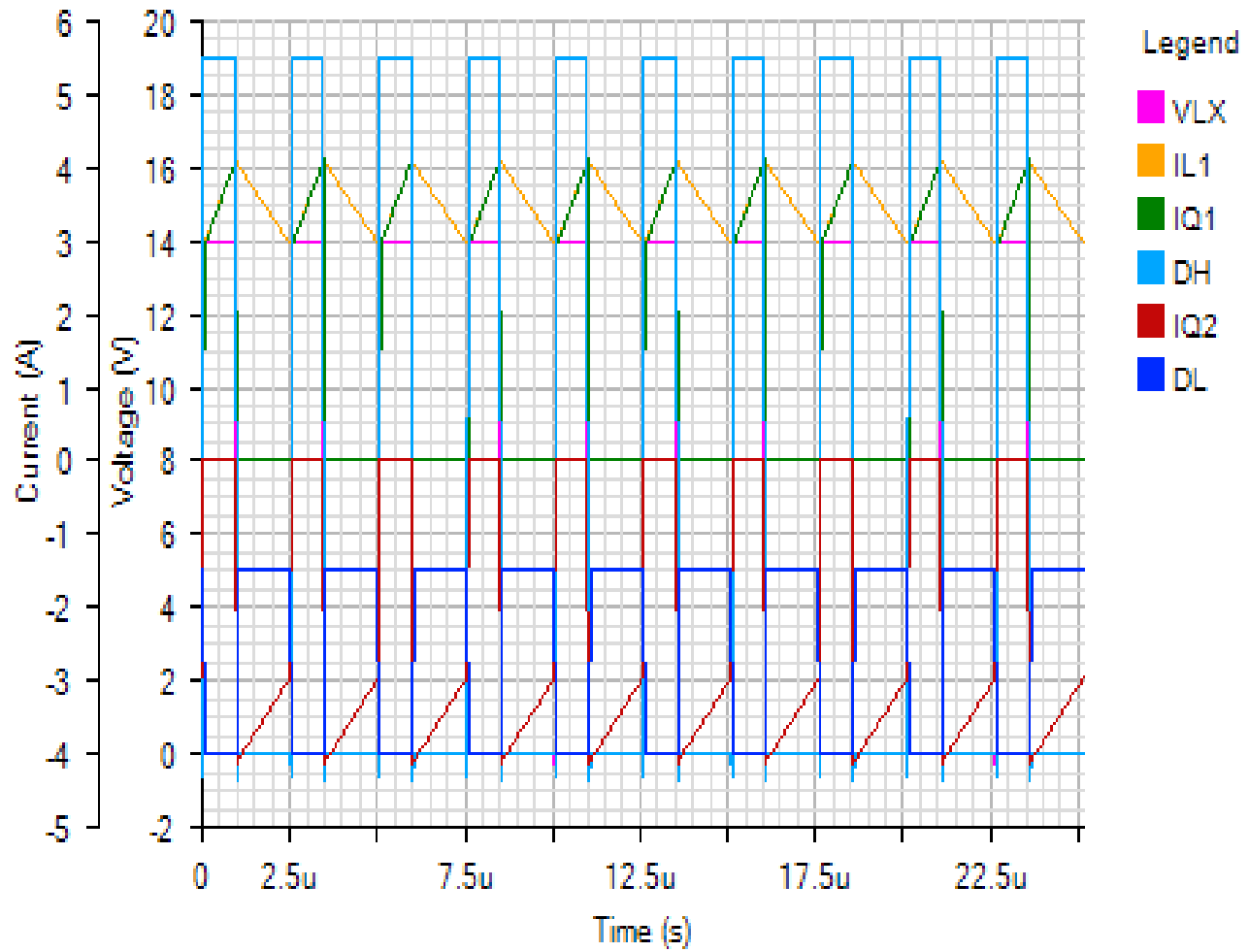
Q2	1	NVMFS5C456NL	ON Semiconductor	6mOhm@4.5V 5.4mOhm@6V 8.2nC 4nC 1.6nF 0.59nF 175°C 87A 55W 2.7°C/W 1.75mm 36mm^2 SO-8FL
R3	1	ERJ3EKF4022V	Panasonic	Res Thick Film 0603 40.2K Ohm 1% 0.1W(1/10W) ±100ppm/°C Pad SMD Automotive T/R
R4	1	ERJ2RKF1002X	Panasonic	Res Thick Film 0402 10K Ohm 1% 0.1W(1/10W) ±100ppm/°C Pad SMD Automotive T/R
RCOMP	1	ERJ2RKF8251X	Panasonic	Res Thick Film 0402 8.25K Ohm 1% 0.1W(1/10W) ±100ppm/°C Pad SMD Automotive T/R
ROSC	1	ERJ2RKF6652X	Panasonic	Res Thick Film 0402 66.5K Ohm 1% 0.1W(1/10W) ±100ppm/°C Pad SMD Automotive T/R
RPGOOD	1	ERJ2RKF1002X	Panasonic	Res Thick Film 0402 10K Ohm 1% 0.1W(1/10W) ±100ppm/°C Pad SMD Automotive T/R
RSENSE	1	WSL12066L000FEA18	Vishay	Res Metal Strip 1206 0.006 Ohm 1% 0.5W(1/2W) ±110ppm/°C Sulfur Resistant Pad SMD Automotive T/R

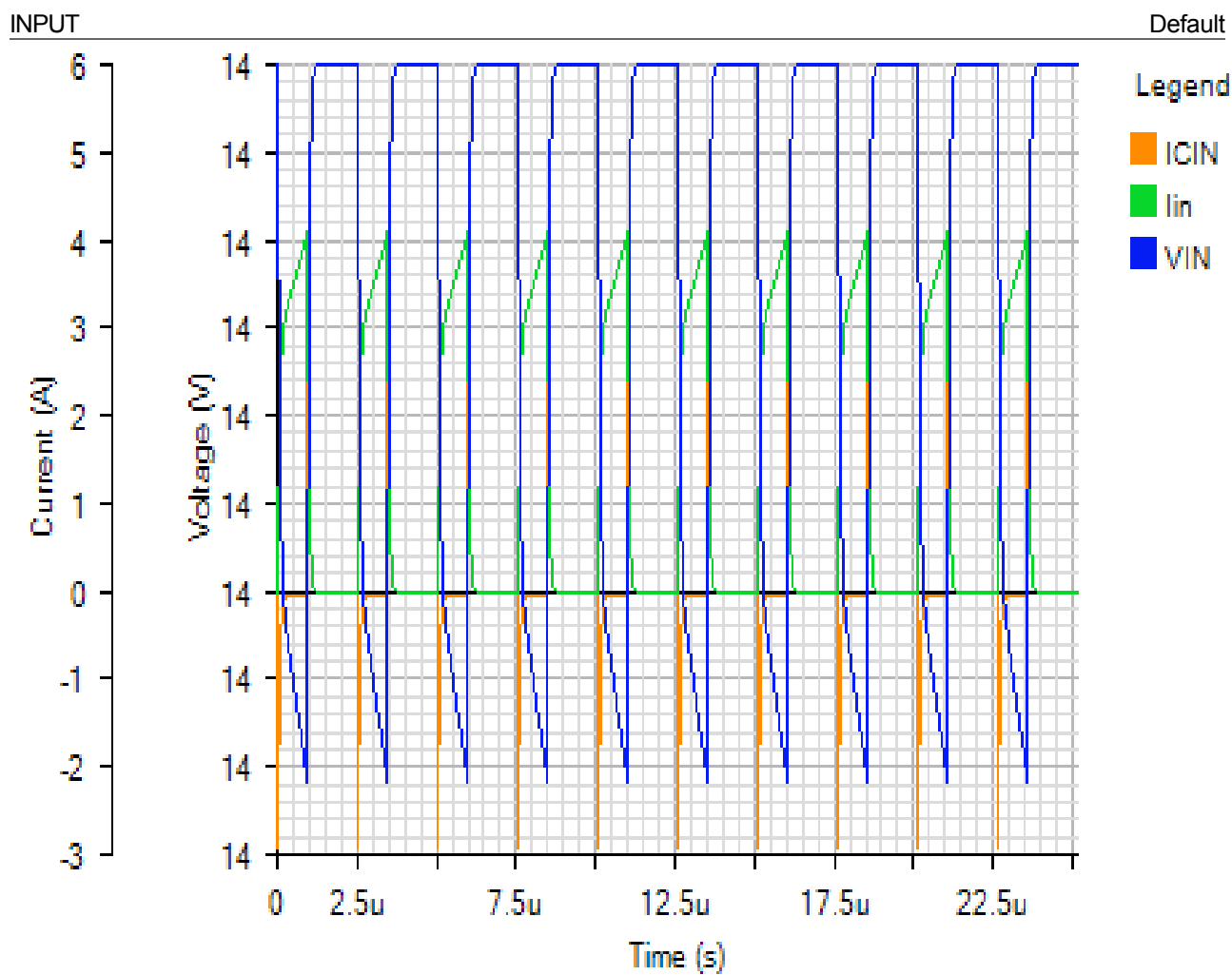
Simulation Results

Steady State - Tue Nov 20 2018 13:30:44

SWITCHING

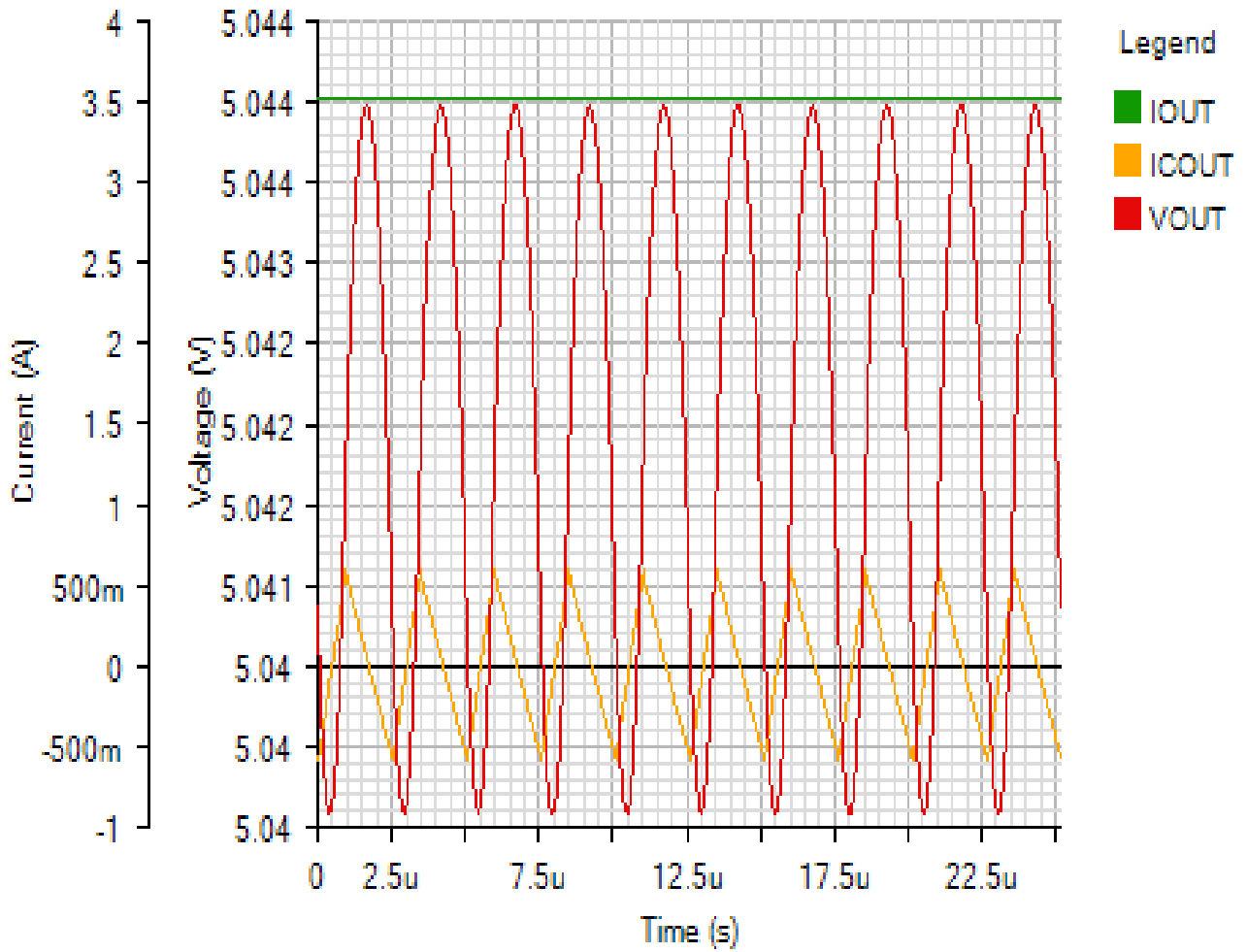
Default

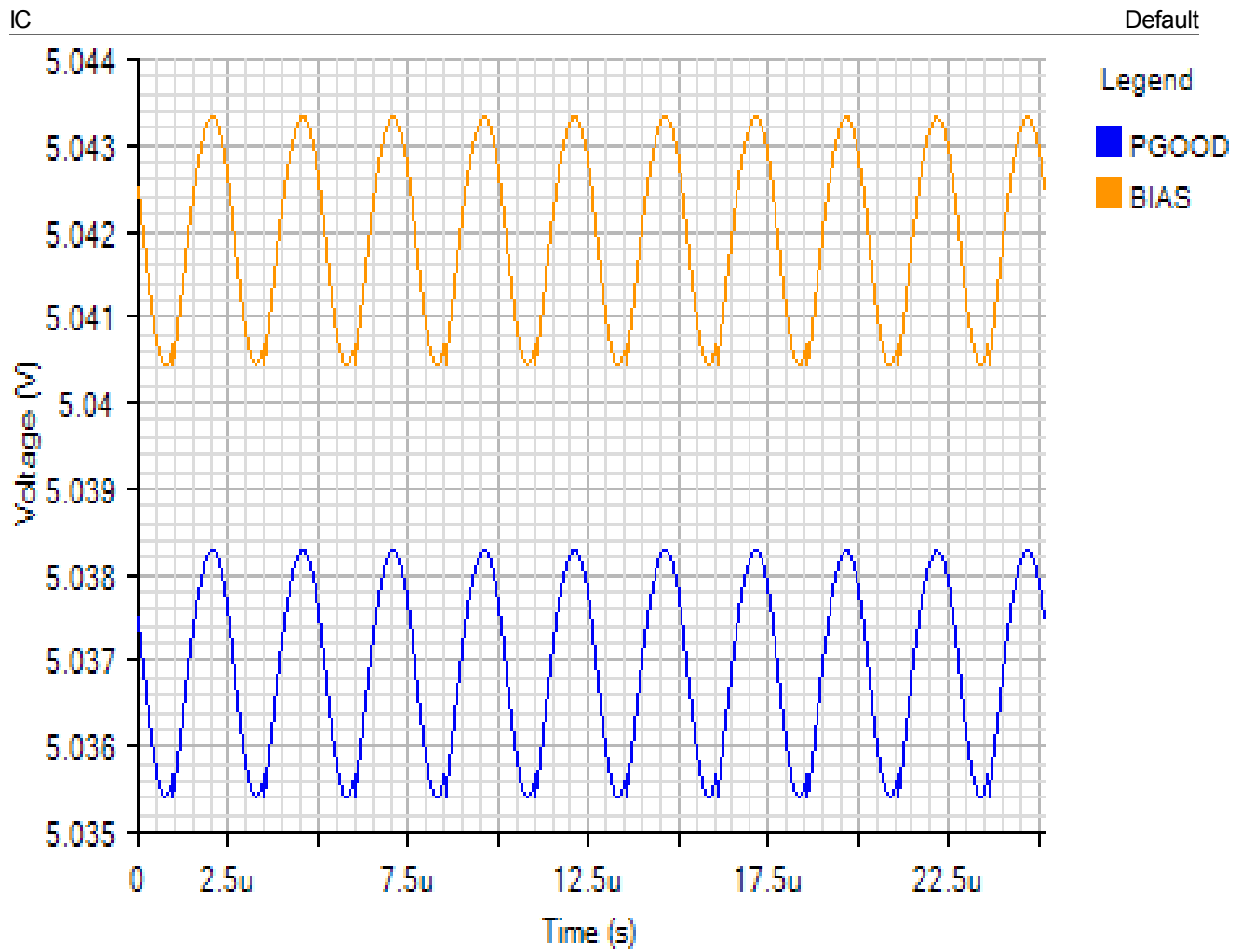




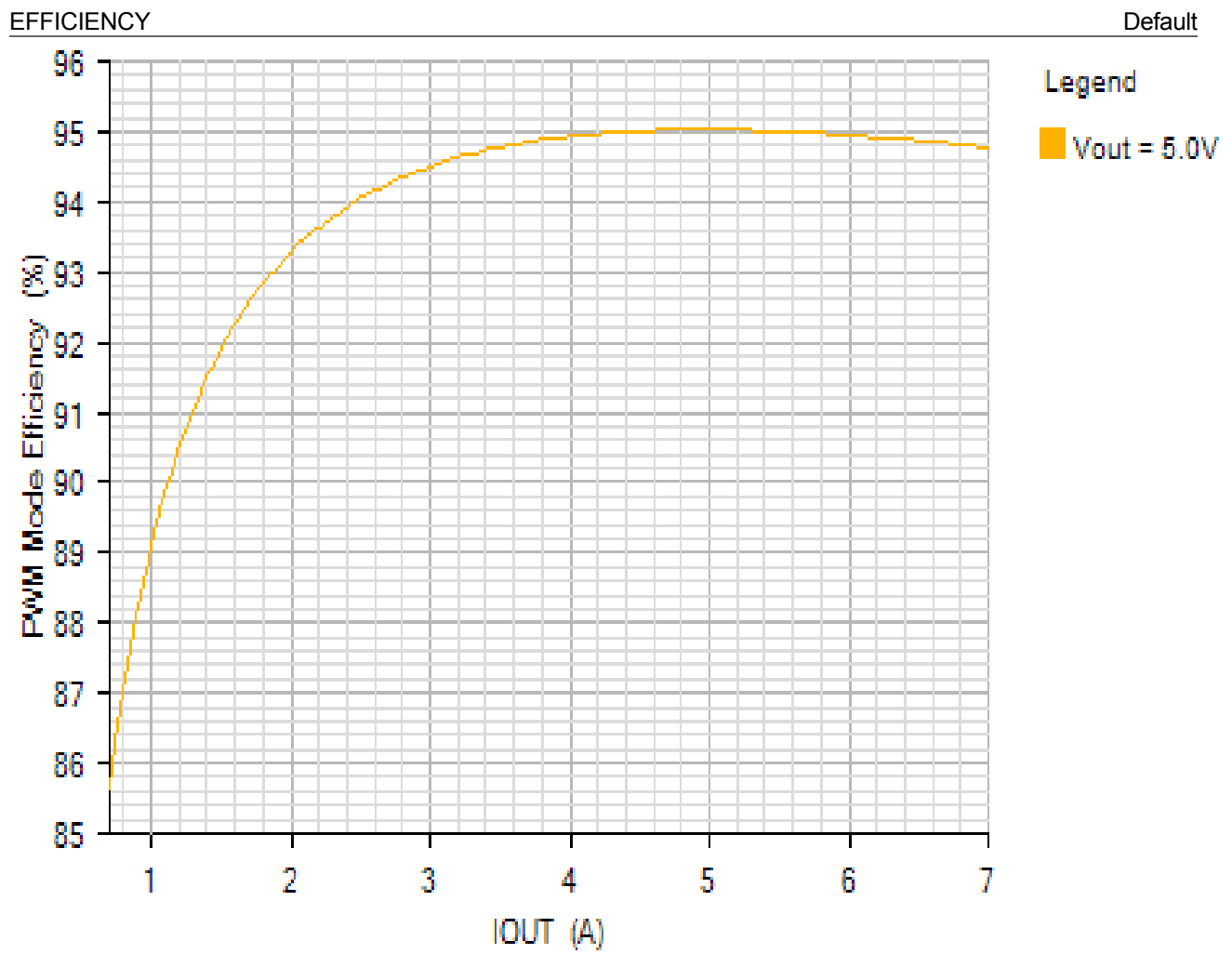
OUTPUT

Default



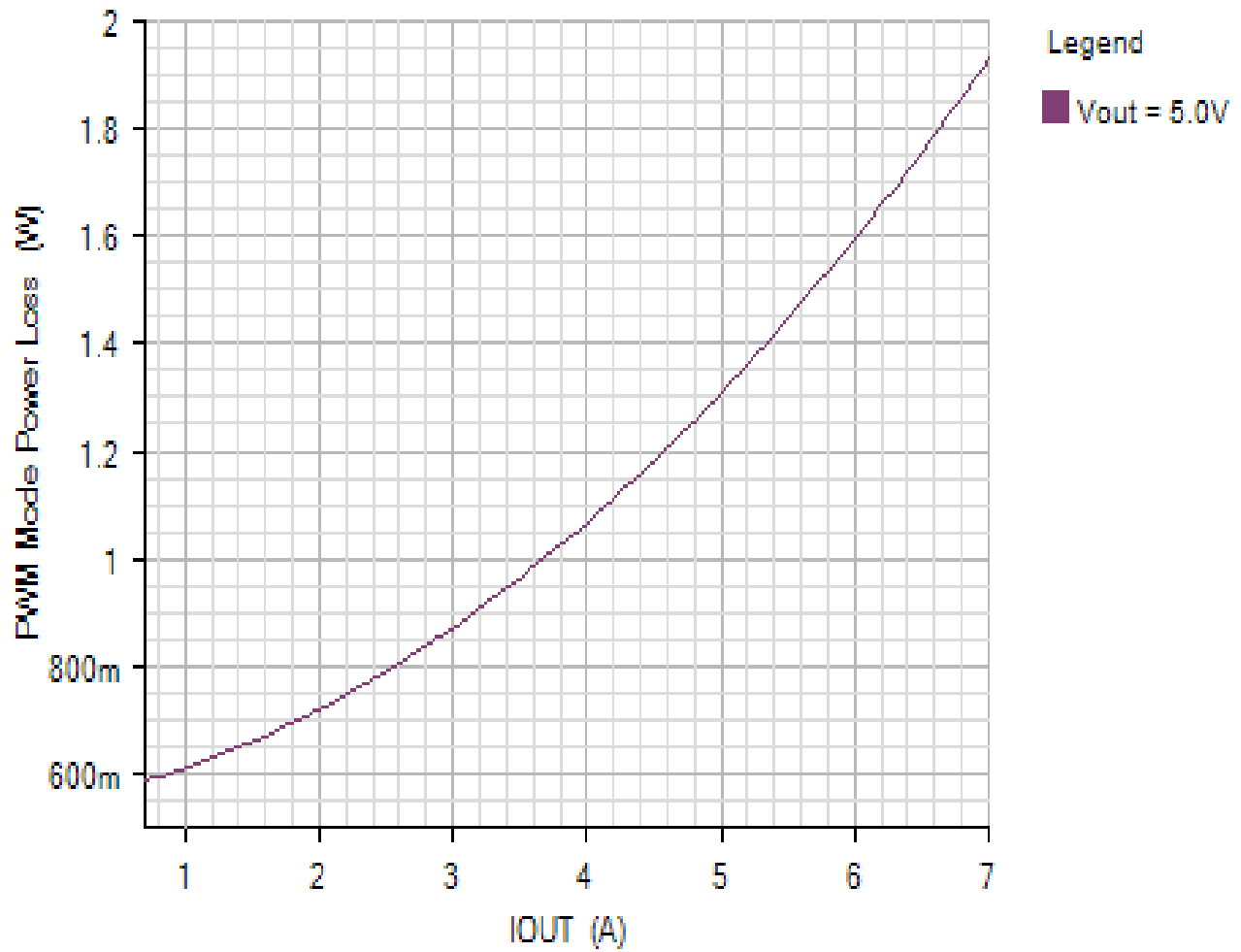


Efficiency - Tue Nov 20 2018 13:30:44

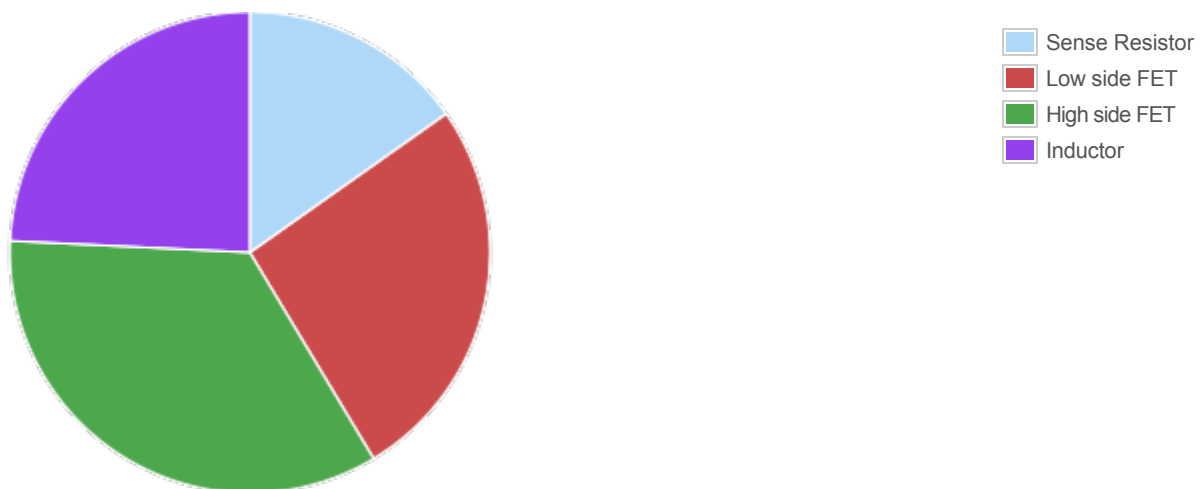


POWER_LOSS

Default



Losses



Component

Loss (W)

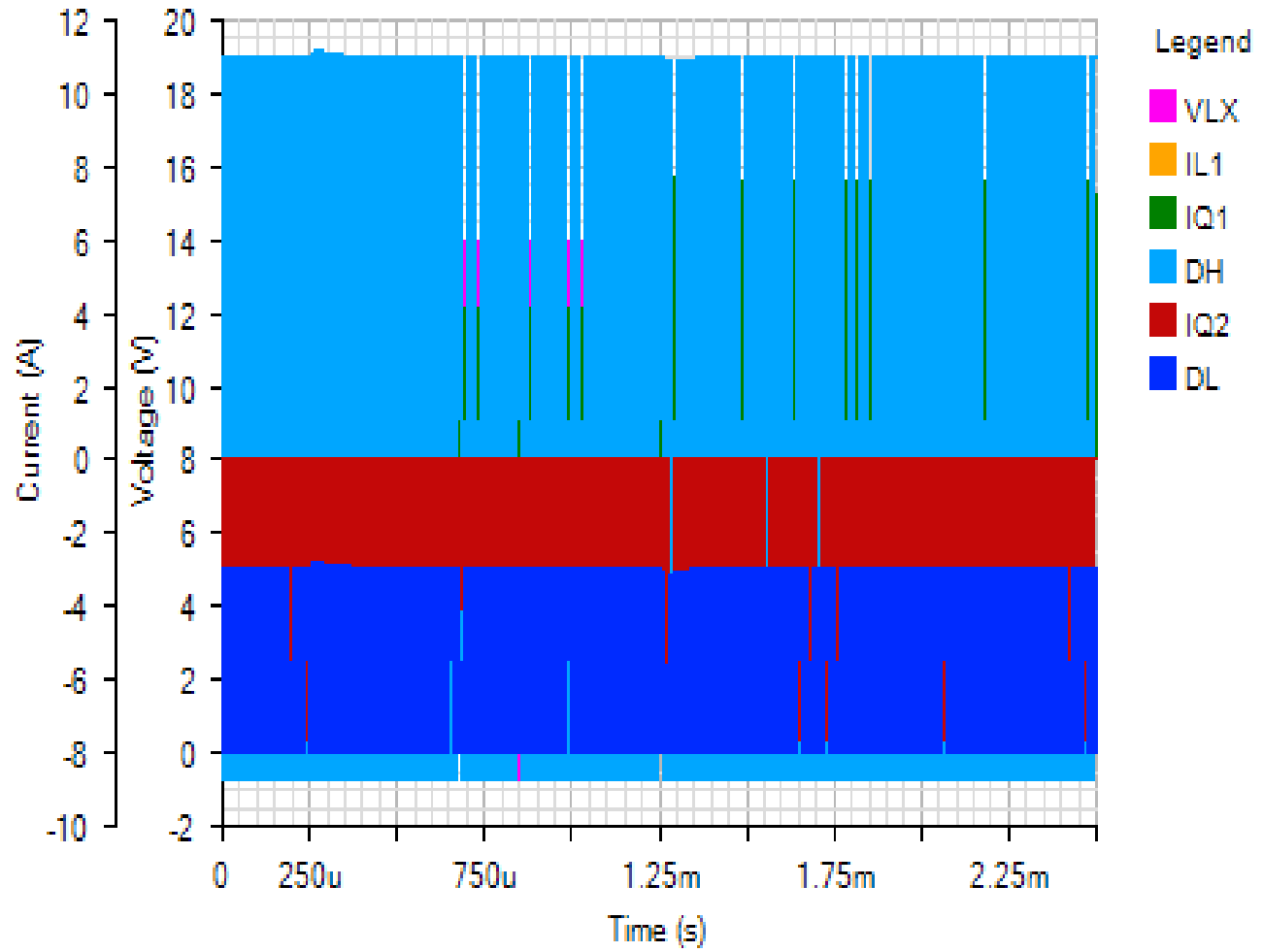
% of total

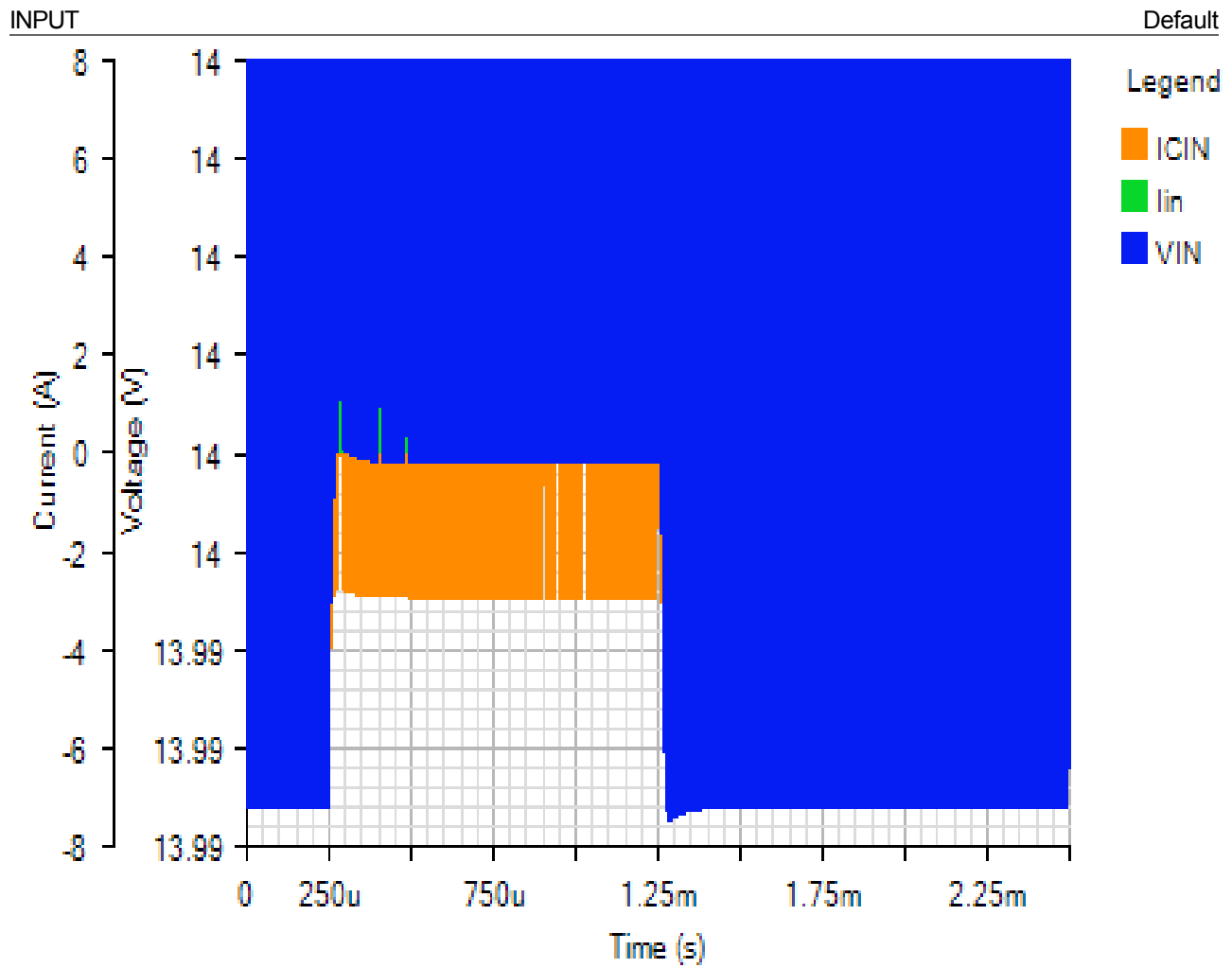
Component	Loss (W)	% of total
Sense Resistor	0.294	15.2
Low side FET	0.505247	26.2
High side FET	0.664156	34.4
Inductor	0.468007	24.2
Total	1.93141	100

Load Step - Tue Nov 20 2018 13:30:44

SWITCHING

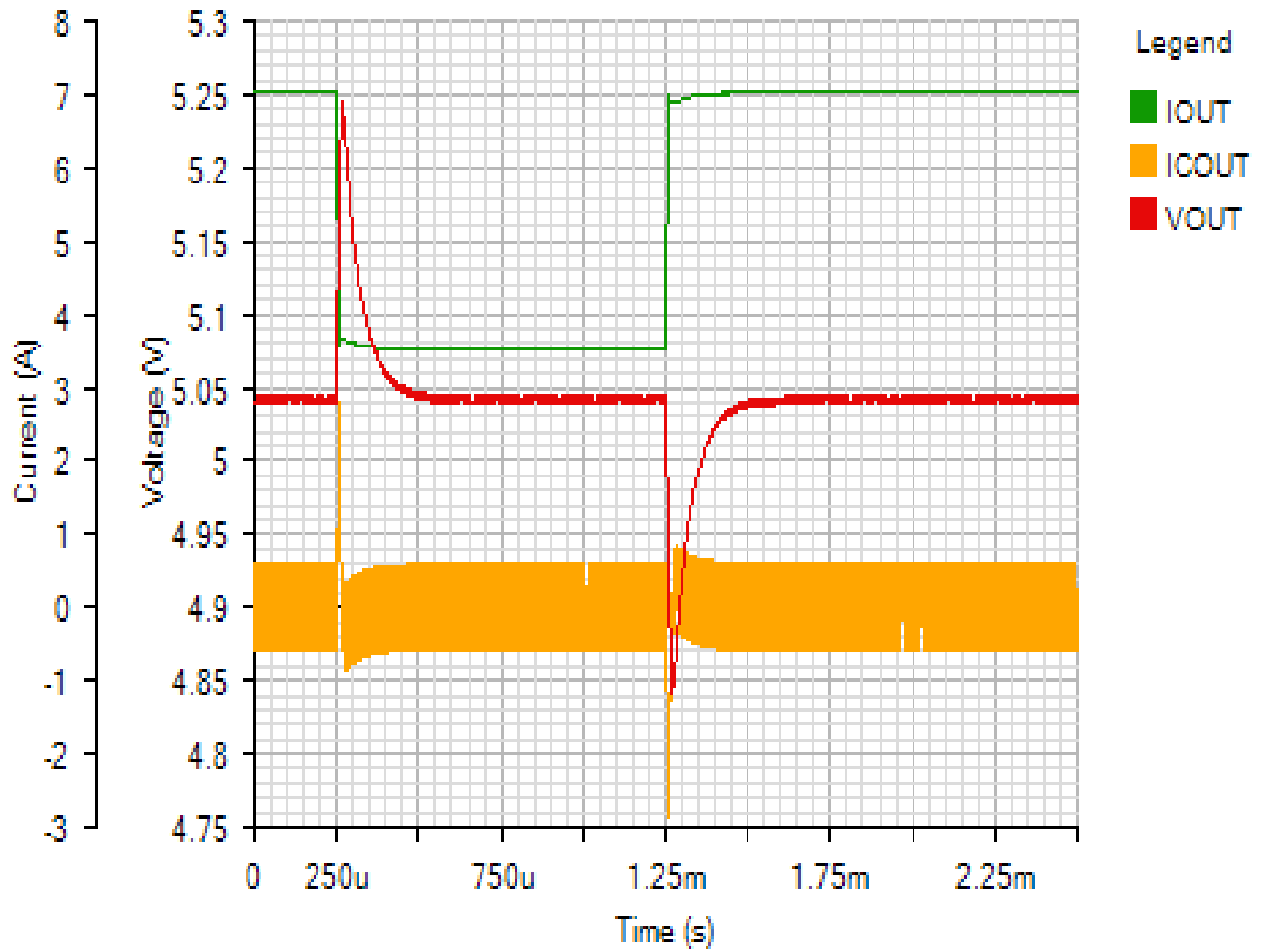
Default





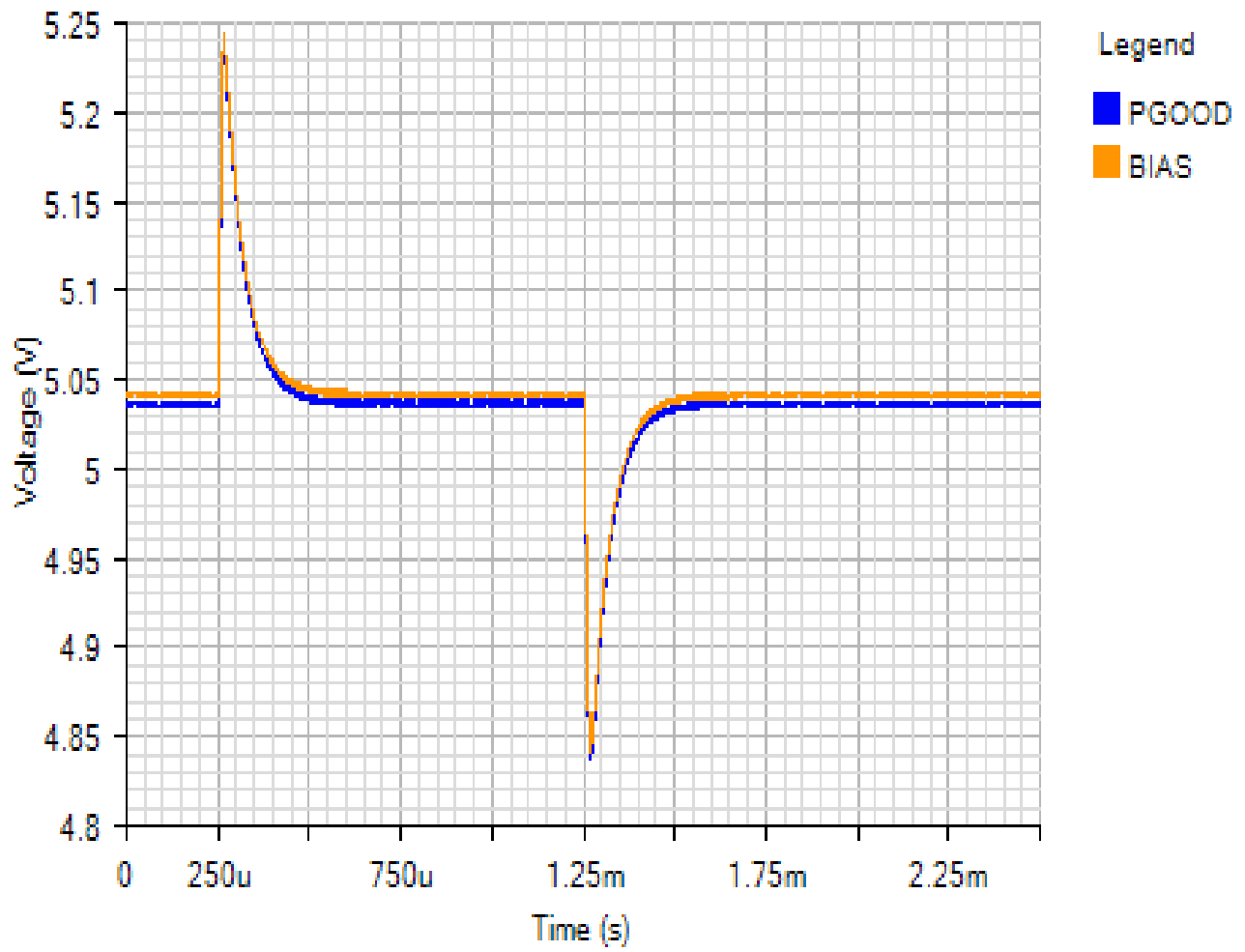
OUTPUT

Default



IC

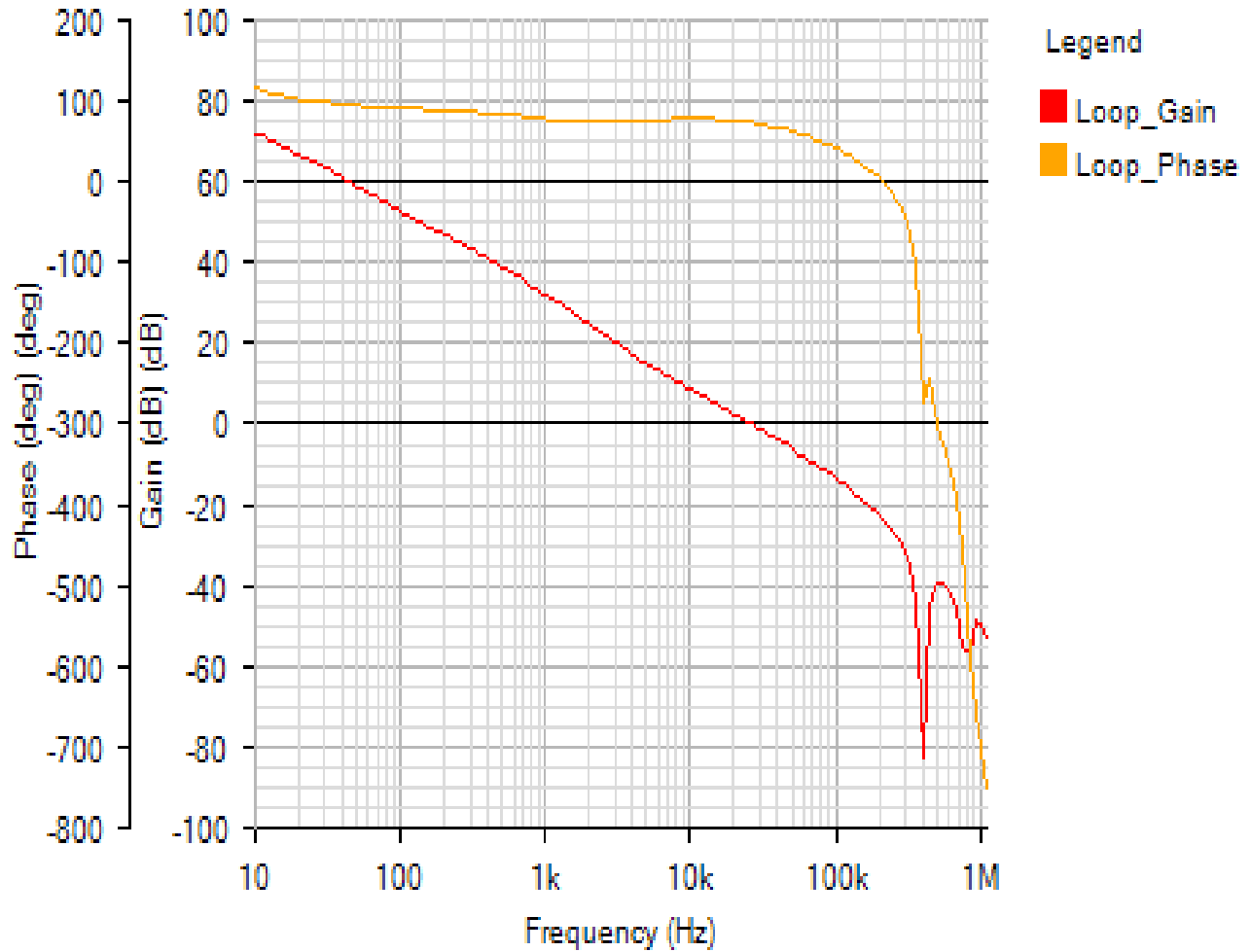
Default



AC Loop - Tue Nov 20 2018 13:30:44

BODE

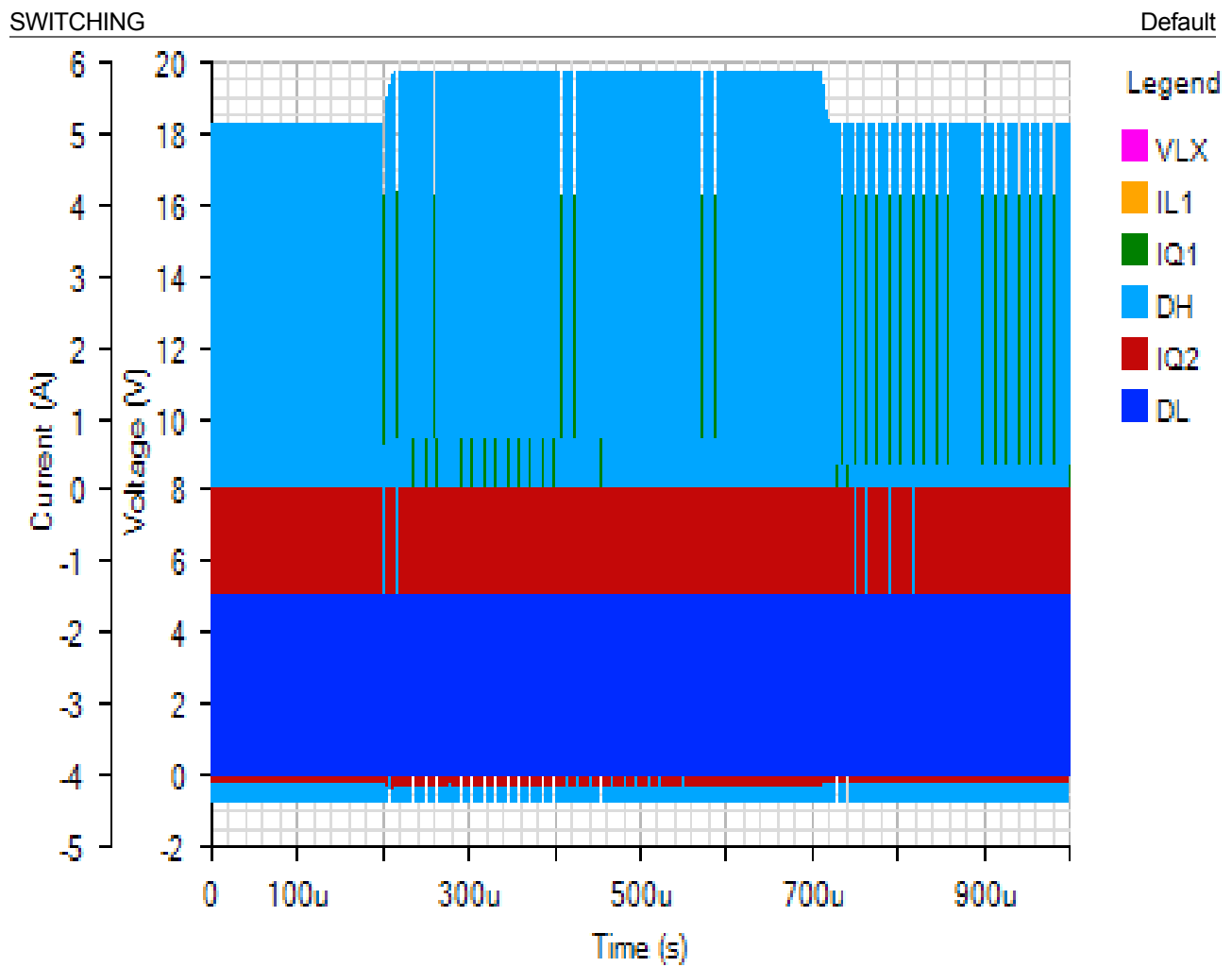
Default



Phase Margin: 73.87° at a crossover frequency of 25.6kHz

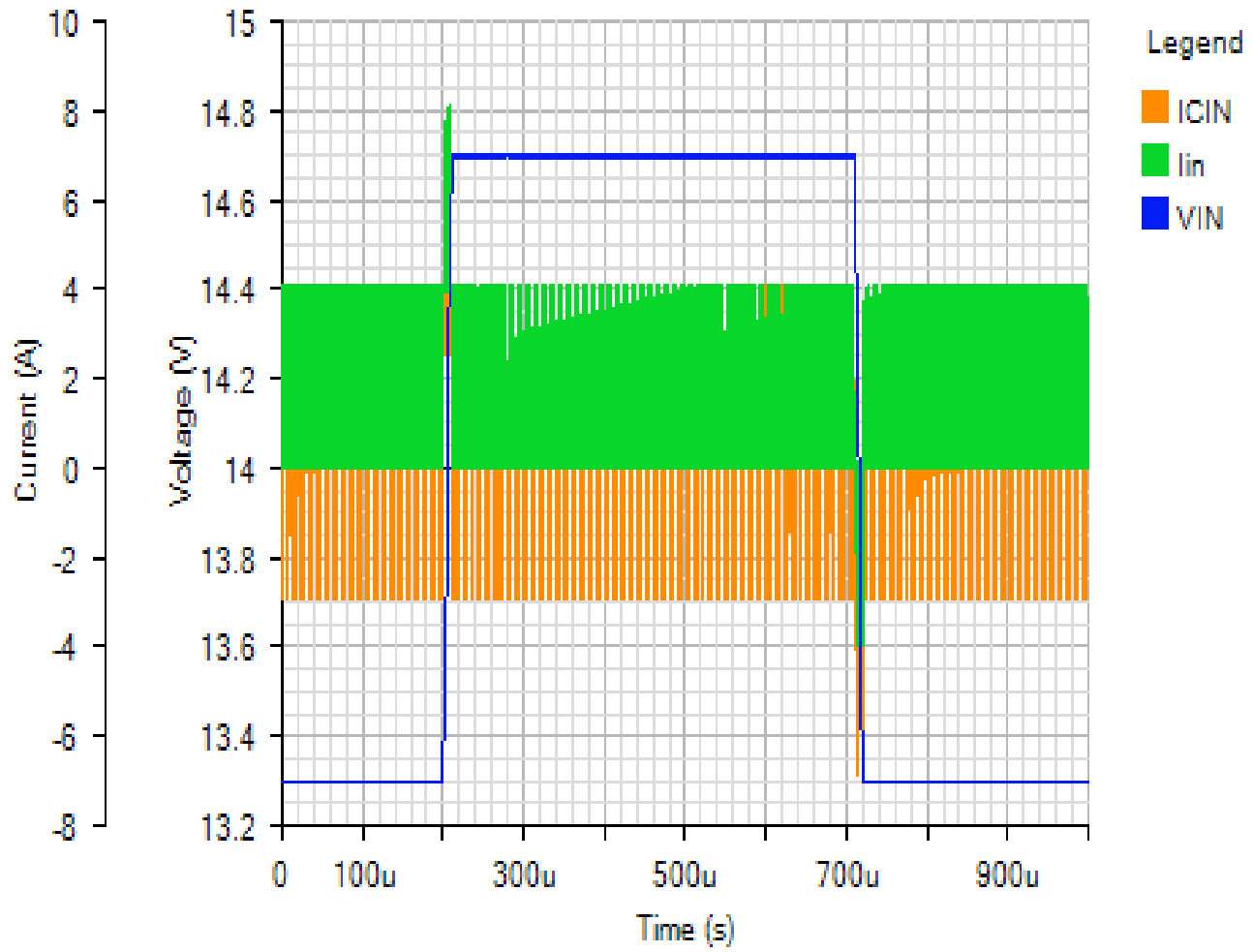


Line Transient - Tue Nov 20 2018 13:30:44



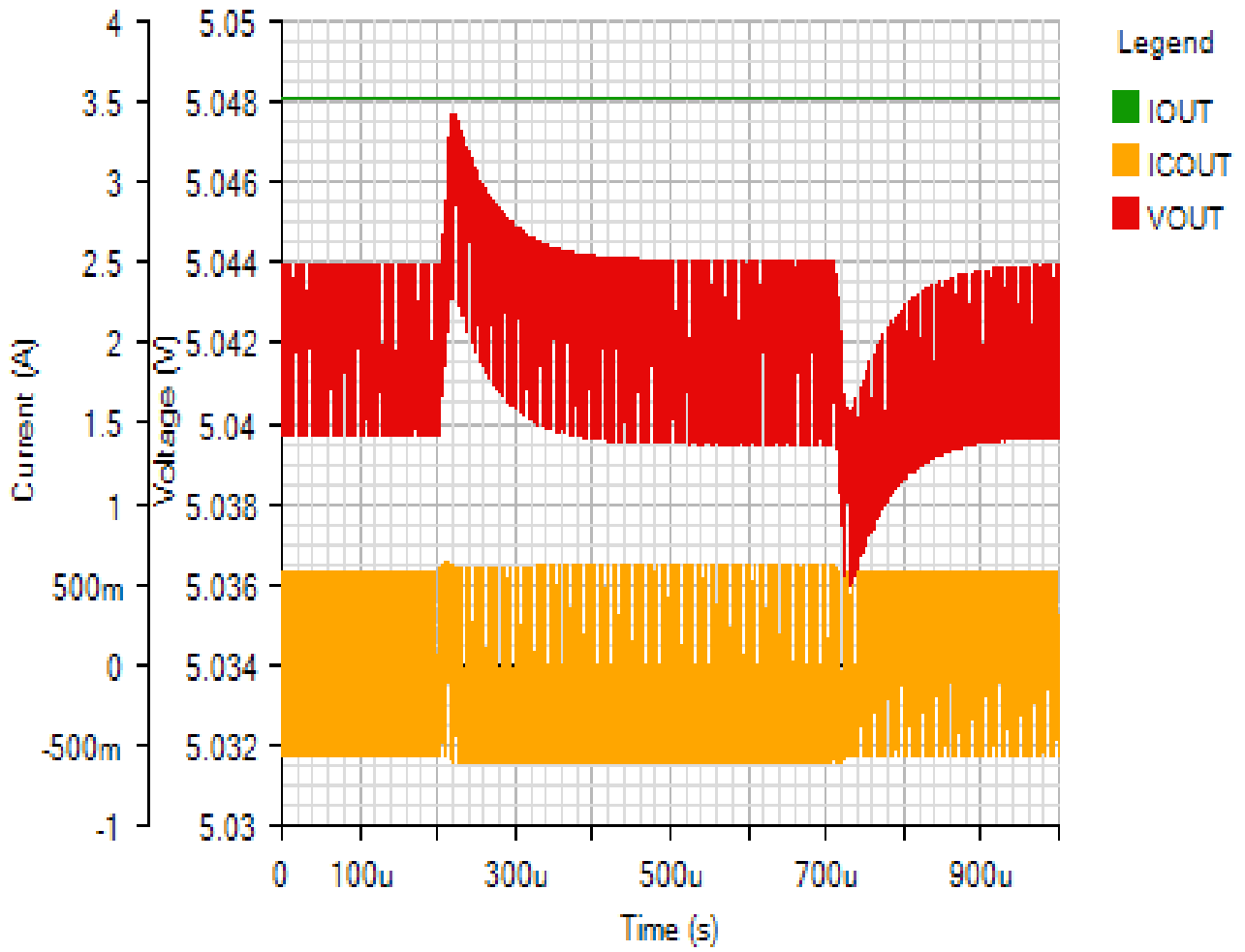
INPUT

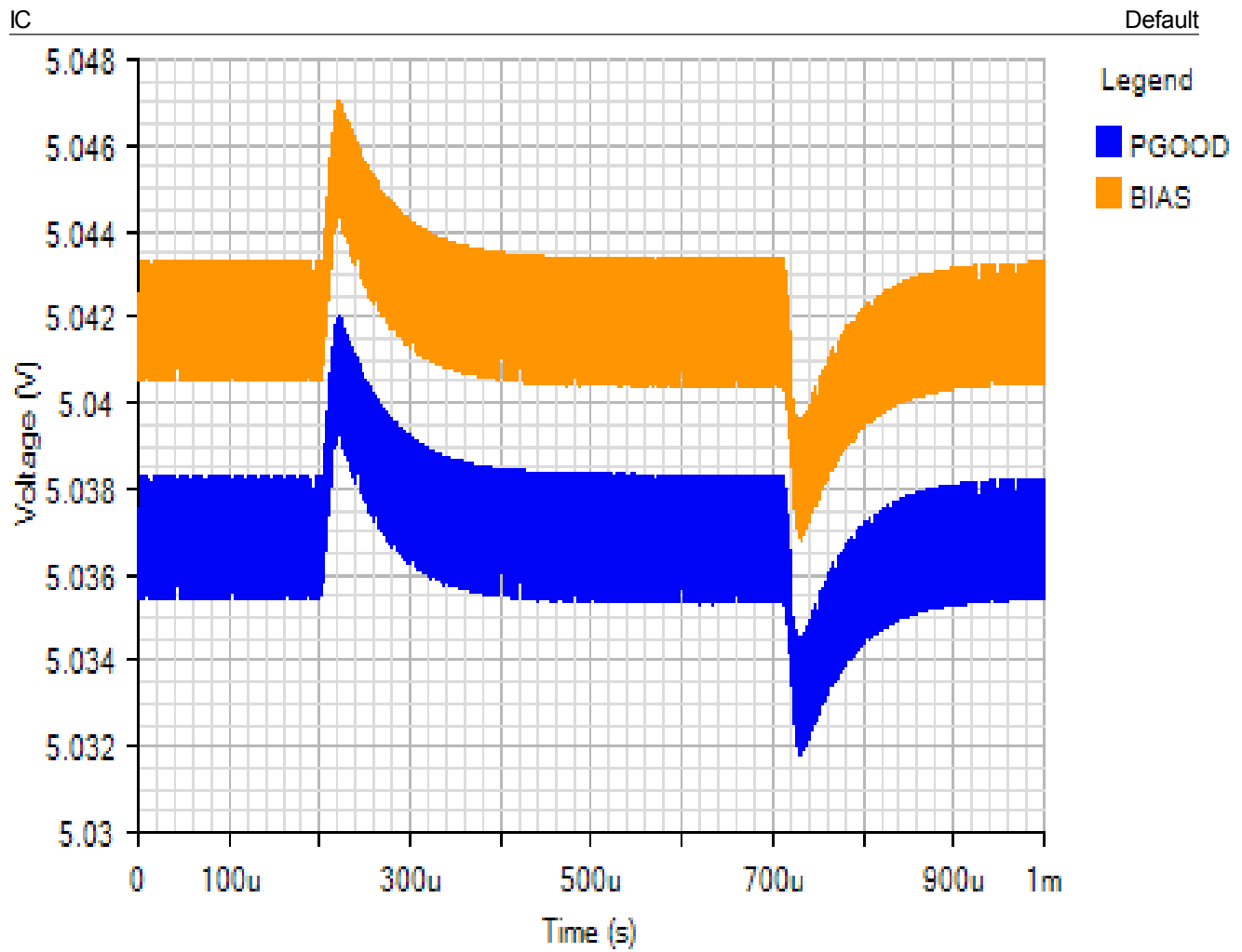
Default



OUTPUT

Default

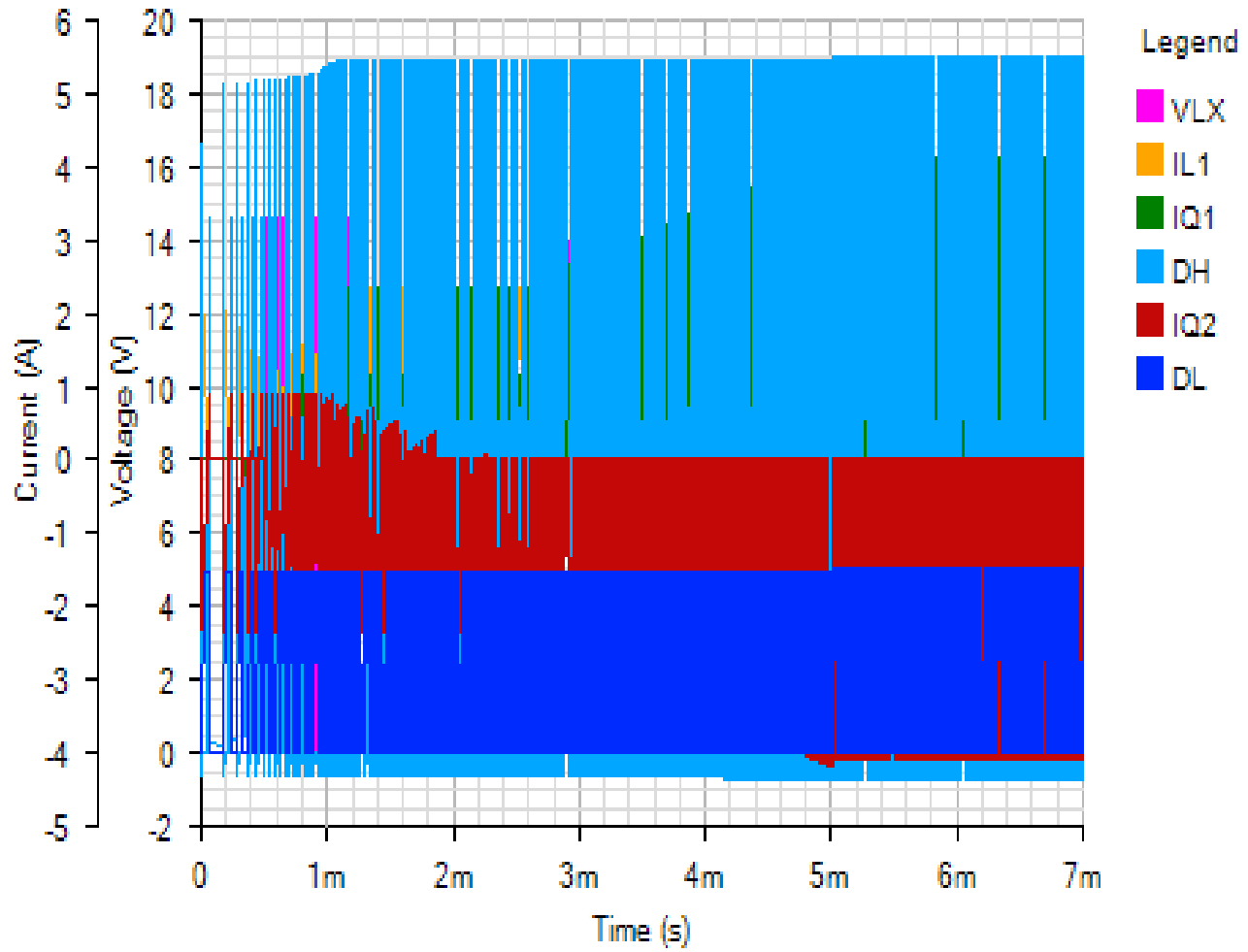




Start Up - Tue Nov 20 2018 13:30:44

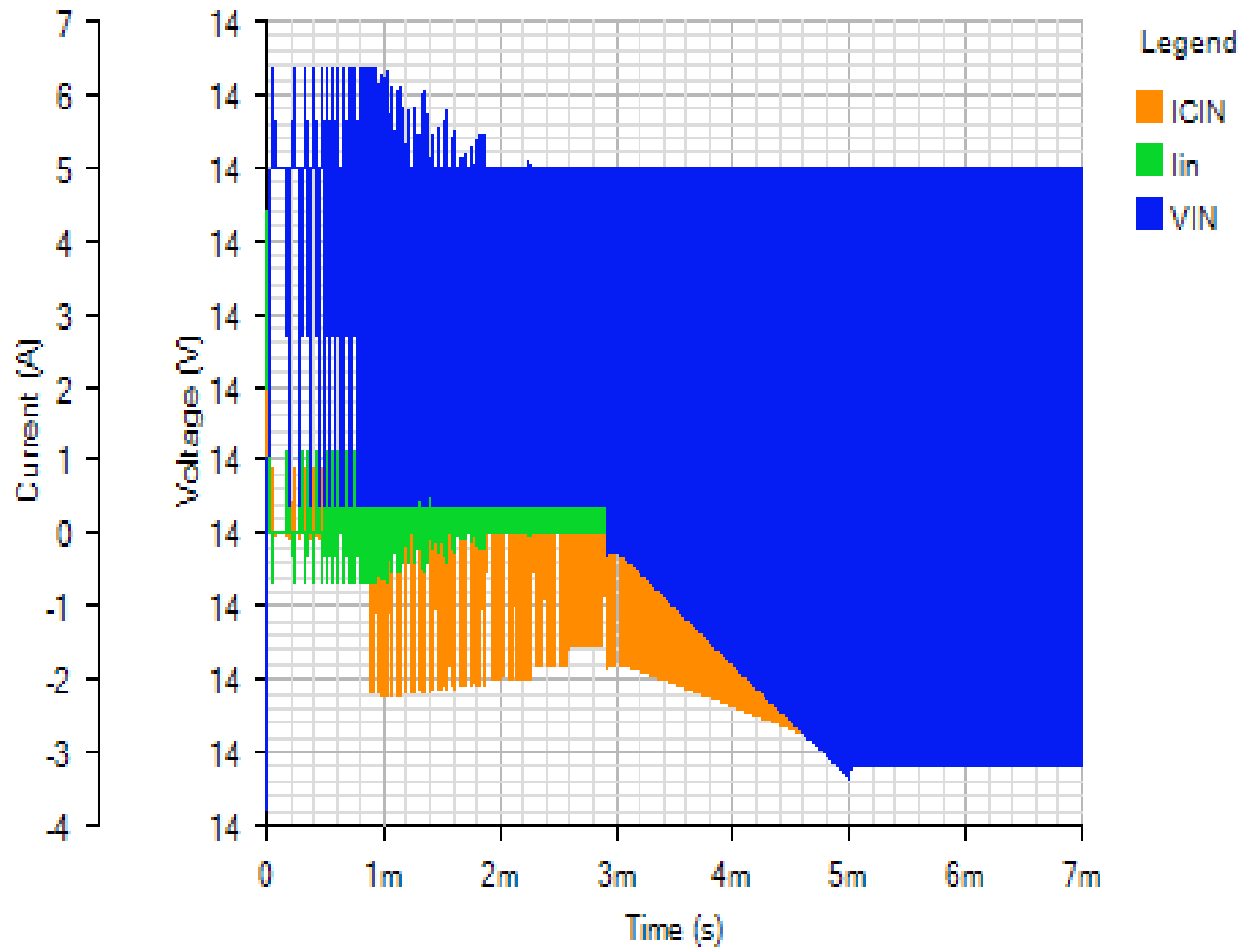
SWITCHING

Default



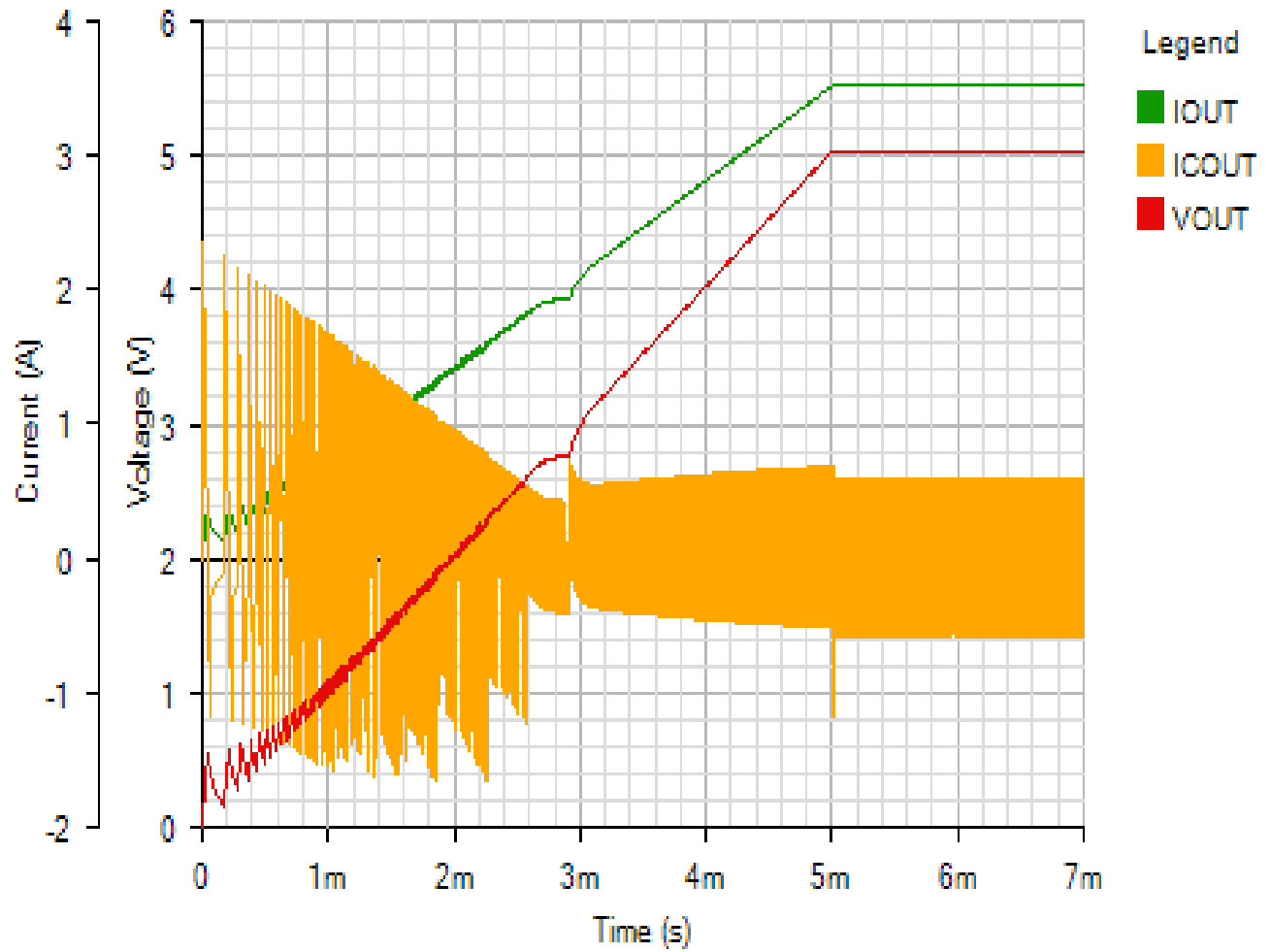
INPUT

Default



OUTPUT

Default



IC

Default

