5V, 500mA Buck Converter using the MAX17501F

MAXREFDES1274

Introduction

The MAXREFDES1274 is a buck converter using the MAX17501F high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs and internal compensation. This design produces a 5V output at up to 500mA from a wide input range of 6.5V to 60V. The device features peak-current-mode control with pulse-width modulation (PWM). The MAXREFDES1274 was optimized for small solution size and is laid out on a two-layer PC board.

Its other features include the following:

- Ultra-Compact Layout (31.52mm^2 Footprint Size)
- Wide Input Voltage Range of 6.5V to 60V
- 500mA Output Current
- 5V Output Voltage
- 600kHz Switching Frequency
- Adjustable Soft-Start Time (SS)
- Enable/Undervoltage Lockout (EN/UVLO)
- Open-Drain Reset Output Functionality
- Peak-Current-Mode Control with Pulse-Width Modulation (PWM)

Hardware Specifications

This document demonstrates the MAX17501F for a 5V application, allowing for a load up to 500mA at 5V. This design was optimized for a small solution size to demonstrate that competitive efficiency is achievable with small components on a two-layer PCB. Table 1 is an overview of the design specifications.

Table 1. Design Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX
Input Voltage	V_{IN}	6.5V	24V	60V
Output Voltage	V_{OUT}		5V	
Output Current	I_{OUT}		500mA	
Output Power	P_{OUT}		2.5W	
Peak Efficiency	η		94.8%	
Output Ripple	ΔV_{OUT}		< 12mV	
Output Undershoot	V_{US}		< 20mV	
Output Overshoot	V_{OS}		< 20mV	
Frequency	f_{SW}		600kHz	
Footprint Size*			31.52mm^2	

**Note:* *The footprint size is the sum of the footprint sizes for required components. This excludes the snubber components, AC analysis resistor (RAC), and electrolytic input capacitor.*

Designed-Built-Tested

This document describes the hardware in Figure 1. It provides a systematic technical guide to design a step-down converter using the MAX17501F, a fixed 5V output, high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs. The power supply was built and tested. The details follow later in this document.

Figure 1. MAXREFDES1274 hardware.

Synchronous Buck Converter

DC-DC buck converters are commonly used for their optimal output efficiency, low heat dissipation, high accuracy, small transient response, and low cost. There are two types of step-down DC-DC converters: synchronous and asynchronous buck converters.

Synchronous buck converters are widely used today in compact designs because of the superior efficiency to the asynchronous buck converter. The asynchronous buck topology uses an external Schottky diode for the low-side switch (Figure 2a) while the synchronous buck topology integrates a low-side MOSFET (LSFET) (Figure 2b). This reduces power loss and increases power efficiency significantly because it eliminates the diode's I_F x V_F power loss in exchange for the power lost across the MOSFET's low on-resistance.

Power dissipation across the diode in the asynchronous solution:

$$P_D = V_D \times I_{OUT} \times (1 - V_{OUT} / V_{IN})$$

Power dissipation across the MOSFET in a synchronous solution:

$$P_{FET} = R_{ON} \times I^2_{OUT} \times (1 - V_{OUT} / V_{IN})$$

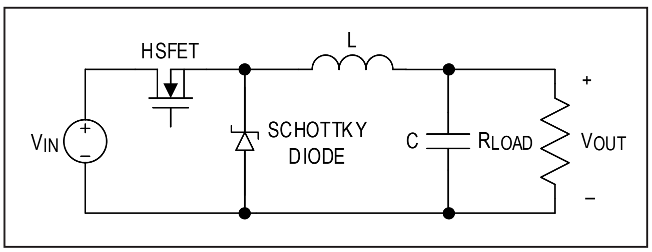

Figure 2a. Asynchronous buck converter topology.

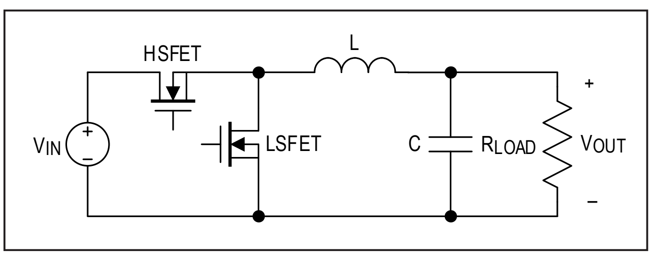

Figure 2b. Synchronous buck converter topology.

Design Procedure for Synchronous Buck Converter Using MAX17501

The design procedure provides a step-by-step process for power supply designers to select external components. The component designators in this document are in reference to the MAXREFDES1274 schematic. All other terms and variables are from the MAX17501 data sheet.

No feedback components are needed because this design uses the MAX17501F, a preset 5V output version of the MAX17501. The FB/VO pin should be connected to the V_{OUT}. Instead of connecting directly to V_{OUT}, this design connects to a 40Ω resistor between the FB/VO and V_{OUT}, named R_{AC}. This component is included for the ease of testing to obtain a loop response bode plot. R_{AC} is not included in the total solution size because is not essential to the operation.

Step 1. Base Design

The initial design was produced by the EE-Sim®, an online design and simulation environment, which greatly streamlines the design of switch-mode DC-DC converters. The EE-Sim® design and simulation environment considers input voltage range, ripple specifications, output voltage, output current, and design priorities. Once the EE-Sim® design and simulation environment produced a schematic, the components were later tweaked to improve performance and minimize solution size. The EE-Sim® produced the following component values, which are later tweaked for the end design:

L = 47µH

C_{IN} = 1µF

C_{OUT} = 3 x 10µF

Step 2. Inductor

Small size is the top priority of this design. So, the inductor was selected as the first component as it is typically the largest component in a power supply design. Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (ISAT), and DC resistance (R_{DCR}).

The MAX17501 data sheet recommends to select the inductor with the following equation:

$$L = \frac{4.8 \times V_{OUT}}{f_{SW}} = \frac{4.8 \times 5V}{600kHz} = 40\mu H$$

The minimum inductor size for CCM is:

$$L_{MIN} = \frac{D_{MAX} \times (V_{IN_{MIN}} - V_{OUT})}{f_{SW} \times di}$$

$$= \frac{0.77 \times (6.5V - 5V)}{600kHz \times 0.075} = 25.66\mu H$$

where *di* is assumed to be 15% of the full load (500mA x 15% = 75mA).

A value of 33µH was selected as small footprint inductors of this value are readily available.

The ASPI-4030S-330M was selected as a 33µH inductor with a saturation current of 1.1A, well above the output current for this design. A low 330mΩ DCR minimizes losses in the inductor.

Table 2. ASPI-4030S-330M Key Specifications

PARAMETER	VALUE
Inductance	33µH
Footprint Size	4mm x 4mm
DC Resistance	330mΩ
Current Rating	0.84A
Saturation Current	1.1A

Step 3. Output Capacitor

The MAX17501 data recommends to connect a minimum of 10µF (1206) capacitor at the output for fixed 3.3V and 5V output voltage versions.

A single ceramic output capacitor is used for this deign to minimize solution size although the EE-Sim® generated schematic recommends three 10µF in parallel. This single capacitor must have a derated value of at least 10µF at 5V DC.

The GRM21BD71A226ME44, a 22µF ceramic capacitor with a 5V derating of ~47% of the nominal capacitance (approximately 10.34µF), was selected. Temperature stability was sacrificed for the small solution size.

Table 3. GRM21BD71A226ME44 Key Specifications

PARAMETER	VALUE
Nominal Capacitance	22µF
5V Derated Capacitance	Approx. 10.34µF
Footprint Size	0805 (2mm x 1.25mm)
Temperature characteristics	X7T
Rated Voltage	10V

Step 4. Input Capacitor

TThe discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and allowable peak-to-peak voltage ripple dictate the capacitance requirement. The device's high switching frequency allows the use of smaller value input capacitors. A minimum value of 1µF should be used for the input capacitor as mentioned in the data sheet.

Generally, an X7R ceramic capacitor should be used for their temperature stability. However, an X7S was deemed as fine for this design.

This design has an input voltage range of 6.5V to 60V. A capacitor was chosen such that the 60V derated capacitance remained near or above 1µF. The GRM31CC72A475KE11 was chosen due to its derated capacitance at 60V DC and relatively small footprint.

Table 4. GRM31CC72A475KE11 Key Specifications

PARAMETER	VALUE
Nominal Capacitance	4.7µF
60V Derated Capacitance	0.94µF
Footprint Size	1206 (2mm x 1.25mm)
Temperature characteristics	X7S
Rated Voltage	100V

*Note that this design also includes a large, 33µF electrolytic capacitor on the input. This capacitor is meant to damp any oscillations caused by a long input power path. It is not included in the final solution footprint size because it is not essential for the operation.

Step 5. Soft-Start Capacitor

The MAX17501 implements an adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to GND programs the soft-start period. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor using the following equation:

$$C_{SS} \geq 19 \times 10^{6} \times C_{SEL} \times V_{OUT}$$

$$C_{SEL} = 22\mu F$$

$$V_{OUT} = 5V$$

$$\text{So, } C_{SS} = 2.09nF$$

The selected soft start capacitor (C_{SS}) is a 4.7nF ceramic capacitor in a 0201 footprint.

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{ss} = \frac{C_{SS}}{5.55 \times 10^{-6}} = \frac{4.7nF}{5.55 \times 10^{-6}} = 846.8\mu s$$

Table 5. GRM033R61E472MA12 Key Specifications

PARAMETER	VALUE
Nominal Capacitance	4.7nF
Footprint Size	0201 (0.6mm x 0.3mm)
Temperature characteristics	X5R
Rated Voltage	25V

Step 6. Input Undervoltage Lockout

The Undervoltage Lockout (UVLO) level sets the input voltage at which the device turns on. The UVLO is set with a resistor divider connected from the V_{IN} to GND, with the center node connected to the EN/UVLO pin (Figure 3).

The data sheet recommends a value of 3.3MΩ for R_1. R_2 is calculated to produce a UVLO of 5.9V using the following equation:

$$R_2 = \frac{R_1 \times 1.218}{(V_{INU} - 1.218)} = \frac{3.3M\Omega \times 1.218}{(5.9V - 1.218)} = 858.5k\Omega$$

R_2 is selected as 866kΩ for this design, which sets UVLO to 5.86V.

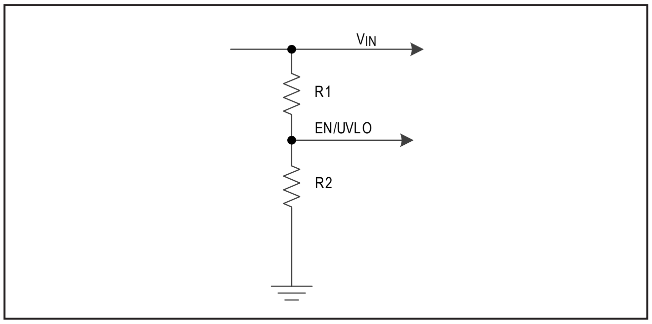

Figure 3. Adjustable EN/UVLO network.

Non-Essential Components Used in this Design

- C_{IN1} is a large, electrolytic capacitor meant to damp any oscillations caused by a long input power path.
- R_{AC} is included to simplify loop response measurements. This can be replaced with a short.
- R_{SNUB} and C_{SNUB} create an RC snubber to reduce ringing on the output. These component values can be finetuned based on the resonant frequency of the device. A capacitance of 10pF and resistance of 100Ω were selected as general values for the time being to give a 'good enough' performance.

Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/21	Initial release	—