1200W DC-DC Buck Converter Using the MAX15157B

MAXREFDES1258

Introduction

The MAXREFDES1258 is a 1200W, 12V, 4-phase DC-DC buck converter that delivers up to 100A load current. The design is optimized for data-center applications with an input voltage range of 35V to 60V. it is also suitable for industrial power supplies, and automotive and communication applications. The MAXREFDES1258 employs a MAX15157B fixed-frequency, current-mode PWM controller that drives power MOSFETs in the buck configuration, allowing the device to operate as a step-down regulator. The control loop uses a valley current-mode architecture to optimize performance with low-duty cycles and provides the shortest on-time possible. The output voltage is set externally through a resistor divider network using the 2V default internal reference. The load current is balanced equally between the two interleaved phases using a state-of-the-art differential current-sense and balancing network.

Its other features include:

- Wide 35V to 60V input voltage range
- Highly regulated output voltage with ±1% ripple
- State-of-the-art current balancing for dual-phase operation
- Interleaved 180° out-of-phase operation
- Current monitor outputs of individual phases
- Robust fault protection
- Cycle-by-cycle and average overcurrent protection
- Multiple levels of overvoltage protection

Hardware Specifications

A 4-phase, 1200W buck converter using the MAX15157B is demonstrated for a 12V DC output application. The power supply delivers up to 100A at 12V. Table 1 is an overview of the design specification.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	35V	60V
Switching Frequency	f_{SW}	150kHz	
Output Voltage	V_{OUT}	12V	
Output Current	I_{OUT}	0	100A
Output Voltage Ripple	ΔV_{OUT}	1% of V_{OUT}	
Output Power	P_{OUT}	1200W	
Maximum Efficiency	η	96%	

Designed–Built–Tested

This document describes the hardware in Figure 1. It provides a detailed, systematic technical guide to design a 4-phase buck converter using the MAX15157B current-mode controller. The power supply was built and tested. The details follow later in this document.

Figure 1. Top and bottom of the MAXREFDED1258 board.

Nonsynchronous Buck Converter

The main components of a buck converter are the power switch, which is usually a MOSFET, inductor, and diode. A magnetic field is generated in the inductor as the MOSFET is switched on and off. Current flows into the inductor and through the output when the switch is on (or closed). Current still flows from the inductor to the output load through the free-wheeling diode due to the magnetic field when the switch is off (or open). The transistor switch supplies the output load with current when it is on. The current flow to the load is restricted initially as energy is also stored in the inductor. Therefore, the current in the load and the charge on the output capacitor build up relatively slowly compared to the switch-on time of the MOSFET. There is a large voltage across the diode when it is on, which causes it to be reverse-biased. The energy stored in the inductor's magnetic field is released when the transistor switch is off. The voltage across the inductor becomes reverse polar and enough stored energy is available to maintain the current flow while the transistor is open. The reverse polarity of the inductor allows the current to flow in the circuit through the load and diode, which is now forward-biased. The load voltage begins to fall once the inductor is drained of most of its stored energy. The charge stored in the output capacitor then becomes the main source of current. This leads to the ripple waveform in Figure 2.

Synchronous Buck Converter

Synchronous buck converters are more efficient than conventional nonsynchronous buck converters. The conventional freewheeling diode is replaced by a low-side MOSFET in a synchronous buck converter (Figure 3). Consequently, the power dissipated in the low-side MOSFET minimizes compared to the power dissipating in the diode.

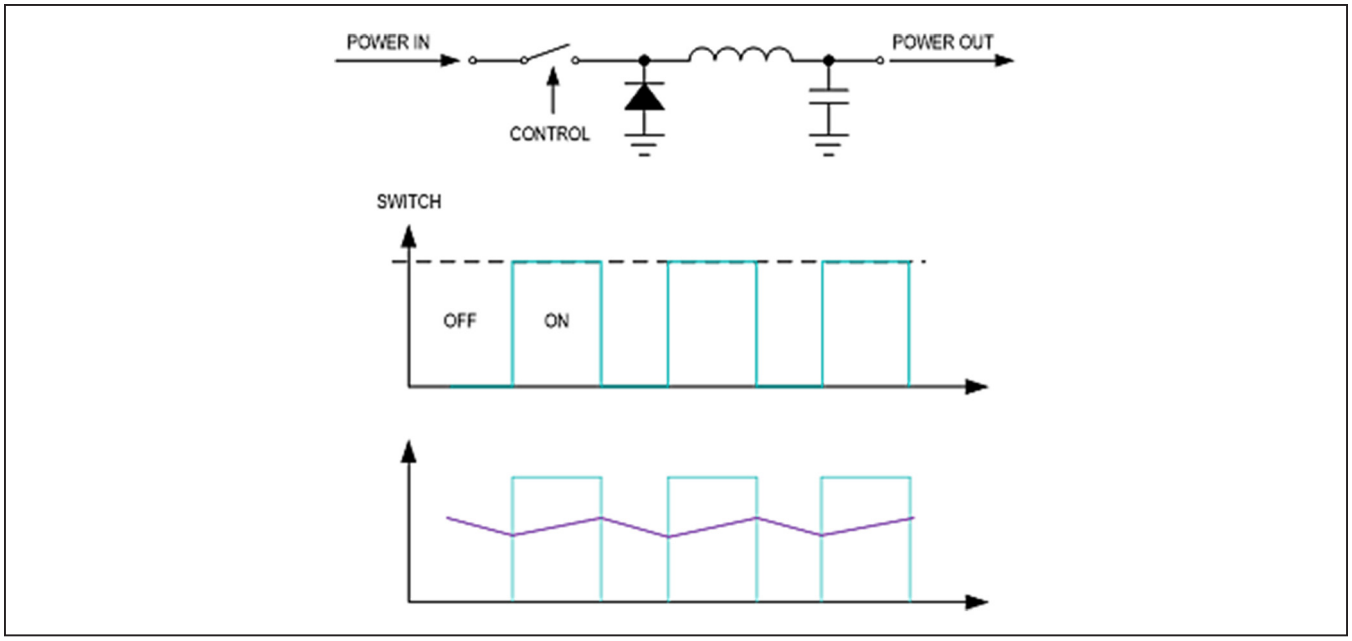

Figure 2. Typical buck converter power supply.

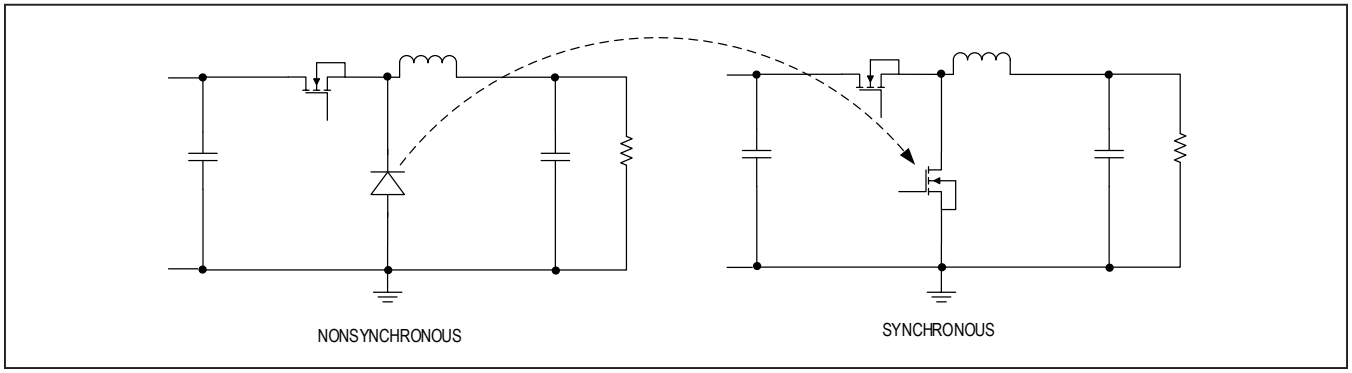

Figure 3. Nonsynchronous vs. synchronous buck converters.

The low-side MOSFET is always driven opposite to the high-side MOSFET (when one switch is on, the other is off). The complementary switching of the high-side and low-side MOSFETs regulates the output to its set value in steady-state conditions. Figure 4 illustrates the basic operation of a synchronous buck converter.

The switching period begins with switch S_1 turning on while switch S_2 is off, which creates a conduction path from V_{IN} to the load. The magnetic field within the inductor builds up while S_1 is on. S_1 is on if the control algorithm dictates. The low-side switch S_2 turns on after a slight delay when S_1 turns off. It is a break-before-make scheme that ensures S_1 and S_2 are never on simultaneously. This time delay is called the dead time (t_D).

The current flows through the body diode in the low-side switch during t_D (Figure 5) because the stored energy in the inductor must be discharged. The low-side MOSFET's body diode acts as a free-wheeling diode when both the MOSFETs are off. S_2 is turned on after T_D and the inductor discharges through the on-resistance of S_2 for the remaining switching period. Discharging the inductor through the low on-resistance of the low-side MOSFET significantly reduces conduction losses compared to a conventional buck converter that uses a diode in place of the low-side MOSFET. The control algorithm uses these three states to regulate the output based on the feedback signals from the converter.

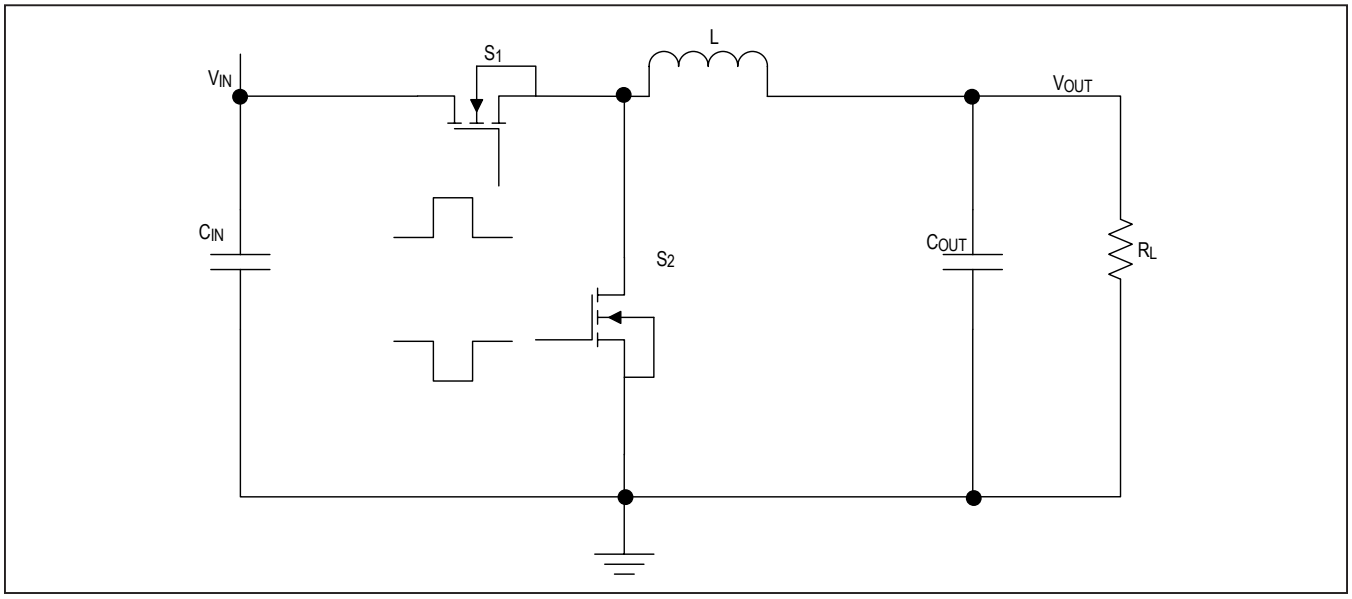

Figure 4. Basic schematic of a synchronous buck converter.

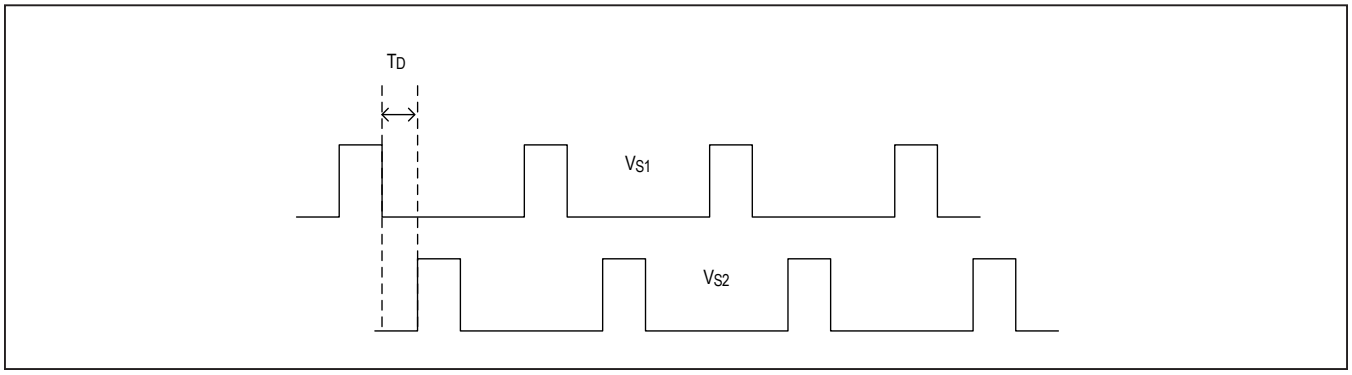

Figure 5. Gate signals of a synchronous buck converter.

Multiphase Synchronous Buck Converter

Many techniques are used to reduce the stress on components used in electronics circuits. For example, two resistors in parallel share the current to reduce current stress flowing through a single resistor. Similarly, two resistors are used in series to divide the voltage stress across them. Buck converter power supplies scale in size at a rate proportional to the load current. Magnetic and capacitive components become more and more stringent in high-current buck power supplies, requiring inductors of larger sizes along with a higher number of input and output capacitors. The multiphase buck converters are used in such scenarios, where two or more buck converters are connected in parallel to scale the power accordingly. Each buck converter has its own input capacitor, low/high-side MOSFETs, and inductor. The load side of each inductor is connected to a single output capacitor bank (Figure 6). The output currents of individual buck converters are added together at the output to give a higher total load current. Multiphase buck converters are typically required for high-current and low-voltage power supplies. They are implemented in computing, data center, and telecommunication applications.

Each individual buck converter in this configuration is called a phase. Two or more phases combine for the multiphase implementation of a buck topology. The phases are interleaved, where each phase is multiplexed in time with respect to other phases to get the advantages of multiphase configurations (Figure 7). The driving signal of the high-side MOSFET of each phase is 360/N degrees out-of-phase with respect to other phases. The phases are 180° out of phase where N is the total number of phases, such as for a two-phase design, while they are 120° out of phase for a three-phase design, and so on.

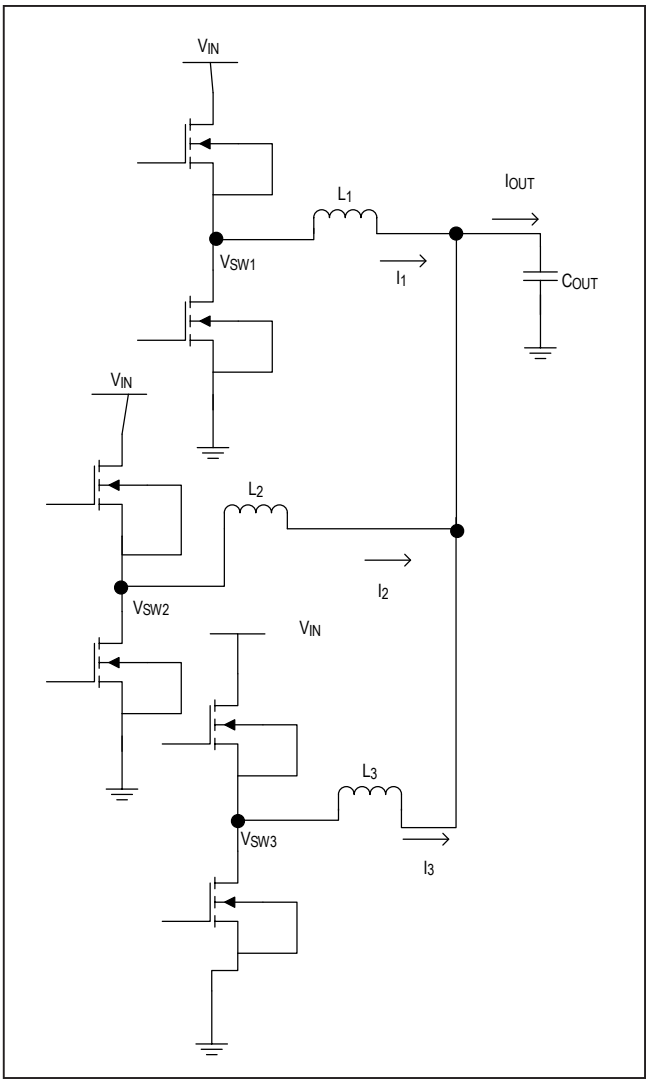

Figure 6. Typical multiphase buck converter configuration.

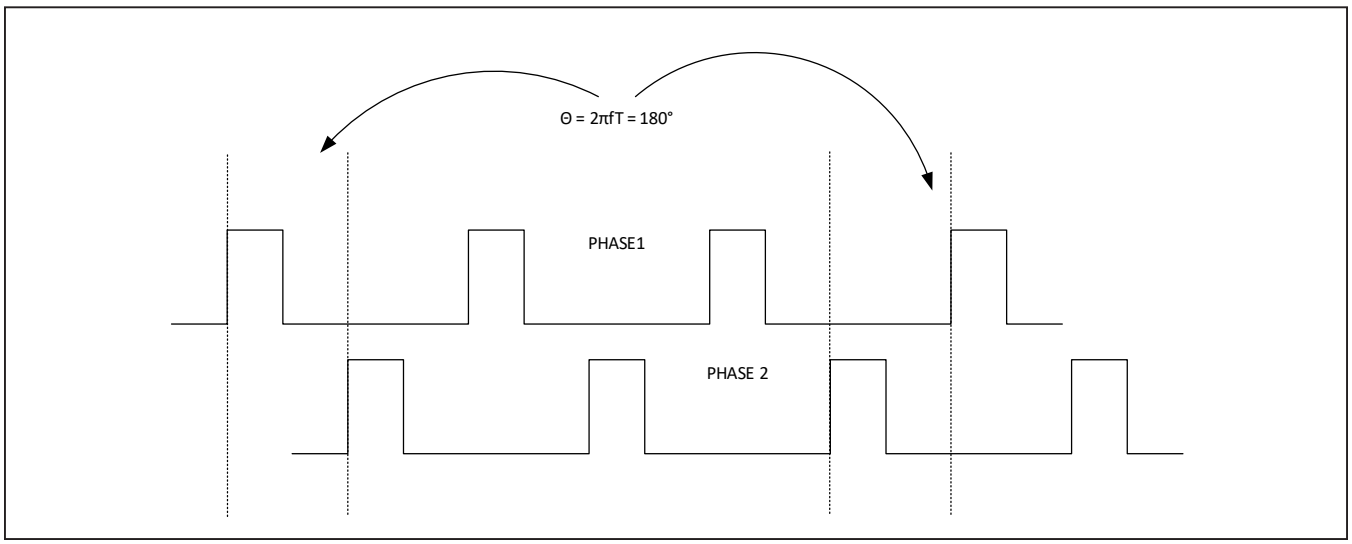

Figure 7. Interleaving of phases in a two-phase buck converter.

Selecting the Output Capacitors in Buck Converters

Output Capacitors of Single-Phase Buck Converters

The output current of a buck converter is the current flowing into the inductor. The inductor current has a certain DC value (I_{OUT}) with the current ripple (ΔI_L) riding over it. The main function of the output capacitor (C_{OUT}) is to provide a constant voltage output under steady-state and transient-load conditions. The ripple of the inductor current passes through the output capacitor while the DC current flows to the load. The COUT capacitance and effective series resistance (ESR) affect the loop stability, output voltage ripple, and load-transient response. The output voltage ripple has two components: voltage drop across the ESR (not shown in Figure 8 for simplicity) and variations in the charge stored in C_{OUT}. The ESR component of the output ripple is minimal for ceramic capacitors. Use multiple capacitors in parallel to meet the ESR requirement in high-current applications.

The voltage ripple (ΔV_{COUT}) across C_{OUT} under steady-state conditions is:

$$\Delta V_{COUT(RIPPLE)} = \frac{\Delta Q_{OUT}}{C_{OUT(MIN)}}$$

where:

ΔQ_{OUT} = rate of change of charge

$C_{OUT(MIN)}$ = minimum output capacitance

The rate of change of charge is calculated by integrating the capacitor current with respect to time:

$$\Delta Q_{OUT} = \frac{1}{2} \times \left(\frac{1}{2} \Delta I_L \right) \times \frac{1}{2} \left[t_{ON} + t_{OFF} \right]$$

$$= \frac{1}{8} \times \Delta I_L \times t$$

where:

t_{ON} = on-time

t_{OFF} = off-time

t = switching period

Therefore, $\Delta V_{COUT(RIPPLE)}$ is:

$$\Delta V_{COUT(RIPPLE)} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT(MIN)}}$$

The $C_{OUT(MIN)}$ is the minimum amount of capacitance required to keep $\Delta V_{COUT(RIPPLE)}$ within limits under static load conditions. Generally, the output capacitors are sized appropriately to withstand the expected step load with acceptable output voltage deviation (ΔV_{COUT}).

The required C_{OUT} is the following for a step current of I_{STEP} and to keep the output voltage deviation as $\pm\Delta V_{COUT}$:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{COUT}}$$

whereas $t_{RESPONSE}$ is:

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}} \right)$$

where:

f_C = bandwidth of the control loop

Output Capacitors of Multiphase Buck Converters

The selection of output capacitors in buck converters is governed by the output voltage ripple requirement. The total output load current is divided in interleaved phases in multiphase buck converters. Therefore, the thermal stress on all the circuit parameters within a phase is effectively reduced. However, Figure 9 shows an advantage in this configuration, which is the reduction of the output voltage ripple. The voltage ripple of the total output voltage is the sum of inductor current ripples in all the phases multiplied by the ESR of the output capacitor because the phases are turning on with a phase shift. The current in one phase is rising while the current in the other phase is falling, leading to lower total current. The output voltage ripple is effectively zero for multiphase operations under certain duty cycle values.

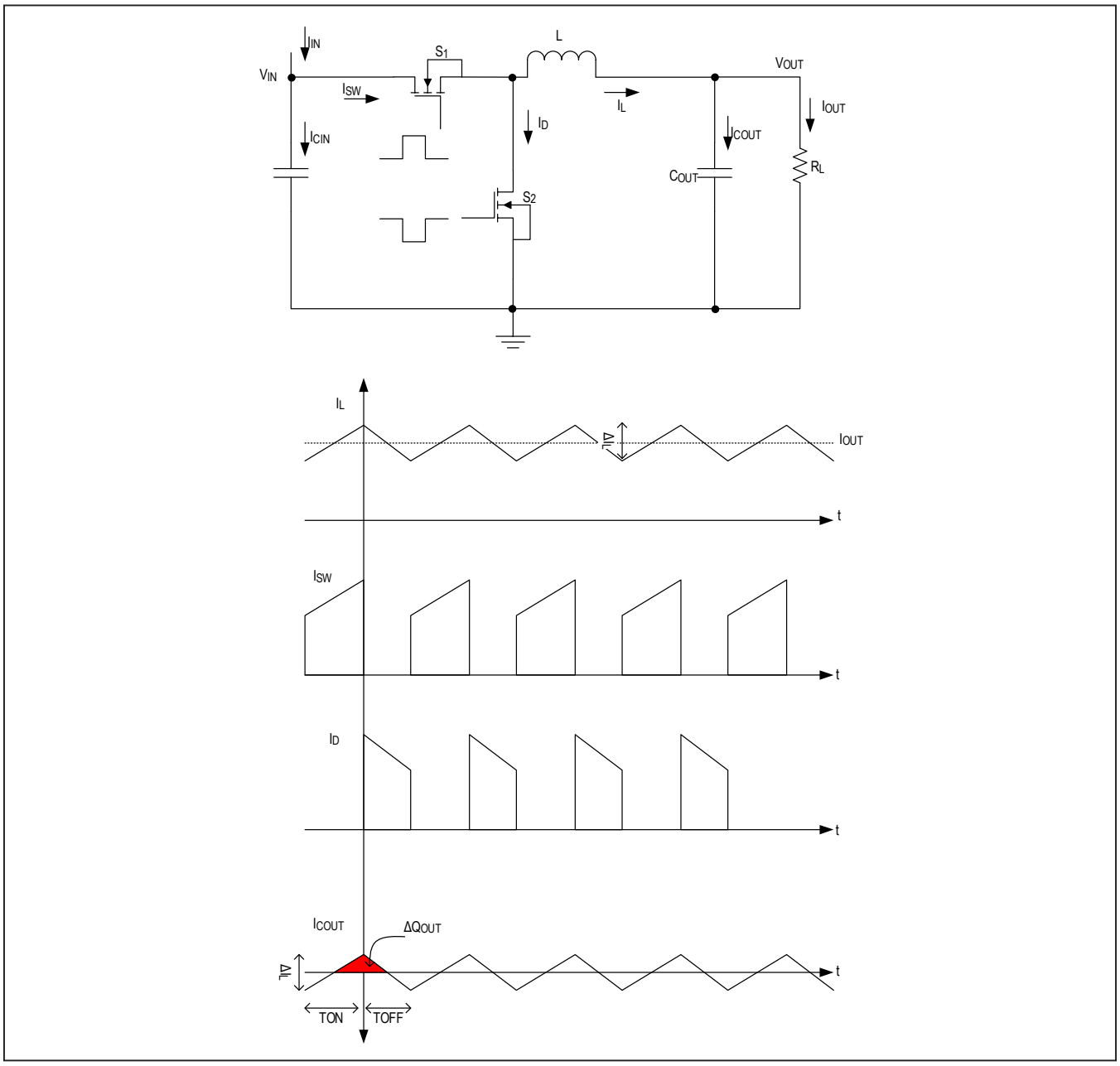

Figure 8. Current in single-phase buck converter output capacitor.

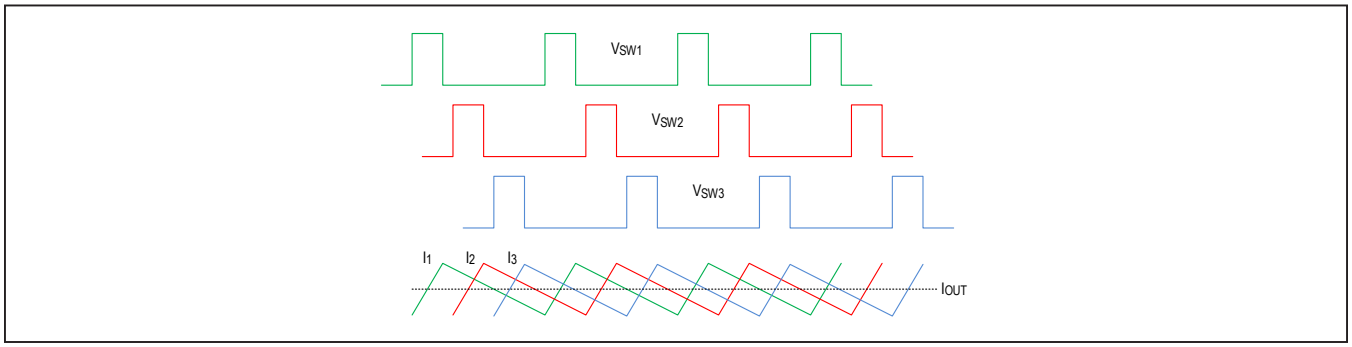

Figure 9. Switch nodes and inductor currents of a three-phase buck converter.

Figure 10 shows the relationship between the ratio of the total/phase ripple and duty cycle. The effective ripple for multiphase operation is zero at certain values of the duty cycle. These points occur at duty cycles of 50% for two-phase, 33% and 66% for three-phase, and 25%, 50%, and 75% for four-phase operations. The magnitude of the output voltage ripple is appreciably reduced while its frequency is effectively multiplied by the number of phases. Thus, we see that the output voltage ripple can be significantly reduced by interleaving the individual phases of the multiphase buck converter power supply.

Selecting the Input Capacitors in Buck Converters

Input Capacitors of Single-Phase Buck Converters

Figure 11 shows the input current of a buck converter is discontinuous. The input voltage source is unable to support rapid current changes. The input capacitor (CIN) supplies this changing current to the inductor and switch. Thus, CIN keeps the input voltage steady. Thus, the DC component of the switch current (ISW) is supplied by the input voltage source while the AC RMS component is supplied by the input capacitor. The switch RMS current is:

$$I_{SW(RMS)} = I_L \sqrt{D\left(1+\frac{LIR^2}{12}\right)}$$

where:

I_L = Average inductor/output current

LIR = Inductor ripple current ratio

D = Duty cycle

Similarly, the RMS current of the inductors and diode are:

$$I_{D(RMS)} = I_L \sqrt{(1-D)\left(1+\frac{LIR^2}{12}\right)}$$

$$I_{L(RMS)} = I_L \sqrt{\left(1+\frac{LIR^2}{12}\right)}$$

The RMS current of the input capacitor is the RMS of the AC current flowing through it as no DC current passes through it. The DC component of the switch current is provided by the input voltage source, while the AC component is provided by the input capacitor. The RMS current of the input capacitor ($I_{CIN(RMS)}$) is:

$$I_{CIN(RMS)}^2 = I_{SW(RMS)}^2 - I_{SW(AVG)}^2$$

The average switch current ($I_{SW(AVG)}$) is supplied by the input voltage source, which is $I_{IN} = D \times I_{OUT}$. Thus, the input capacitor RMS current is:

$$I_{CIN(RMS)} = I_{OUT} \sqrt{D\left[1-D+\frac{LIR^2}{12}\right]}$$

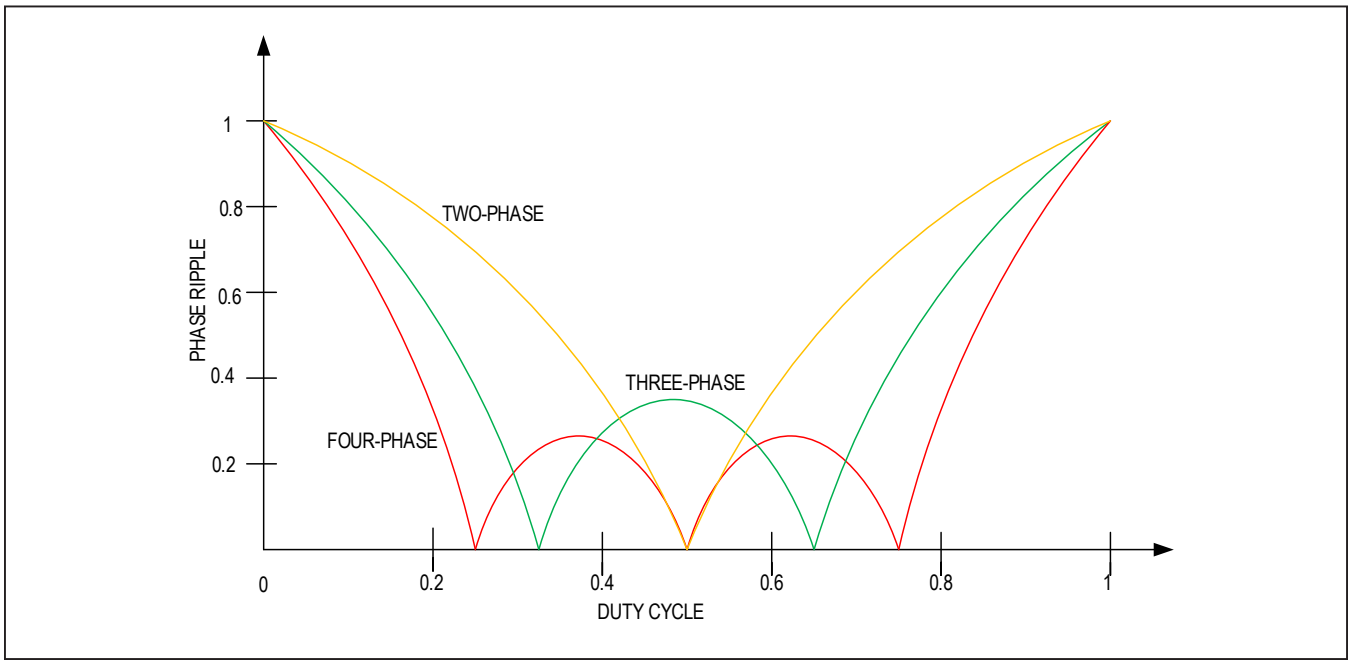

Figure 10. Duty cycle vs. output voltage ripple.

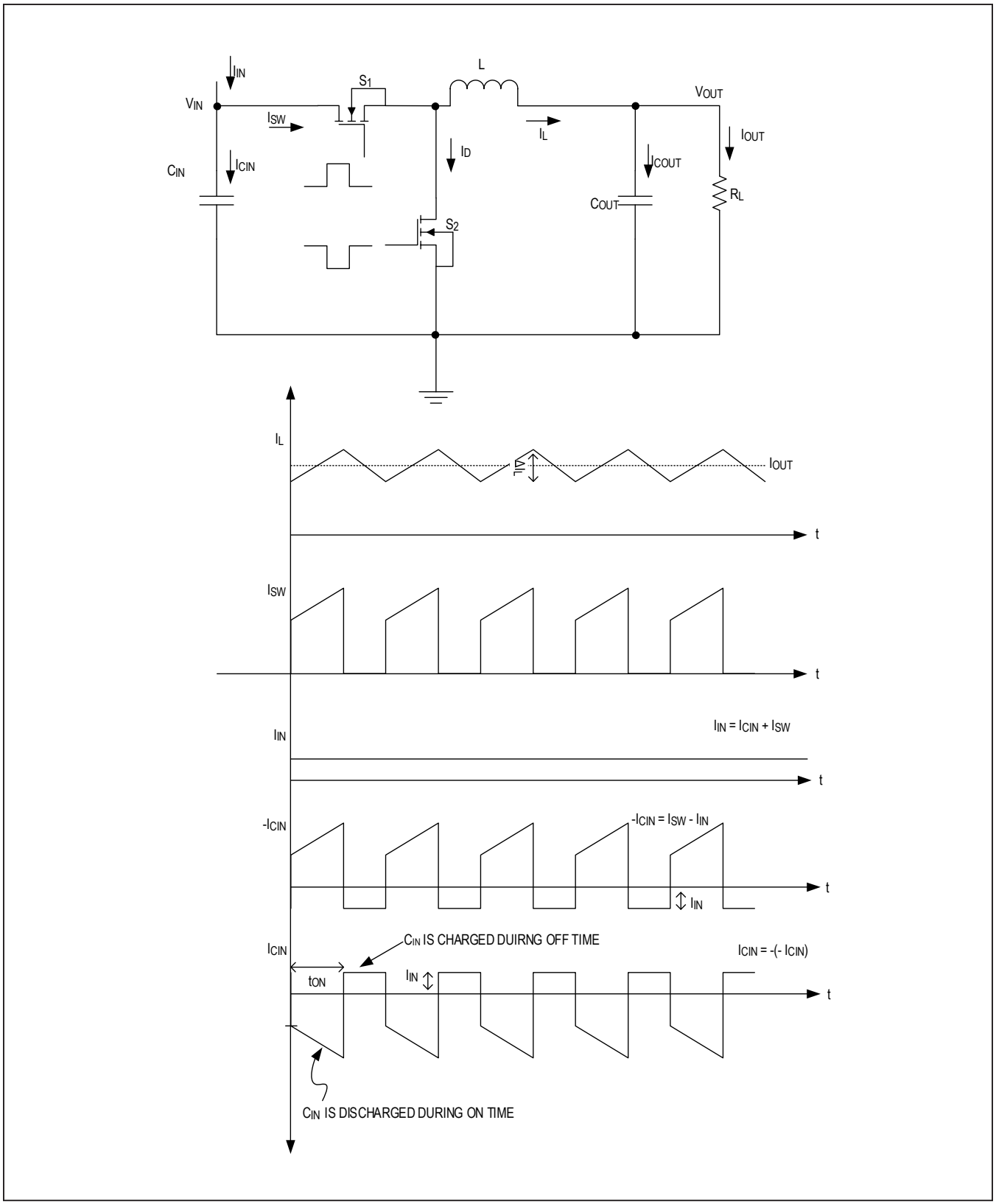

Figure 11. Current in single-phase buck converter input capacitor.

The input current (I_{IN}) supplied by the DC input source (V_{IN}) is:

$$I_{IN} = \frac{P_{IN}}{V_{IN}} = \frac{P_{OUT}}{\eta \times V_{IN}} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}}$$

The current from the input voltage source is used to charge the input capacitor during t_{OFF}. Therefore, it becomes:

$$C_{IN} \times \frac{\Delta V_{CIN}}{(1-D)t} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}}$$

$$C_{IN} = \frac{I_{OUT} \times D(1-D)}{\eta \times \Delta V_{CIN} \times f_{SW}}$$

where:

η = Efficiency

ΔV_{CIN} = Input voltage ripple

The input voltage ripple expression is:

$$\Delta V_{CIN} = \frac{I_{OUT} \times D(1-D)}{\eta \times C_{IN} \times f_{SW}}$$

The input voltage ripple depends on the duty cycle. The duty cycle at which the maximum ripple occurs is:

$$\frac{dV_{CIN}}{dD} = 0$$

$$D(0-1) + (1-D) = 0$$

$$1 - 2D = 0$$

$$D = 0.5$$

Thus, the input voltage ripple and input RMS current drawn from the input capacitor are maximum at a duty cycle of 0.5 for a single-phase buck converter (Figure 12).

Input Capacitors of Multiphase Buck Converters

The selection of input capacitors in buck converters is governed by the input RMS current requirement. This is an important parameter and scales linearly with the increase in the output current of the converter. The interleaving of phases in multiphase buck converters greatly reduces the RMS current requirement compared to a standalone buck converter with the same power level. Interleaved phases use the same input capacitor to draw individual input phase currents one after the other compared to drawing a higher amount of current when the phases are running together. This reduction in RMS current requirement leads to smaller values of capacitors required for the design, which in turn leads to a more compact and efficient power supply design.

Thus, the input ripple RMS current reduces in multiphase (Figure 13). The magnitude of the input ripple current is half that of the single-phase solution in the two-phase instance because each phase is only carrying half the load current.

The second phase does not draw current until the first phase stops its conduction and vice versa when a two-phase buck converter is running at a duty cycle of 50%. Therefore, at 50% duty cycle, the changeover takes place, and theoretically at D = 0.5 there is no RMS current requirement for the converter. The second converter starts drawing current as soon as the first converter stops drawing current. Thus, the net input current DC has no

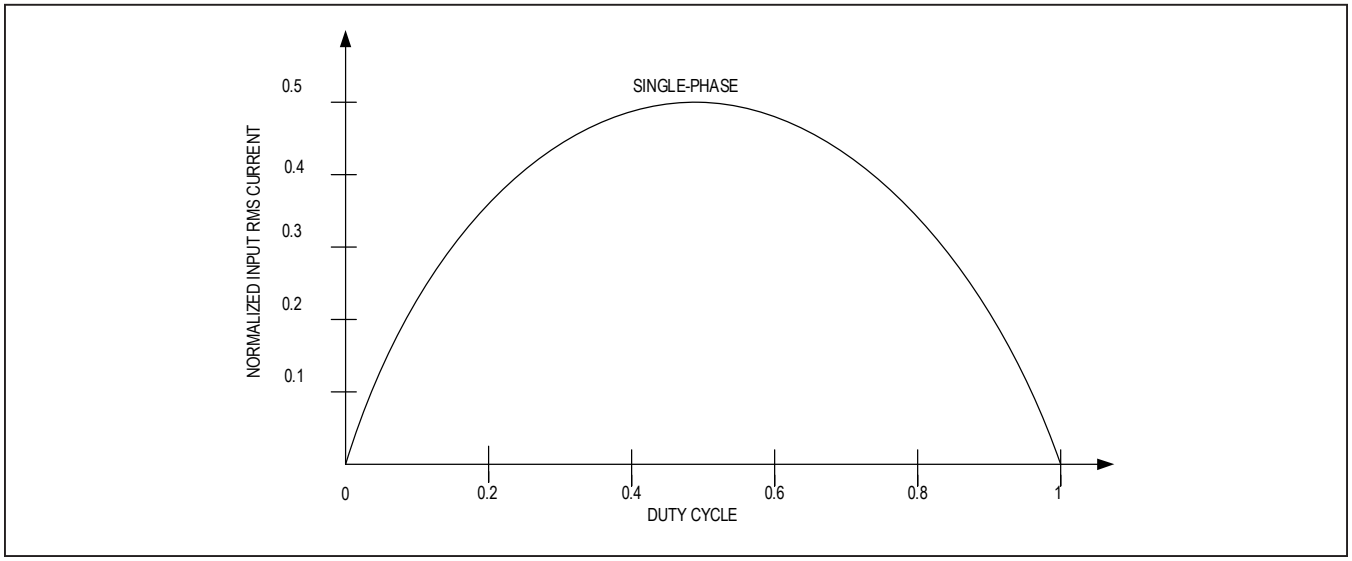

Figure 12. Duty cycle vs. input RMS current for a single-phase buck converter.

or very little RMS content. Similarly, the input RMS current requirement is zero at a duty cycle of 33.33% for a three-phase converter and at a duty cycle of 25% for a four-phase converter (Figure 14). Thus, the requirement of input RMS current stress for input capacitors greatly reduces in interleaved converters, and they are even theoretically zero at certain duty cycles.

The input RMS current requirement for a multiphase converter is:

$$I_{CIN(RMS)} = I_{OUT}\sqrt{\left[D - \frac{M}{N}\right]\left[\frac{1+M}{N} - D + \frac{LIR^2}{12}\right]}$$

where:

N = Number of phases

M = Floor (N x D)

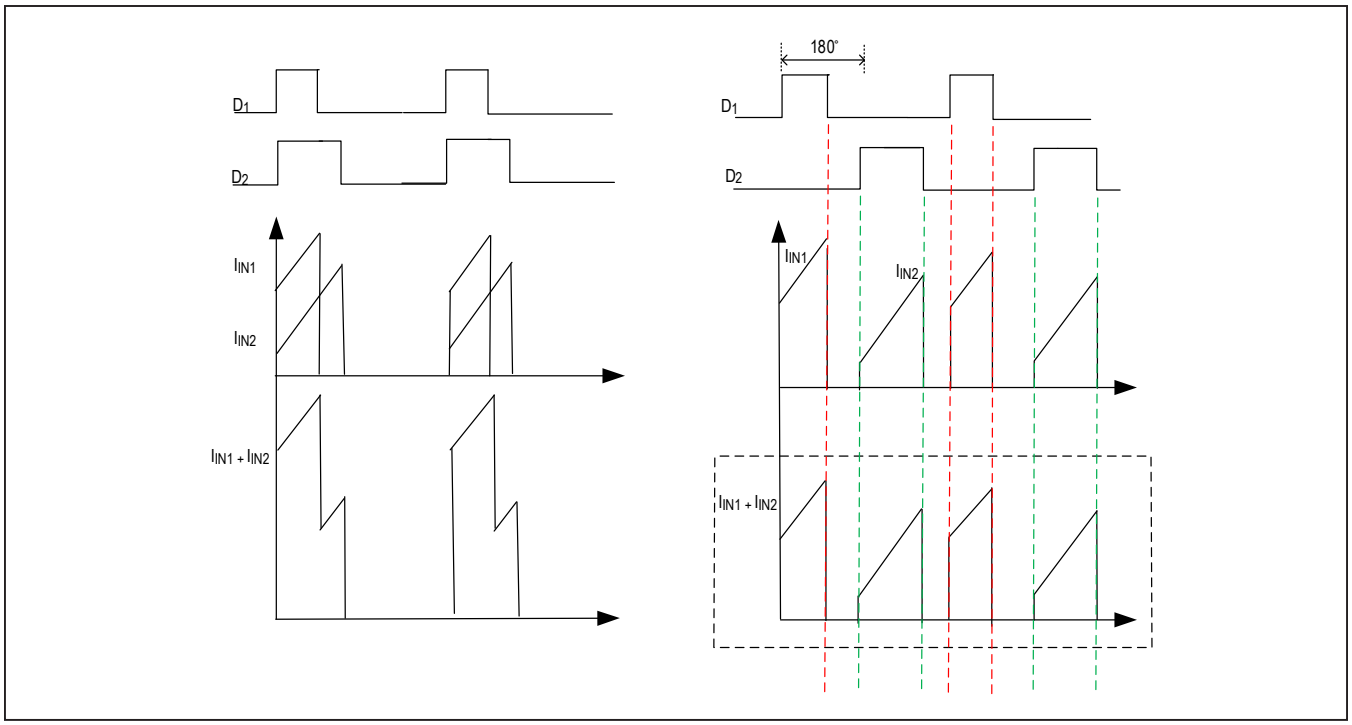

Figure 13. Interleaved phases in multiphase bucks reduce stress on the input capacitor.

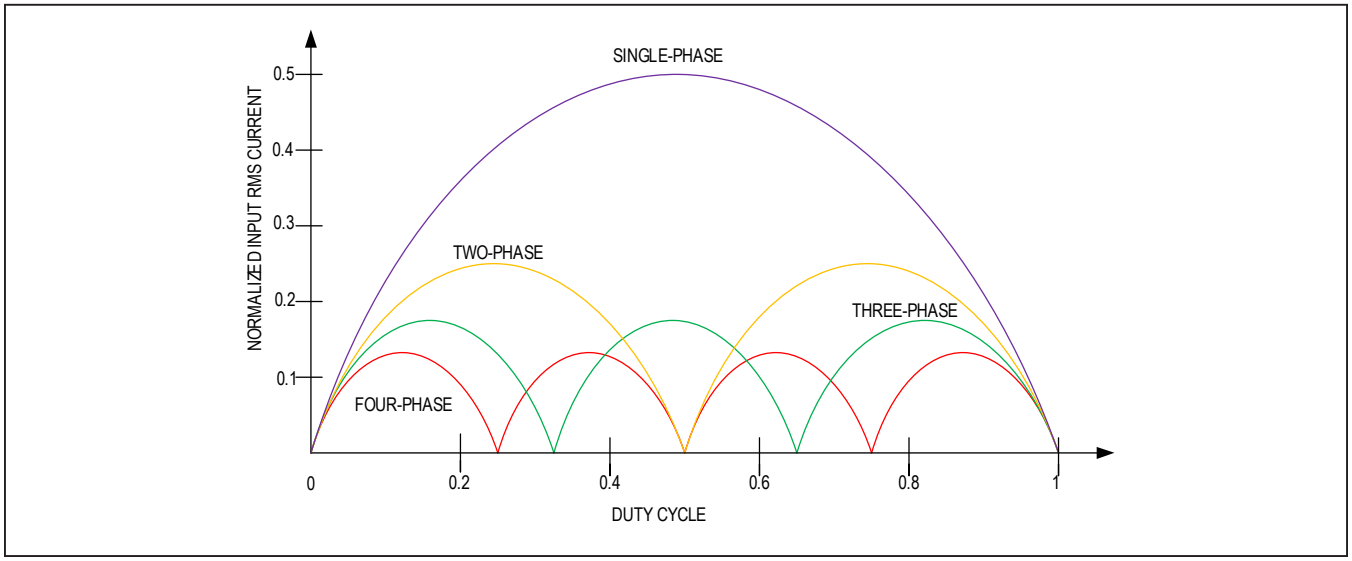

Figure 14. Duty cycle vs. input RMS current for single/multiphase buck converters.

Selecting the Inductor in Buck Converters

Inductors of Single-Phase Buck Converters

The expression for inductor selection of a buck converter (Figure 15) is calculated from the following inductor voltage expression:

$$V_L = L\frac{\Delta I_L}{\Delta t}$$

The voltage induced in the inductor is V_{IN} - V_{OUT} during t_{ON}. Thus, it is:

$$V_{IN} - V_{OUT} = L\frac{\Delta I_{L(ON)}}{t_{ON}}$$

Similarly, the voltage induced in the inductor is V_{OUT} during t_{OFF}. Thus, it is:

$$V_{OUT} = L\frac{\Delta I_{L(OFF)}}{t_{OFF}}$$

$$= L\frac{\Delta I_{L(OFF)}}{[1-D]t}$$

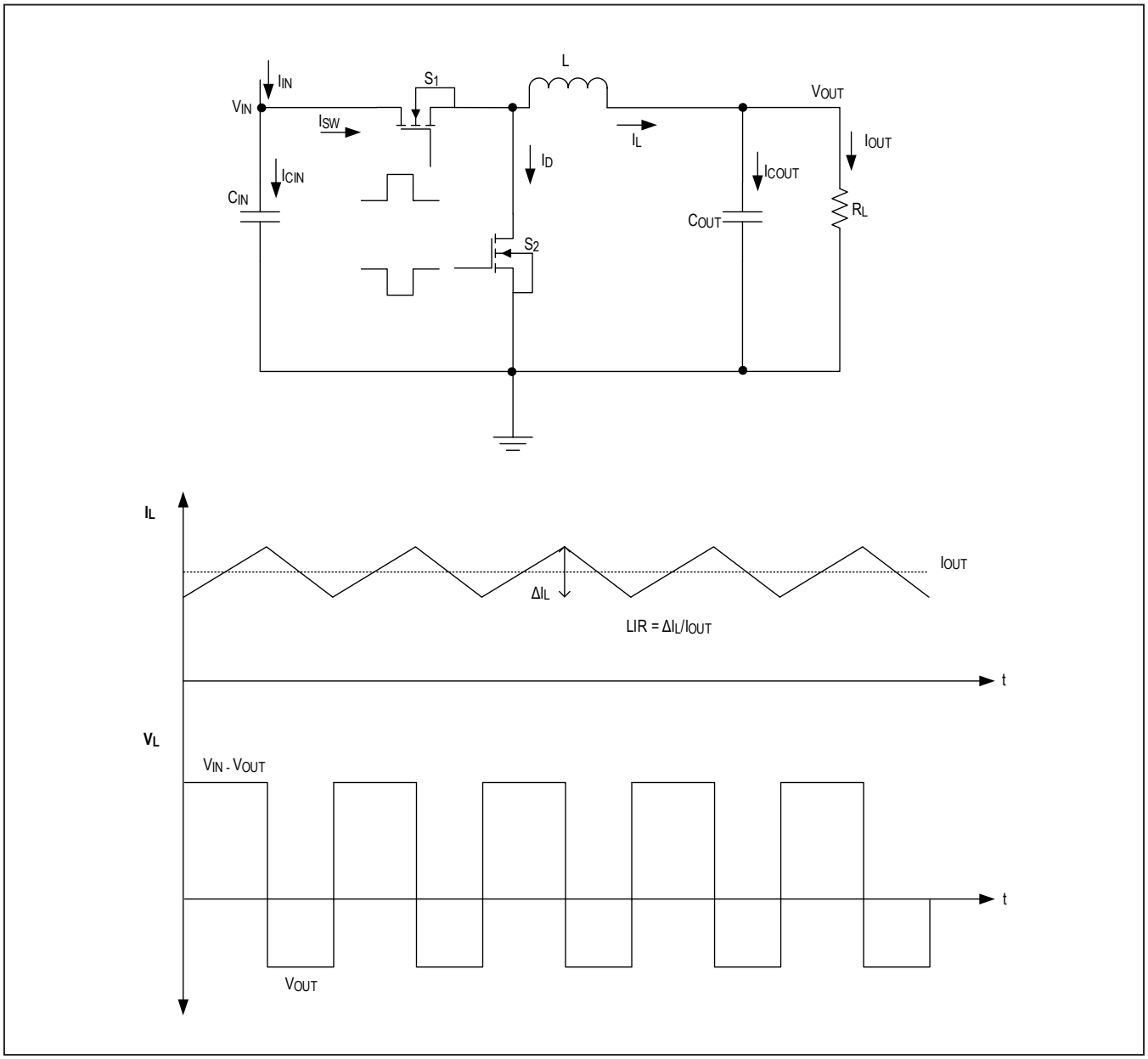

Figure 15. Inductor voltage and current for a buck converter.

The expression of the inductor (L) per the previous equation is:

$$L = \frac{[1-D]V_{OUT}}{\Delta I_{L(OFF)} \times f_{SW}}$$

The above expression in terms of LIR is:

$$L = \frac{[1-D]V_{OUT}}{LIR \times I_{OUT} \times f_{SW}}$$

Another important parameter of the inductor is the peak inductor current ($I_{L(PEAK)}$) (Figure 16). The peak current that flows through the inductor is:

$$I_{L(PEAK)} = I_{OUT} + \frac{\Delta I_L}{2}$$

Similarly, the valley inductor current ($I_{L(VALLEY)}$) is:

$$I_{L(VALLEY)} = I_{OUT} - \frac{\Delta I_L}{2}$$

Inductors of Multiphase Buck Converters

The inductor value, derived previously, is inversely proportional to the load current. The other parameters are unchanged. The required inductor's value must be halved to retain the same LIR for the same frequency and output voltage if the load current is doubled (power-supply scaling). The output voltage ripple is much lower than the individual phase inductor current ripple in multiphase buck converters due to interleaving. Therefore, for a given output voltage ripple, the LIR of the individual phases is increased (use phase inductors with smaller inductances as LIR is inversely proportional to L) to further optimize the size of the inductors used.

Thus, the interleaving of phases can greatly decrease the size of the input and output capacitors. A reduced value of the output capacitor makes the loop response of the power supply faster as the LC filter charges and discharges faster. It responds to sudden load changes more effectively and efficiently.

Current Balance in Multiphase Buck Converters

The assumption so far is that the output load current is divided equally among all the phases of a multiphase buck converter. However, this is not correct because the tolerance variations of components, doping irregularities of MOSFETs, and different layout tracks lengths among different phases cause one or more phases to draw more current than the others. This is called phase-current imbalance, which can lead to detrimental consequences for the power supply. There is a risk of inductor saturation, localized hotspots, thermal imbalance, and efficiency degradation issues because one or more phase inductors draw more current than others.

The phase imbalance problem (Figure 17) is addressed with per phase current balance networks in multiphase buck converters. The basic principle is to sense the current in each phase and force the currents in individual phases to be equal using the current feedback.

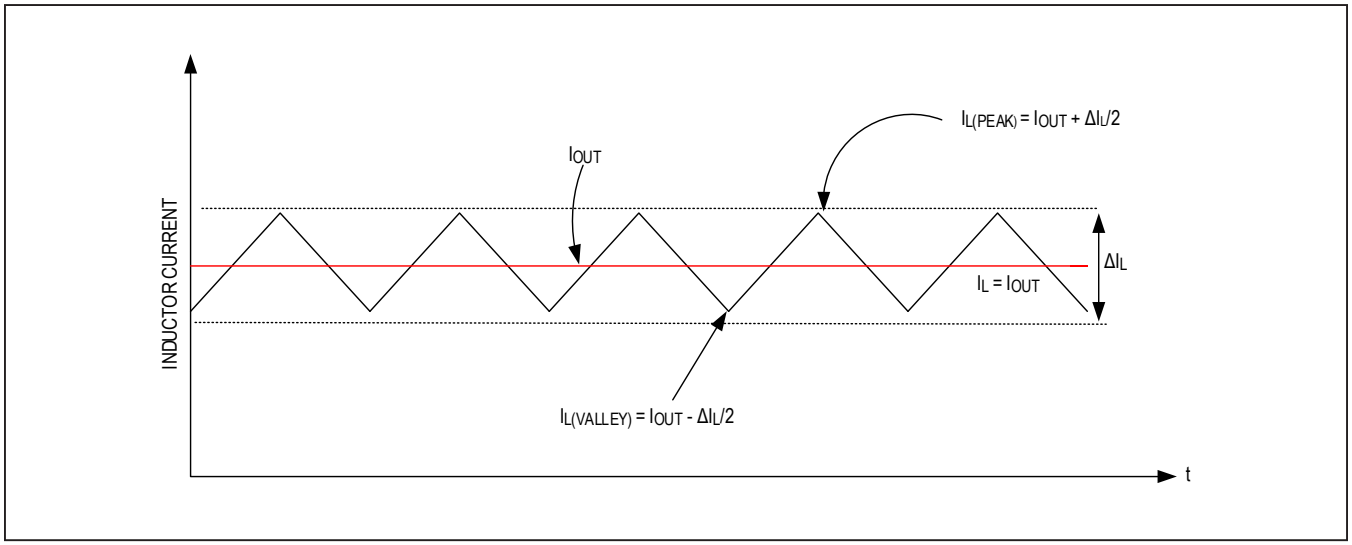

Figure 16. Inductor current of a buck converter.

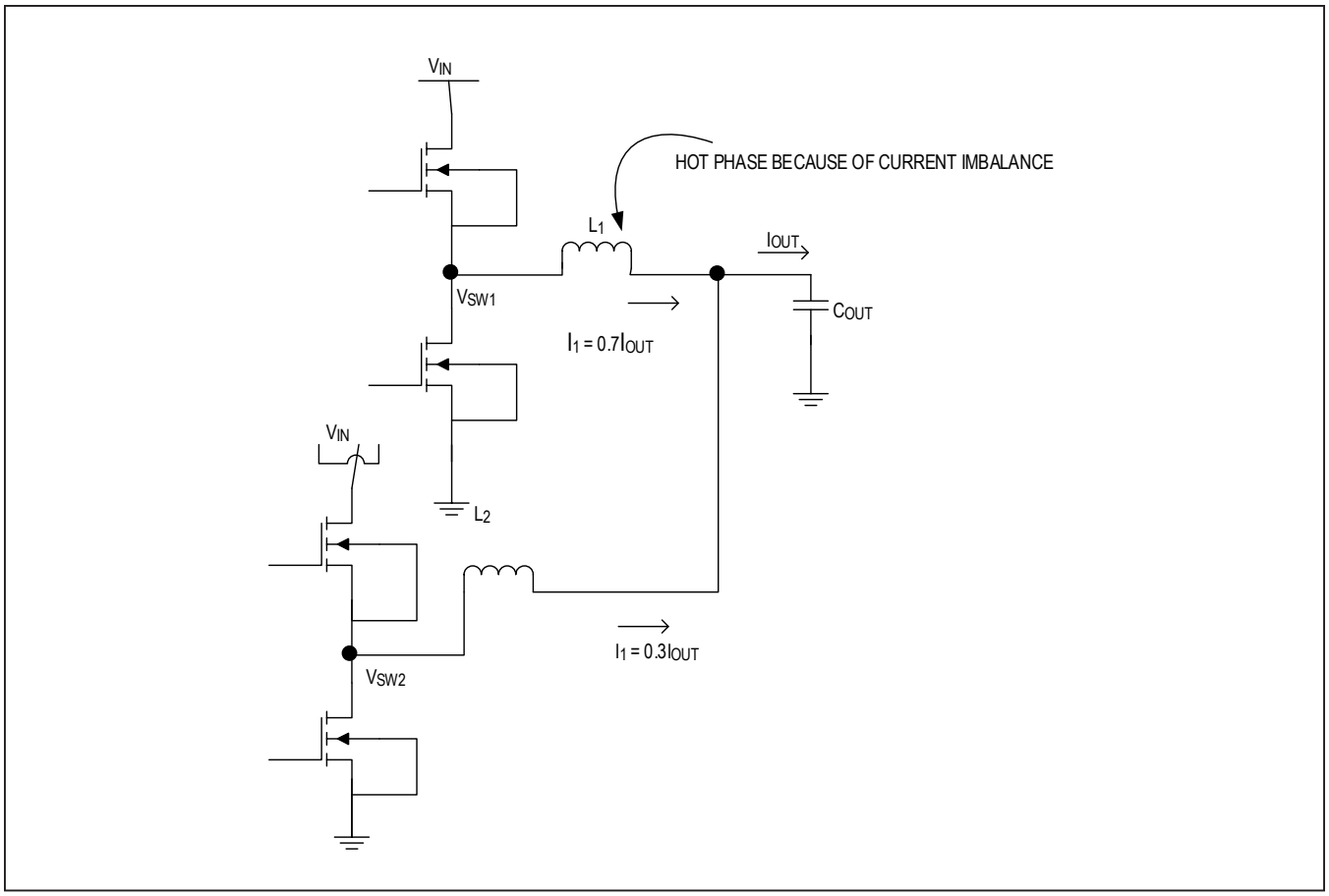

Figure 17. Current imbalance in a typical two-phase buck converter.

Multiphase Synchronous Buck Converter Using the MAX15157B

Multiphase Analog Connection in the MAX15157B

The number of required MAX15157Bs is equal to the number of phases for multiphase operations. One of the devices acts as a master phase while the others act as slave phases. The master and slaves are connected through multiple analog lines (Figure 18). Connect the SYNCIN output of the master to the FREQ/CLK signals of all the slave devices for proper synchronization between the phases in a multiphase configuration. The SYNCIN of the master device acts as a master clock. Also, the interleaved phase control is communicated by connecting the SYNCOUT signal to the SYNCIN input of the next phase. The daisy-chained signal ensures that the phases run out of phase. The phase setting communicates the frequency at which the master SYNCIN signal must run, and the clock count needed to maintain the out-of-phase operation. The 4V6 pin of the master must be connected to the EN pins of all the slaves. The CSIOP pins of the master and all the slave phases must be connected. Similarly, the CSION pins of the master and all the slave phases must also be connected. The REFIN pins of all the slaves must be connected to the SS pin of the master. The COMP pins of all the slaves must be connected to the COMP pin of the master using a gain resistor (R_{GAIN}) with a parallel RC network. The FB pins of the slave phases must be connected to their corresponding 4V6 pins. The SS pin of all the slave phases must be left unconnected. The PHASE pins of all the devices must be grounded through a resistor.

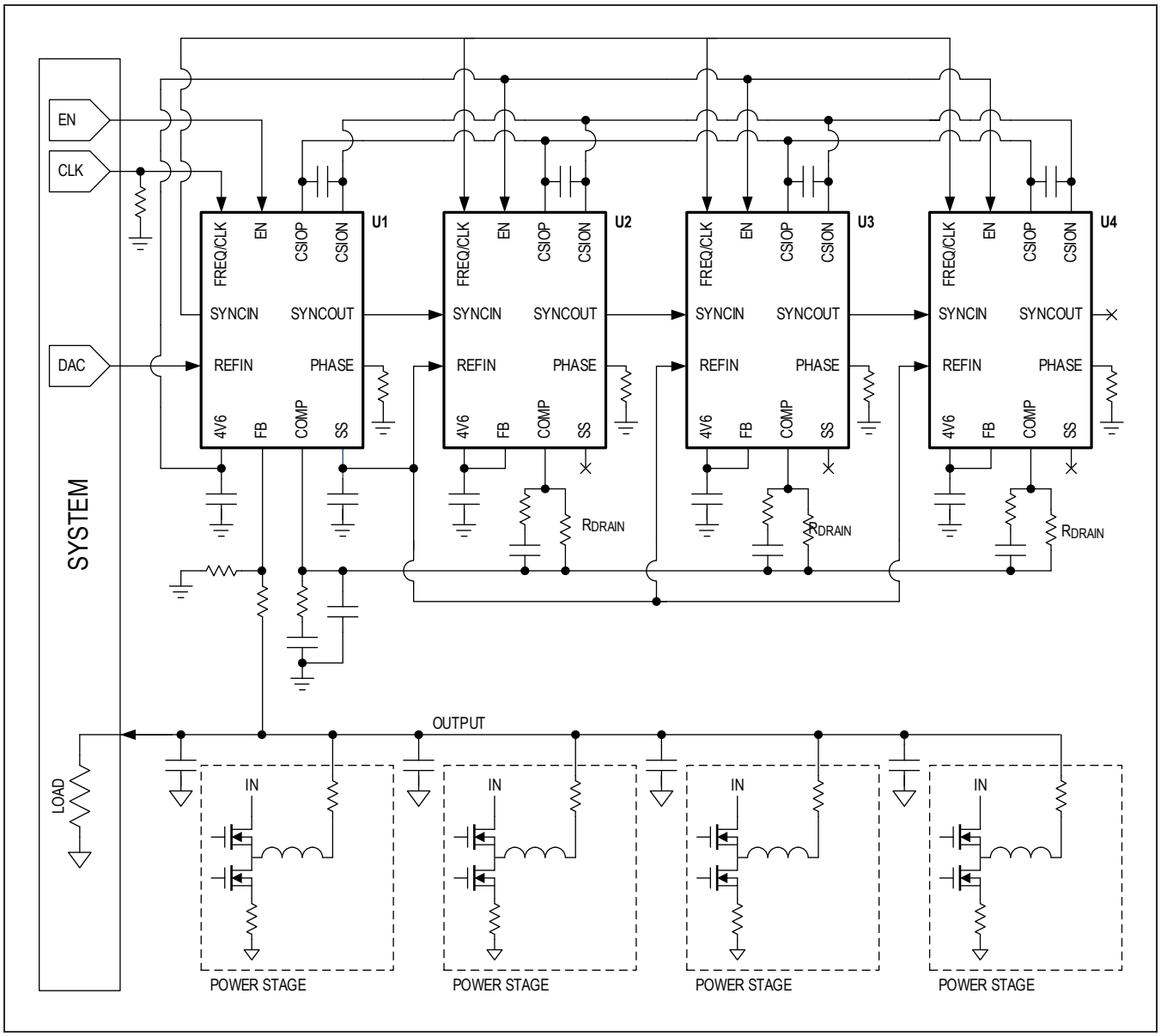

Figure 18. Connections to operate two or more MAX15157B devices in a master/slave configuration for multiphase operations.

Multiphase Current Balance Network

The MAX15157B uses the differential CSIOP and CSION connections at startup to configure the multiphase configuration. The differential interconnect communicates the average per-phase current of each regulator once this configuration period is complete. The current-mode slave devices regulate their current so that all phases share the output load.

The COMP pins of the master and slave phases must be connected through R_{GAIN} in a multiphase operation. A current balance network gain of 100 is recommended. A 25kΩ resistor is used to achieve this. The higher the value of this resistor, the higher the current balance gain. However, it is not desirable to set the gain too high, as it slows down the current loop response and the power supply responds slowly during load-transient events. It is advisable to use a RC network in parallel with the R_{GAIN} if a very high gain is required (i.e., a very high value of R_{GAIN}). Set the cut-off frequency of the RC network to 5kHz to ensure a high DC gain with a desirable low gain at higher frequencies.

Design Procedure for Dual-Phase Buck Converter Using the MAX15157B

Step 1. Selecting the Switching Frequency

The selection of the switching frequency involves a trade-off between the efficiency and component sizes. Low-frequency operation increases efficiency by reducing the MOSFET-switching losses and gate-drive losses, but it requires a larger inductor and/or capacitor to maintain a low output ripple voltage.

The switching frequency of the device can be programmed between 120kHz to 1MHz using the FREQ/CLK pin. The preset switching frequency of 150kHz was selected for this design. A resistor (R_{FREQ}) is connected between the FREQ/CLK pin and analog ground (AGND) for the other values of frequencies. Use the following formula to find the required resistor for a given switching frequency:

$$f_{SW} = \frac{R_{FREQ} \times 600}{100k\Omega} kHz$$

A standard 24.9k resistor is connected to the FREQ/CLK pin to ground.

Step 2. Selecting the Phase Inductor

Specify three key inductor parameters to select the output inductor:

- Inductance (L)
- Inductor saturation current (ISAT)
- DC resistance of inductor (DCR)

The rated current per phase for this design is 25A. However, the maximum current drawn per phase is equal to 30A. The required per phase inductance (L) is calculated based on the LIR of the inductor's peak-to-peak ripple AC current to its DC average current. An LIR of 0.3 was selected for this design. The selected LIR, f_{SW}, V_{IN}, and V_{OUT} then determine the inductor value as:

$$L = \frac{V_{OUT} \times (1 - D)}{LIR \times I_{LOAD} \times f_{SW}}$$

Output D, which is equal to the ratio of V_{OUT} and V_{IN}, varies from 0.2 (at V_{INMAX}) to 0.342 (at V_{INMIN}) depending on the variation in the input voltage range. Substituting these in the inductor value equation gives the minimum and maximum values of inductance for the output as:

$$5.84\mu H \le 6.67\mu H \le 7.11\mu H$$

L = 6.8µH for all the phases. The minimum inductor saturation current must be equal to or greater than the maximum inductor peak current given as:

$$I_{L(PEAK)} = I_{OUT} + \frac{\Delta I_L}{2}$$

$\Delta I_{LPK-PK(MAX)}$ is the maximum inductor ripple current (Figure 19) that flows at the maximum input voltage (V_{INMAX}) and is calculated as:

$$\Delta I_{LPK-PK(MAX)} = \frac{V_{OUT} \times \left[1 - \frac{V_{OUT}}{V_{INMAX}}\right]}{L \times f_{SW}}$$

The maximum inductor ripple currents $\Delta I_{LPK-PK(MAX)}$ for the output is:

$$\Delta I_{LPK-PK(MAX)} = \frac{12V \times \left[1 - \frac{12V}{60V}\right]}{6.8\mu F \times 150kHz} = 9.4A$$

The peak inductor current ($I_{L(PEAK)}$) is:

$$I_{L(PEAK)} = 30A + \frac{9.4A}{2} = 34.7A$$

6.8µH dual-stacked inductors 7443642724068D from Wurth Electronics® were selected. These are two 6.8µH inductors in one package, which ensure a compact and efficient PCB board design. Two of these packages were used for four phases.

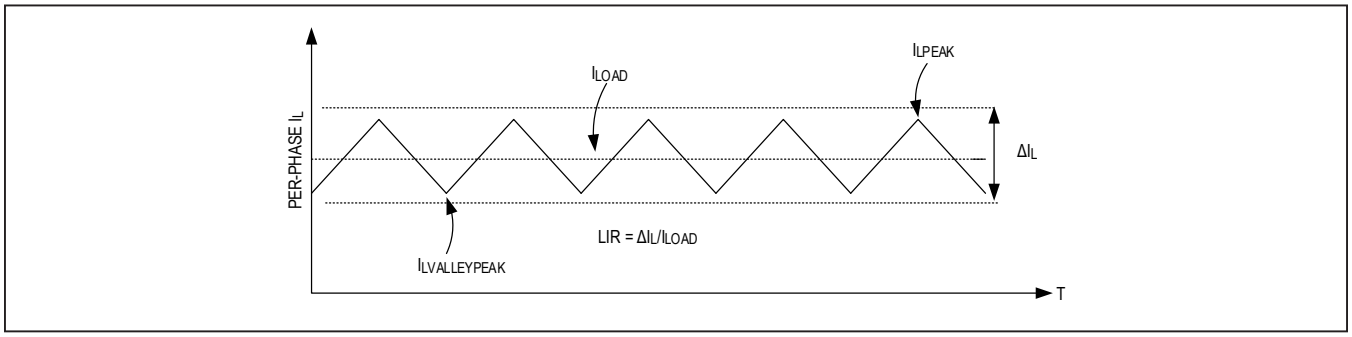

Figure 19. Inductor current of a typical buck converter.

Wurth Electronics is a registered trademark of Wurth Electronics, Incorporated.

Step 3. Selecting the Current-Sense Resistor

Selecting the Low-Side, Current-Sense Resistor (RCSL)

The control loop uses a valley current-mode architecture to optimize performance with low-duty cycles and provides the shortest possible minimum on-time. Figure 20 shows the low-side, current sense circuit parameters. The peak valley current per phase ($I_{L(VALLEYPEAK)}$) is:

$$I_{L(VALLEYPEAK)} = 30A - \frac{9.4A}{2} = 25.3A$$

The controller drives the DL pin high on the low-side MOSFET at each clock edge. The controller pulls DL low and drives DH high when the PWM comparator detects that the amplified, low-side, current-sense signal (CSLP to CSLN) and slope compensation are below the COMP voltage. An external current-sense resistor R_{CSL} senses the current for both the phases. The cycle-by-cycle current-limit threshold is 36mV. The low-side, current-sense resistor for both the phases is:

$$R_{CSL} = \frac{V_{CSL(THRESHOLD)}}{I_{L(VALLEYPEAK)}}$$

$$= \frac{36mV}{25.3A} = 1.42m\Omega$$

R_{CSL} is 1mΩ. Two 2mΩ, 1W current-sense resistors are used in parallel as R_{CSL} for both the phases.

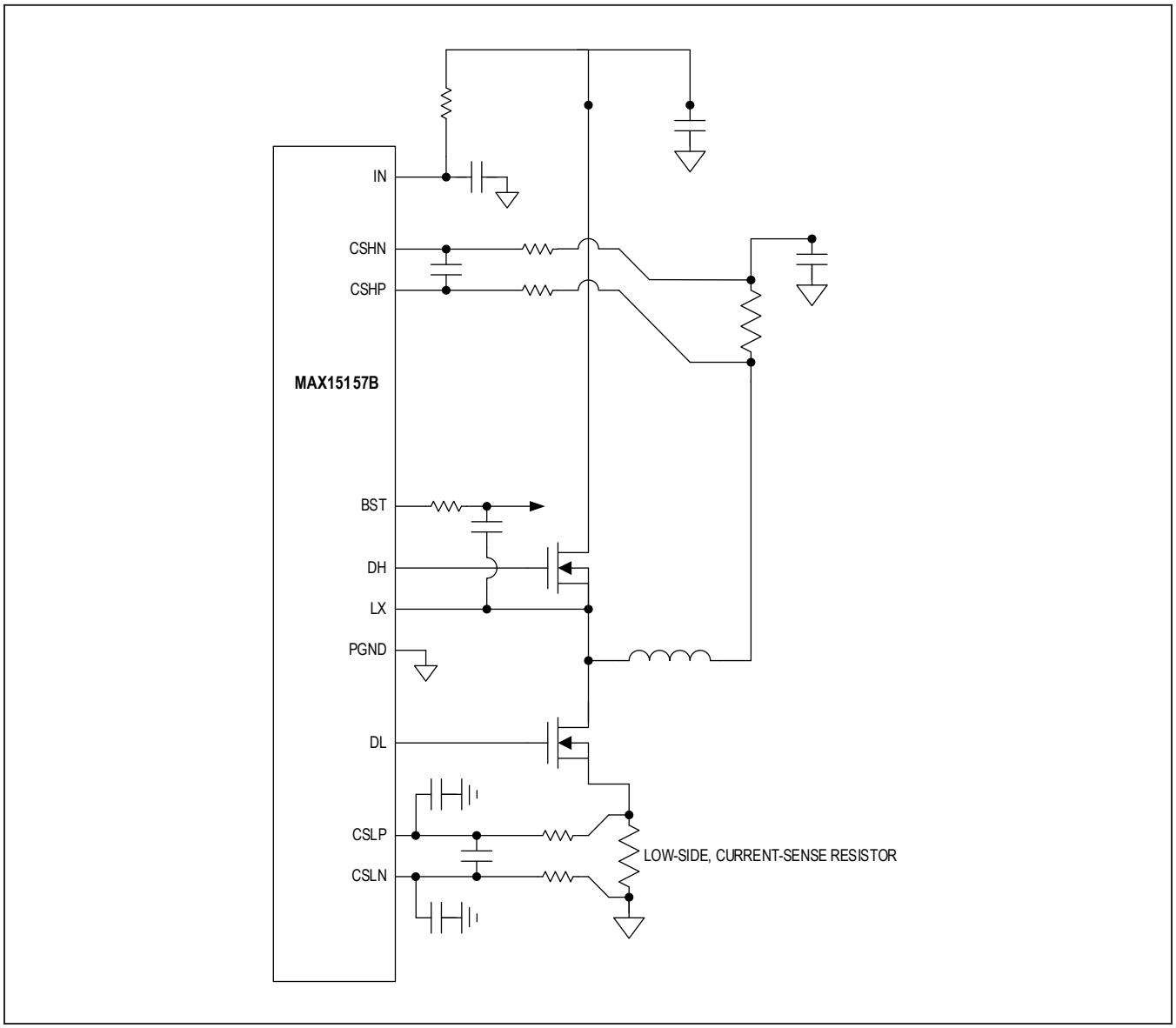

Figure 20. Low-side, current-sense network of the MAX15157B.

Selecting the High-Side, Current-Sense Resistor (R_{CSH})

The controller also includes a high-side, current-sense amplifier (Figure 21). A high-side, current-sense resistor (R_{CSH}) is used in series with the phase inductor to monitor the output current information.

The current-monitor output drives a voltage equivalent to 50x the differential CSHP-to-CSHN voltage. The current-sense amplifier only functions in a single quadrant. So, the controller only monitors the current sourced to the output. The IMON output is compared with a 2.5V threshold. The part enters the hiccup-mode once the monitored voltage exceeds 2.5V than 32 consecutive clock cycles.

The high-side, current-sense differential voltage threshold ($V_{CSH(THRESHOLD)}$) is 50mV. It is the voltage measured across the amplifier when the absolute maximum current (I_{MAX} = 30A in this design) flows through the phase inductor. The high-side, current-sense resistor for both the phases are:

$$R_{CSH} = \frac{V_{CSH(THRESHOLD)}}{I_{MAX}} = \frac{50mV}{30A} = 1.66m\Omega$$

R_{CSH} is 1.66mΩ. Three 5mΩ, 1W current-sense resistors are used in parallel as R_{CSH} for both the phases..

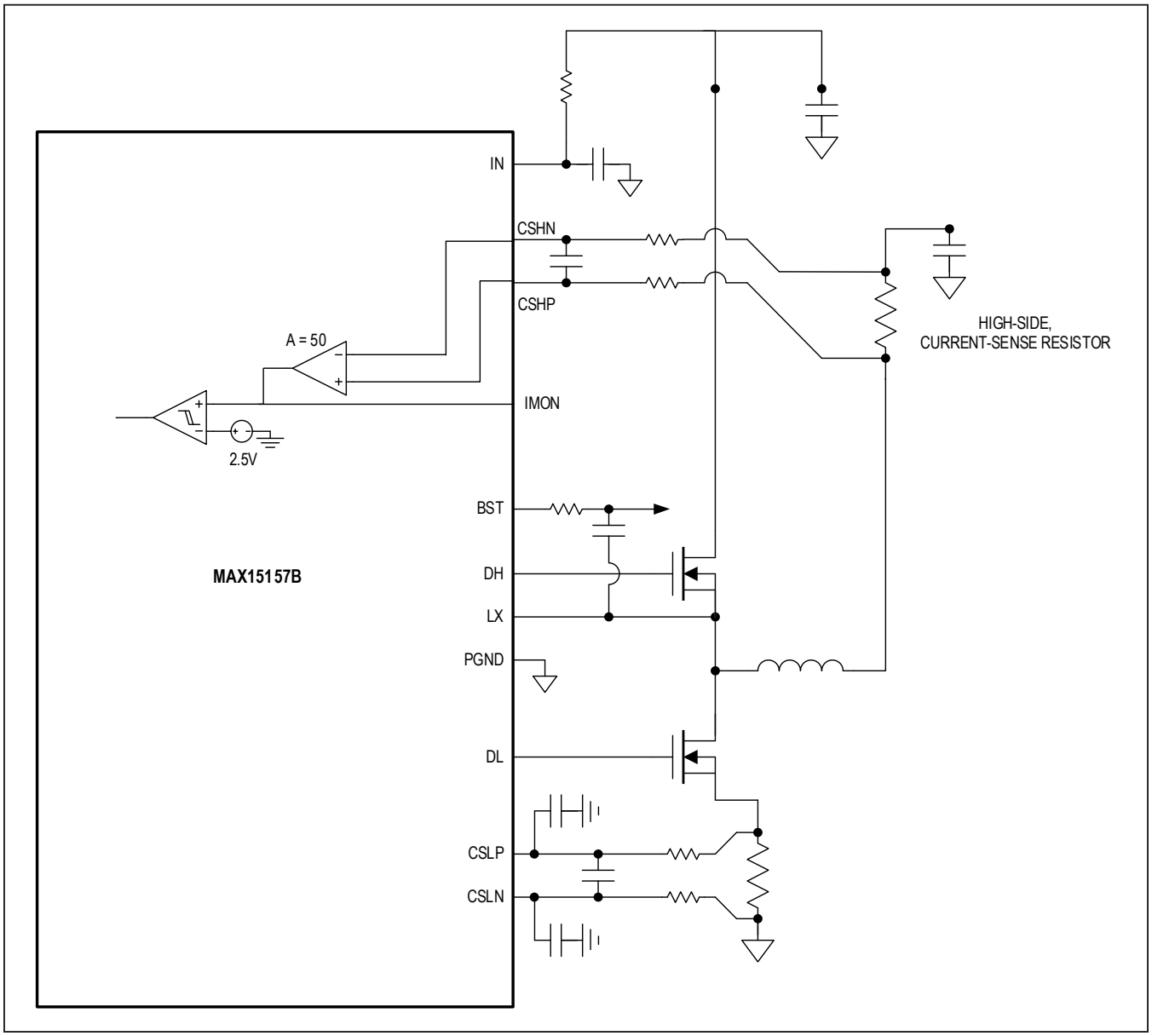

Figure 21. High-side, current-sense network of the MAX15157B.

Step 4. Programming the Output Overvoltage

The MAX15157B has three separate overvoltage protection (OVP) comparators. The first monitors the FB voltage, second the high-side, current-sense input (CSHN), and third the independent OVP input. The feedback (FB) overvoltage comparator trips if the feedback voltage exceeds the SS voltage by 9% (typ) for more than 20µs. The high-side, current-sense overvoltage comparator trips if the current-sense voltage exceeds 65V, which is the operating limit of the regulator and current-sense amplifier. Finally, the OVP comparator (Figure 22) trips if the output voltage exceeds the set overvoltage threshold (V_{OV}).

The output voltage overvoltage threshold (V_{OV}) is 15V in this design. R_2 is 10kΩ and R_1 is:

$$R_1 = \left[\frac{V_{OV}}{2} - 1\right] \times R_2$$
$$= \left[\frac{15V}{2} - 1\right] \times 10k\Omega = 65k\Omega$$

A typical resistor of 64.9kΩ is selected as R_1.

Step 5. Setting the Output Voltage

The output voltage is set by connecting the center node of a resistor-divider network between the output voltage and ground to the FB pin of the master phase (Figure 23). R_4 is 10kΩ and R_3 is:

$$R_3 = \left[\frac{V_{OUT}}{2} - 1\right] \times R_4$$
$$= \left[\frac{12V}{2} - 1\right] \times 10k\Omega = 50k\Omega$$

A typical resistor of 49.9kΩ is selected as R_3.

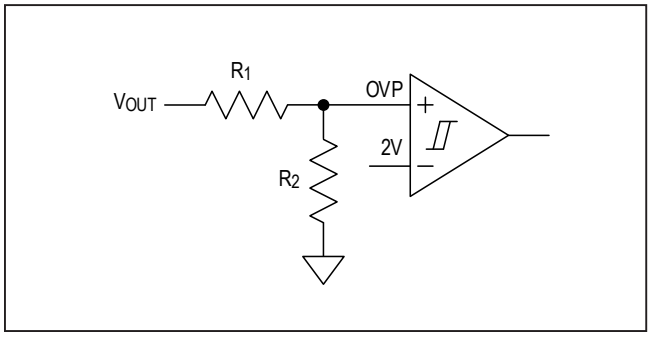

Figure 22. OVP programming of the MAX15157B.

Step 6. Setting the Input UVLO

The external UVLO sense pin allows the input voltage operating range to be externally adjusted or used for power sequence control. Either the input power source (IN) or driver supply (DRV) is monitored. The controller powers up and remains active if the UVLO exceeds and remains above 1V. The controller pulls PGOOD low, disables the drivers (all driver outputs pulled low), and discharges the SS capacitor through an internal 5Ω discharge MOSFET once the UVLO drops below 0.9V (typ).

The input operating voltage of this design is 35V, while the undervoltage lockout voltage (V_{UVLO}) is set to 32V. The UVLO voltage is set (Figure 24) by connecting the center node of a resistor-divider network between the input voltage and ground to the UVLO pin of the master and slave phases. R_6 is 10kΩ and R_5 is:

$$R_5 = \left[\frac{V_{UVLO}}{1} - 1\right] \times R_6$$
$$= \left[\frac{32V}{1} - 1\right] \times 10k\Omega = 310k\Omega$$

A typical resistor of 309kΩ is selected as R_5 for the master and slave phases.

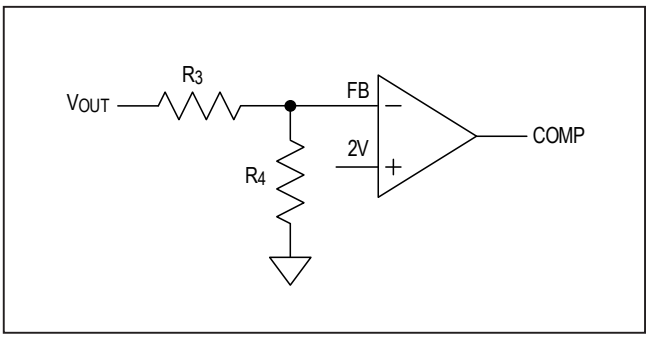

Figure 23. Output voltage programming of the MAX15157B.

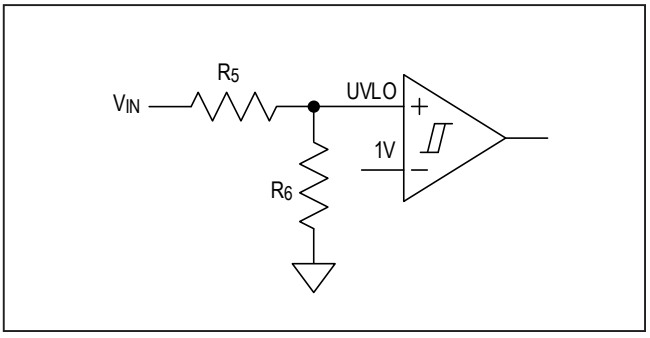

Figure 24. UVLO programming of the MAX15157B.

Step 7. Soft-Start

The soft-start/stop time of the output voltage is controlled by the voltage on the master SS pin. The device regulates the FB voltage to the SS pin voltage instead of the 2V internal fixed reference when the voltage on the SS pin is less than the 2V internal reference. The SS pin can thus be used to program the output-voltage soft-start time by connecting an external capacitor from the SS pin to the ground. The soft-start time for this design is 40ms.

The regulator charges the SS capacitor with a constant 5µA current source until the SS voltage reaches either the preset 2V target voltage (REFIN = 4V6) or the externally driven REFIN voltage (V = 0.4V to 2.2V).

The soft-start capacitor value is:

$$C_{SS} = T_{SS} \times \frac{5\mu A}{2V}$$
$$= 40ms \times \frac{5\mu A}{2V} = 100nF$$

A typical capacitor of 100nF is selected as the C_{SS} of the master phase. The SS pins of the slave phases must be left unconnected.

Step 8. Generating the Driver Power Supply (DRV) and Setting the EN Pin

The device requires an external driver supply in addition to the system input supply. The MOSFET drivers require a 5.5V to 14V supply capable of supporting the supply current needed to drive the MOSFETs. The power loss through an internal linear regulator is significant. So, the driver supply typically comes from the regulated 12V system supply. The maximum current required is determined by the f_{SW} and gate charge of each MOSFET (Q_G):

$$I_{DRV} = 2 \times f_{SW} \times Q_G$$

The total gate charge Q_G of the MOSFET in this design is 46nC. So, the minimum drive current required is:

$$I_{DRV} = 2 \times 150kHz \times 46nC = 13.8mA$$

Thus, a voltage in the range of 5.5V to 14V must be supplied externally to the DRV pin. A separate MAX15062 onboard voltage regulator is used in this design to generate a 9V output capable of supplying 300mA to the internal MOSFET drivers of the MAX15157B. Refer to the MAX15062 data sheet (or simulate in EE-Sim®) to find the part selection details for generating a 10V output with 300mA capability.

The MAX15157B has a control input called EN to enable the device. The EN pin has a rising logic threshold of 0.7V. The device is enabled by connecting the center node of a resistor-divider network between the DRV pin and ground to the EN pin of the master phase (Figure 25).

EE-Sim is a registered trademark of Maxim Integrated Products, Inc.

R_8 is 10kΩ and R_7 is:

$$R_7 = \left[\frac{DRV}{0.7} - 1\right] \times R_8$$
$$R_7 = \left[\frac{10}{0.7} - 1\right] \times 10k\Omega = 131k\Omega$$

A typical resistor of 100kΩ is selected as R_7 for the master. The EN pin of the slave phase must be connected to the 4V6 pin of the master phase.

Step 9. Slope Compensation

The MAX15157B provides a RAMP input to select the internal compensation ramp within a range of 130mV to 600mV. The device programs the minimum default value of 130mV slope compensation by shorting the RAMP pin to the analog ground. Higher values of slope compensation are achieved by connecting a resistor between the RAMP pin and analog ground. The current sourced from the RAMP pin to ground is 6µA. The selected ramp voltage is 550mV. The required resistor value is:

$$R_{RAMP} = \frac{V_{RAMP}}{I_{RAMP} \times 1.55}$$
$$= \frac{550mV}{6\mu A \times 1.55} = 59k\Omega$$

A typical resistor of 59kΩ is selected as R_{RAMP}.

Step 10. Selecting the Input Capacitor

The total input RMS current for this design is:

$$I_{CIN(RMS)} = I_{OUT}\sqrt{\left[D - \frac{M}{N}\right]\left[\frac{1+M}{N} - D + \frac{LIR^2}{12}\right]}$$

N = 4. The maximum RMS current depends on the duty cycle and peaks at D = 0.125, D = 0.375, D = 0.625, and D = 0.875 for a 4-phase buck converter. The RMS current requirement is zero at the duty cycles of D = 0.25, D = 0.5, D = 0.75, and D = 1. The duty cycle varies as follows:

D_{MIN} at 60V = 0.2

D_{NOM} at 48V = 0.25

D_{MAX} at 35V = 0.342

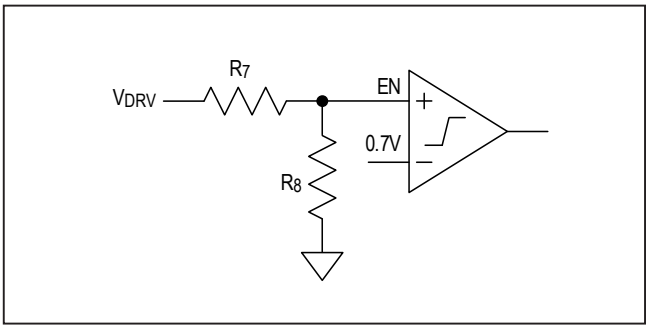

Figure 25. EN pin programming of the MAX15157B

The RMS current required at D = 0.25 is 0A, while the RMS current values at D = 0.2 and D = 0.342 are:

$$I_{CIN(RMS)@D=0.2} = 120A\sqrt{\left[0.2-\frac{0}{4}\right]\left[\frac{1+0}{4}-0.2\right]} = 12A$$

$$I_{CIN(RMS)@D=0.342} = 120A\sqrt{\left[0.342-\frac{1}{4}\right]\left[\frac{1+1}{4}-0.342\right]} = 14A$$

Thus, the input capacitor RMS current requirement per phase is 14A.

The input capacitance required for a specified input-ripple voltage (ΔV_{IN}) for each phase is:

$$C_{IN\_PHASE} = \frac{I_{OUT\_PHASE} \times D \times (1-D)}{\eta \times \Delta V_{IN} \times f_{SW}}$$

where:

η = Target efficiency

ΔV_{IN} = Allowed peak-to-peak ripple voltage

I_{OUT_PHASE} = Maximum output current per phase

The required per phase input capacitor varies from 24.06µF to 33.88µF for a target efficiency of η = 95% and ΔV_{IN} = 2% of $V_{IN(MIN)}$. The calculation for a maximum duty cycle of 0.342 is:

$$C_{IN\_PHASE} = \frac{25A \times 0.342 \times (1-0.342)}{0.95 \times 0.720V \times 150kHz} = 54.9\mu F$$

5 x 4.7µF/100V capacitors in parallel with 4 x 150µF electrolytic capacitors are used as C_{IN} for each phase considering the derating of capacitors due to component tolerances, temperature, and DC biasing.

Step 11. Selecting the Output Capacitor Selection

The key selection parameters for the output capacitor are capacitance value, ESR, and voltage rating. These parameters affect the overall stability, output ripple voltage, and transient response. The output capacitor is chosen as 3% output voltage deviation (ΔVC_{OUT} = 360mV) for a 50% load step of the rated output current (50A). The bandwidth is usually selected in the range of $f_{SW}/10$ to $f_{SW}/20$. The bandwidth is chosen as 10kHz.

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{SW}}\right) = \frac{0.33}{10kHz} + \frac{1}{150kHz} = 40\mu s$$

The required output capacitance is:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{COUT}} = \frac{50A \times 40\mu s}{2 \times 360mV} = 2777\mu F$$

22 x 22µF/25V MLCC capacitors are used along with 20 x 150µF tantalum capacitors considering the derating of capacitors due to component tolerances, temperature, and DC biasing. The worst-case capacitance of these capacitors is 2738µF. The total ESR of the output capacitors is 0.09mΩ.

Step 12. Loop Compensation for the Master Phase

The controller uses a current-mode scheme that regulates the output voltage by forcing the required current through the external inductor. The current-mode control, in the case of voltage-mode control, eliminates the double pole in the feedback loop caused by the inductor and output capacitor. It leads to a smaller phase shift and less elaborate error-amplifier compensation. Figure 26 shows a typical type II compensation.

The compensation resistor (R_Z) is:

$$R_Z = \frac{2 \times \pi \times f_{CO} \times C_{OUT} \times G_{CS} \times R_{SENSE}}{G_M \times G_{FB}}$$

where:

f_{CO} = Cut-off frequency (10kHz)

C_{OUT} = Worst-case output capacitance (2738µF)

G_{CS} = Current-sense amplifier gain (4.9)

G_M = Internal transconductance amplifier gain (1.1mA/V)

G_{FB} = Output-voltage feedback divider gain of $2/V_{OUT}$ (0.166)

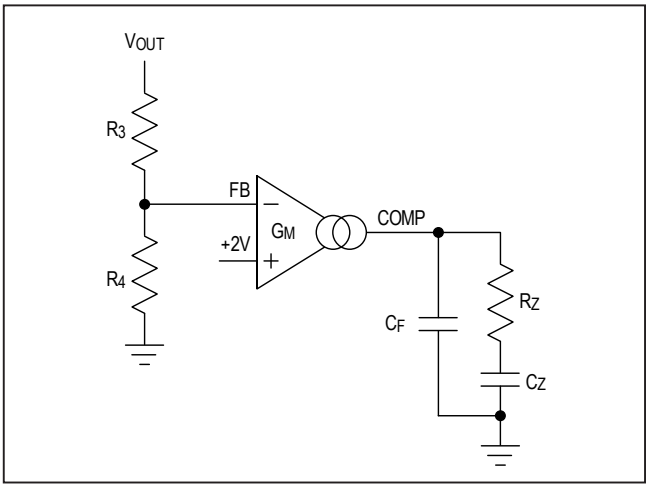

Figure 26. MAX15157B type II compensation network.

The value of R_Z is:

$$R_Z = \frac{2 \times \pi \times 10kHz \times 2738\mu F \times 4.9 \times 1m\Omega}{1.1mA/V \times 0.166} = 4.59k\Omega$$

The typical resistor value of 4.7kΩ is selected as R_Z.

f_{P_LOAD} is the load pole frequency calculated as:

$$f_{P\_LOAD} = \frac{1}{2 \times \pi \times C_{OUT} \times \frac{V_{OUT}}{I_{LOAD}}} = \frac{1}{2 \times \pi \times 2738\mu F \times \frac{12V}{100A}} = 484.2Hz$$

C_Z is calculated as (Figure 26):

$$C_Z = \frac{1}{2 \times \pi \times F_{P\_LOAD} \times R_Z} = \frac{1}{2 \times \pi \times 484.2Hz \times 4.7k\Omega} = 69.9nF$$

A typical capacitor of 68nF is selected as C_Z.

The minimum of ESR zero frequency (f_{Z_ESR}) is:

$$f_{Z\_ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times ESR} = \frac{1}{2 \times \pi \times 2738\mu F \times 0.09m} = 650.8kHz$$

Calculate C_F (Figure 26) as:

$$C_F = \frac{1}{2 \times \pi \times R_Z \times F_{P\_EA}}$$

where f_{P_EA} is the pole frequency created by R_Z and C_F. Set it to the minimum ESR zero frequency calculated above. CF for both the outputs is:

$$C_F = \frac{1}{2 \times \pi \times 4.7k\Omega \times 650.8kHz} = 451pF$$

Step 13. Selecting the External MOSFET

Each controller drives two pairs (2 x high side and 2 x low side) of external, logic-level nMOSFETs as the circuit switch elements. The key selection parameters for these MOSFETs include:

- On-resistance ($R_{DS(ON)}$)
- Maximum drain-to-source voltage ($V_{DS(MAX)}$)
- Miller plateau voltage on the high-side MOSFET gate (V_{MIL})
- Total gate charge (Q_{GATE})
- Output capacitance (C_{OSS})
- Power dissipation rating and package thermal resistance

Infineon® BSC030N08NS5 80V/100A MOSFETs are used as the high-side and low-side MOSFETs for all the four phases.

Step 14. Selecting the Bootstrap Capacitor

The selected high-side MOSFET determines the appropriate bootstrap capacitance values as:

$$C_{BST} = \frac{Q_{GATE}}{\Delta V_{BST}}$$

where:

Q_{GATE} = Total gate charge of the high-side MOSFET (46nC for the selected high-side MOSFET)

ΔV_{BST} = Voltage variation allowed on the high-side MOSFET driver after turn-on (100mV)

The minimum bootstrap capacitance value for both the outputs is:

$$C_{BST} = \frac{46nC}{100mV} = 460nF$$

A typical value of 470nF is selected as bootstrap capacitance (C_{BST}) for both the phases.

Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/20	Initial release	—