24V, 3A Average Current, 4A Peak Current Active Clamp Forward DC-DC Converter Using the MAX17599

MAXREFDES1218

Introduction

The MAXREFDES1218 is an active-clamp forward power supply that delivers up to 4A at 24V from a 18V to 36V supply voltage. It is designed for industrial equipment that needs high power isolated power supply. The typical application of the MAXREFDES1218 is an IO-Link® application that needs a 24V isolated voltage from an industrial 24V supply voltage.

The MAXREFDES1218 illustrates techniques using the active-clamp forward controller to generate isolated voltages. This document explains how the MAX17599 active-clamp forward controller can be used to generate 24V isolated voltage from 18V to 36V input voltage. An overview of the design specification is shown in Table 1.

Table 1. Design Specification

PARAMETER	SYMBOL	MIN	MAX
Input Voltage	V_{IN}	18V	36V
Switching Frequency	f_{SW}	250kHz	
Peak Efficiency	η	93%	
Duty Cycle	D	29%	60%
Output Voltage	V_{OUT}	23.76V	24.24V
Output Voltage Ripple	ΔV_{OUT}	240mV	
Output Current	I_{OUT}	0A	4A
Output Power	P_{OUT}	96W	

Designed–Built–Tested

This application note describes the hardware shown in Figure 1. It provides a detailed systematic technical guide to design an active-clamp forward DC-DC converter (ACFC) using the Maxim® MAX17599 current mode controller. The power supply has been built and tested, details of which follow in this document.

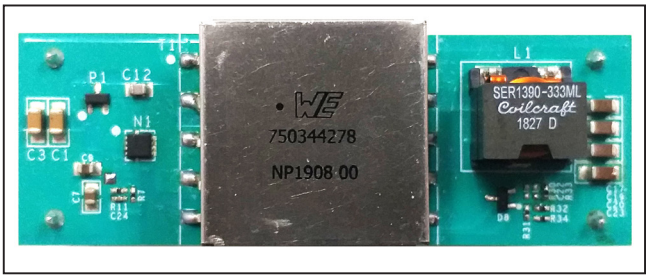

Figure 1. MAXREFDES1218 hardware.

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Active Clamp Forward Converter

Single-ended forward converters have always been a favorite of designers for single and multiple output power supplies in the range of watts to kilowatts. In this topology, a second out-of-phase winding (reset winding) is used to reset the magnetic flux in the power transformer's core while the secondary-side freewheeling diode is conducting. If the number of turns on this winding is equal to the number of turns on the main transformer's primary winding, the drain-source voltage of the main power switch is limited (excluding ringing due to leakage inductance and parasitic capacitance in the circuit) to two times the input voltage of the power supply, but so, too, is the maximum duty cycle limited to less than 50%. This duty cycle limit can be extended above 50% to improve transformer utilization by increasing the number of turns on the reset winding but only at the expense of a higher drain-source voltage (increased voltage stress and switching power losses) on the main power switch.

These and other limitations of the forward converter can easily be overcome when the designer fully understands the operation and unique benefits of the ACFC topology.

The main components of an ACFC are shown in Figure 2. The active clamp comprises a P-channel MOSFET (Q_{AUX}) and a clamp capacitor C_{CLAMP}. The difference between the traditional forward converter and the ACFC occurs when main power MOSFET (Q_{MAIN}) is off. The reset winding and diode of the traditional forward converter clamps the drain-source voltage of Q_{MAIN} to approximately twice the power supply input voltage during the first half of the interval when Q_{MAIN} is off, whereas in the ACFC the drain-source voltage of Q_{MAIN} will be clamped to an intermediate voltage between V_{IN} and 2 V_{IN} for the full interval when Q_{MAIN} is off.

The benefits of the ACFC topology go far beyond reducing the voltage stress on the main power MOSFET and increasing the duty cycle limit.

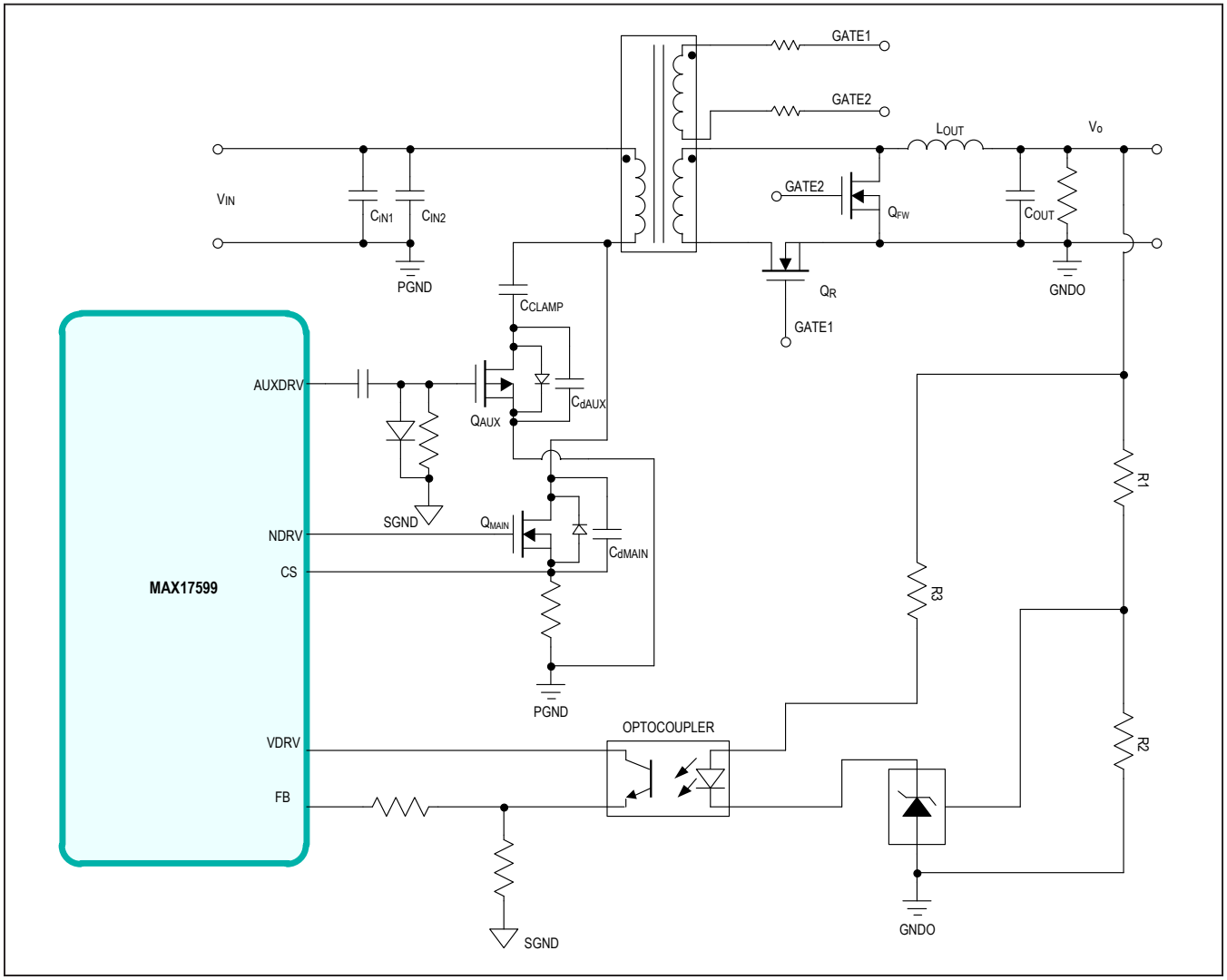

Figure 2. ACFC topology.

Further benefits provided by the ACFC topology are as follows:

- Zero voltage switching (ZVS) can be achieved for Q_{MAIN} and Q_{AUX} over the full load range by careful design, thus significantly improving power supply efficiency.
- A smaller output inductance can be used due to higher operating duty cycle.
- Operating at a duty cycle higher than 50% allows a higher secondary-to-primary turns ratio on the transformer leading to a lower reflected current from the secondary to primary, and thus a lower peak current in the main power MOSFET.
- Lower EMI due to the ZVS nature of the switching.

Figure 3 shows the main steady state waveforms of the ACFC.

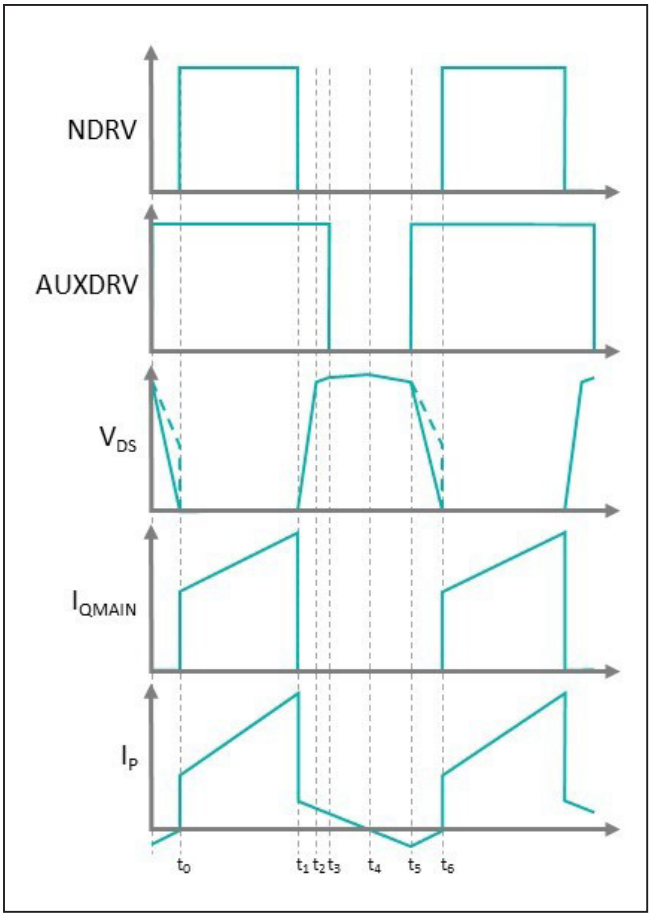

Figure 3. ACFC waveforms.

It is important to understand what is happening during one complete switching cycle of the converter. The table below describes what occurs at each time interval of the switching cycle.

INTERVAL	DESCRIPTION
t_0 - t_1	Q_{MAIN} turns on at t_0. Q_{AUX} remains off. The primary current I_P, which is the sum of the transformer magnetizing I_{MAG} and the reflected secondary current I_{SEN}, flows through the primary of the transformer and Q_{MAIN}. I_P ramps up linearly while Q_{MAIN} is on. Current also flows in the secondary side through the rectifying MOSFET Q_R while Q_{MAIN} is on. No current flows through Q_{AUX} during this interval.
t_1 - t_2	Q_{MAIN} turns on at t_1. Q_R is now reversed-biased so the reflected secondary current component of I_P is zero. IP is now only the transformer magnetizing current. It decreases toward zero, charging the drain capacitance of Q_{MAIN}, C_{dMAIN}.
t_2 - t_3	At t_2 the drain voltage of Q_{MAIN} reaches the same voltage level as that voltage across C_{CLAMP}, the body diode of Q_{AUX} becomes forward-biased and voltage across C_{CLAMP} increases. The rate of increase of the drain voltage of Q_{MAIN} is now much lower, because C_{CLAMP} >> C_{dMAIN}.
t_3 - t_4	At t_3 Q_{AUX} turns on. Q_{AUX} switches under the ZVS condition providing it turns on after its body diode starts conducting (at t_2) and before I_P goes negative (at t_4). Q_{AUX} must be on before t_4, otherwise I_P has no path to go negative at t_4.
t_4 - t_5	At t_4 I_P is now negative and is discharging C_{CLAMP} through Q_{AUX}, which is on. I_P continues to become more negative and the drain voltage of Q_{MAIN} decreases. Q_{AUX} turns off at t_5 and the voltage across C_{CLAMP} stops decreasing. The only current path now available for the negative I_P to flow is out of C_{dMAIN}. The voltage across C_{dMAIN} decreases until I_P reaches zero. V_{DS} decays to zero by t_6 providing the energy stored in the magnetizing and leakage inductance at t_5 is greater than the energy stored in C_{dMAIN} at t_5. ZVS occurs if this condition is met, otherwise Q_{MAIN} switches on at t_6 at some intermediate voltage between zero and V_{DSMAX}.

IMPORTANT: Reducing L_{MAG} increases the inductive energy stored in L_{MAG} so if L_{MAG} is too big, ZVS does not occur as shown by the dashed line on the V_{DS} graph.

Design Procedure for the ACFC

Now that the principle of operation of the ACFC is understood a practical design example can be illustrated. The converter design process can be divided into several stages: power stage design, setup of the MAX17599 ACFC current mode controller, and the feedback loop. This document is primarily concerned with the power stage design, and the feedback loop is intended to complement the information contained in the MAX17599 data sheet for details on how to set up supervisory and protection functions of the controller.

The following design parameters are used throughout:

PARAMETER	SYMBOL
V_{IN}	Input Voltage
V_{START}	Undervoltage Turn-on Threshold
V_{OVI}	Overvoltage Turn-off Threshold
t_{SS}	Soft-Start Time
V_{OUT}	Output Voltage
ΔV_{OUT}	Output Ripple Voltage
I_{OUT}	Output Current
P_{OUT}	Output Power
η	Target Maximum Efficiency
P_{IN}	Input Power
f_{SW}	Switching Frequency
D	Duty Cycle
n	Primary-Secondary Turns Ratio
N_P	Turns of Primary Winding
N_S	Turns of Secondary Winding
N_{SD}	Turns of Secondary Self-Driven

The above symbols are sometimes followed by parentheses to indicate whether minimum or maximum values of the parameters are intended; for example, minimum input voltage is intended by the symbol $V_{IN(MIN)}$. Otherwise, typical values are intended.

In addition, through the design, procedure reference is made to the schematic in another document.

Step 1: Choosing a Suitable Switching Frequency

The MAX17599 can operate at a switching frequency between 100kHz and 1MHz. A lower switching frequency optimizes the design for efficiency, whereas a higher frequency allows for smaller inductive and capacitive components as well as lower costs. A switching frequency of 250kHz was chosen for this design. R1 sets the switching frequency according to the following expression:

$$R1 = \frac{1 \times 10^{10}}{f_{SW}}$$

Step 2: Setting the Maximum Duty Cycle

One advantage of using the MAX17599 for the ACFC is the maximum allowable duty cycle. If the duty cycle is not clamped at some maximum value, transformer saturation can occur, resulting in catastrophic failure, and Q_{MAIN} can be subjected to increased voltage stress. A maximum duty cycle of 72.5% is recommended at switching frequencies up to 400kHz. An initial choice of 63% allows for some design margin.

$$D_{MAX} = 0.63$$

Step 3: Calculating the Transformer Turns Ratio

For the forward converter topology, the transformer turns ratio is given by the following expression:

$$n = \frac{V_{IN(MIN)} - V_{MDS(ON)}}{V_{RDS(ON)} + V_{LOUT} + \frac{V_{OUT}}{D_{MAX}}}$$

where $V_{MDS(ON)}$ is the drain-source voltage of Q_{MAIN} in the on state, $V_{RDS(ON)}$ is the drain-source voltage of Q_R in the on state, and V_{LOUT} is the resistive DC voltage drop across the output inductor winding. D_{MAX} occurs at $V_{IN(MIN)}$. Assuming $V_{MDS(ON)}$ = 0.2V, $V_{RDS(ON)}$ = 0.2V, and V_{LOUT} = 0.2V then,

$$n = \frac{N_P}{N_S} = \frac{18V - 0.2V}{0.2V + 0.2V + \frac{24V}{0.63}} = 0.46$$

Step 4: Calculating Turns of the Primary Winding N_P, Secondary Winding N_S, Secondary Self-Driven Winding N_{SD}

For the forward converter topology, the transformer turns of the primary winding is given by the following expression:

$$N_P = \frac{V_{IN(MIN)} \times D_{MAX}}{\Delta B \times A_e \times f_{sw}} \times 10^4$$

where ΔB is the Flux density deviation of the transformer, which should be below or equal to 2000GS, A_e is the effective magnetic cross-section of the transformer core. Considering the maximum output power and the size of this design, we chose EFD25 as the transformer core. The effective magnetic cross of EFD25 is 0.58cm^2, then,

$$N_P = \frac{18V \times 0.63}{2000 \times 0.58 \times 10^{-4} \times 250 \times 10^3 Hz} \times 10^4 = 3.91$$

We use four turns for the primary winding; for the secondary turns,

$$N_S = \frac{N_P}{n} = \frac{4}{0.46} = 8.69$$

We use 9 turns for the secondary winding, then,

$$n = \frac{N_P}{N_S} = \frac{4}{9} = 0.44$$

The secondary self-driven voltage VSD of the rectifying MOSFET and freewheeling MOSFET is 5V.

$$N_{SD} = N_S \times \frac{V_{SD}}{V_{OUT}} = 9 \times \frac{5}{24} = 1.875$$

We use two turns for the secondary self-driven winding.

Step 5: Calculate D at $V_{IN(TYP)}$ and $V_{IN(MAX)}$

Re-arranging the expression in step 3 above gives

$$D = \frac{V_{OUT}}{\left(\frac{V_{IN} - V_{MDS(ON)}}{n}\right) - V_{RDS(ON)} - V_{LOUT}}$$

And,

DMIN	DTYP	DMAX
0.29	0.45	0.6

Step 6: Calculate $V_{MDS(MAX)}$ of Q_{MAIN} at D_{MIN}, D_{TYP} and D_{MAX}

For the forward converter topology, V_{MDS} is given by the following expression:

$$V_{MDS} = \frac{V_{IN}}{1 - D}$$

Given the D_{MAX} occurs at $V_{IN(MIN)}$, D_{TYP} occurs at $V_{IN(TYP)}$, and D_{MIN} occurs at $V_{IN(MAX)}$, we have

V_{MDS} AT $V_{IN(MAX)}$	V_{MDS} AT $V_{IN(TYP)}$	V_{MDS} AT $V_{IN(MIN)}$
50.7V	43.6V	45V

The critical operating parameters of the converter are now fixed, so it is possible to continue the design process of calculating and selecting suitable components for the power train.

Step 7: Calculating and Selecting L_{OUT}

The output inductance is calculated assuming a maximum peak-to-peak output ripple (ΔI_{SEC}), which occurs at maximum input voltage. The output inductance can be calculated as follows:

$$L_{OUT} = \frac{(V_{OUT} - V_{DSFW}) \times (1 - D_{MIN})}{I_{OUT} \times \%\,\Delta I_{SEC} \times f_{SW}}$$

Where V_{DSFW} is the drain-source voltage of the secondary freewheeling MOSFET, $\%\Delta I_{SEC}$ (0.6, typical) is the ratio of peak-to-peak output inductor current ripple to the average output current at maximum input voltage. We have

$$L_{OUT} = \frac{(24V - 0.2V) \times (1 - 0.29)}{4A \times 0.6 \times 250kHz} = 27.21\mu H$$

Where I_{OUT} = 4A and V_{DSFW} = 0.2V.

In this design, we can chose a standard ±20% tolerance 33µH inductor.

Finally, we must choose an output inductor with a DC winding resistance that is sufficiently low to ensure that V_{LOUT} is less than 0.2V at $I_{O(MAX)}$, because this is the value we have used for V_{LOUT} in the preceding calculations. We should choose an inductor with

$$R_{LDC} < \frac{V_{LOUT}}{I_{OUT(MAX)}} = \frac{0.2V}{4A} = 50m\Omega$$

The final inductor value chosen for this design is a 20% tolerance 33µH/44A/23.1mΩ inductor.

Step 8: Calculate the Transformer Magnetizing Inductance L_{MAG} and the Secondary and Primary Peak Winding Currents, $I_{S(PK)}$ and $I_{P(PK)}$

The physical design of the power transformer is outside the scope of this document; however it is necessary to calculate the critical parameters of the transformer.

We must first calculate the minimum output inductor ripple current by rearranging the expression in Step 7 and remembering that minimum ripple occurs at D_{MAX} as follows:

$$\Delta I_{L(MIN)} = \frac{(V_{OUT} - V_{DSFW}) \times (1 - D_{MAX})}{L_{OUT(MAX)} \times f_{SW}}$$

$L_{OUT(MAX)}$ for the selected ±20% 33µH inductor is 39.6µH. So,

$$\Delta I_{L(MIN)} = \frac{(24V - 0.2V) \times (1 - 0.6)}{39.6\mu H \times 250kHz} = 0.96A$$

For the MAX17599 ACFC current mode controller to function properly the maximum magnetizing current referred to the primary side of the transformer must be less than the minimum output inductor ripple current reflected to the primary side of the transformer. So:

$$I_{MAG(MAX)} < \frac{\Delta I_{L(MIN)}}{n}$$

And,

$$I_{MAG(MAX)} < \frac{0.96A}{0.44} = 2.18A$$

To allow for design margin we chose a value for I_{MAG} = 1.85A (85% of $I_{MAG(MAX)}$).

The next step is to calculate a minimum magnetizing inductance that ensures that $I_{MAG(MAX)}$ < 1.1A. We use the following expression to calculate $L_{MAG(MIN)}$:

$$L_{MAG(MIN)} = \frac{\left(V_{IN(MAX)} - V_{DS(ON)}\right) \times D_{MIN}}{I_{MAG(MAX)} \times f_{SW}}$$

So,

$$L_{MAG(MIN)} = \frac{(36V - 0.2V) \times 0.29}{1.85A \times 250kHz} = 22.45\mu H$$

Allowing for a ±30% tolerance for the magnetizing inductance we can choose L_{MAG} = 40µH ±30%.

Figure 4 illustrates the output inductor current I_L, the secondary transformer current I_S, primary transformer current I_P and the current flowing in main power MOSFET, I_{QM}.

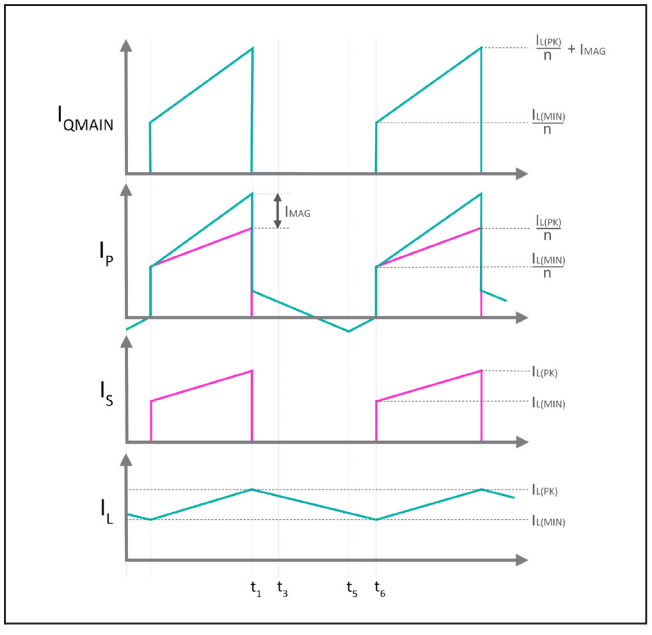

Figure 4. Current waveforms.

Although I_P appears linear when both Q_M and Q_A are off (t_1 to t_3 and t_5 to t_6), there is a resonance between the two end points, which makes ZVS possible.

The peak current in the secondary winding $I_{S(PK)}$ is equal to the peak current in the output inductor $I_{L(PK)}$. $I_{L(PK)}$ is a maximum at $V_{IN(MAX)}$ and $I_{O(MAX)}$, therefore:

$$I_{L(PK)} = I_{O(MAX)} + \frac{(V_{OUT} - V_{DSFW}) \times (1 - D_{MIN})}{2 \times L_{OUT(MIN)} \times f_{SW}}$$

And,

$I_{S(PK)} = I_{L(PK)}$

So,

$$I_{S(PK)} = 4A + \frac{(24V - 0.2V) \times (1 - 0.29)}{2 \times 26.4\mu H \times 250kHz} = 5.28A$$

The peak current in the primary winding $I_{P(PK)}$ is the peak current in the secondary winding reflected back to the primary side of the transformer plus I_{MAG}.

Therefore,

$$I_{P(PK)} = \frac{I_{S(PK)}}{n} + I_{MAG}$$

So,

$$I_{P(PK)} = \frac{5.28A}{0.44} + 1.85A = 13.85A$$

The transformer must not saturate at a magnetizing force of (N_P x $I_{P(PK)}$) where N_P is the number of turns on the primary winding.

Step 9: Calculate the Maximum RMS Currents in the Transformer Secondary and Primary Windings, $I_{S(RMS)}$ and $I_{P(RMS)}$

The maximum RMS currents in the transformer primary and secondary windings occur at $V_{IN(MIN)}$ and $I_{OUT(MAX)}$, i.e., at D_{MAX}. To calculate $I_{S(PK)}$ at $V_{IN(MIN)}$ we must first calculate $I_{L(PK)}$ in the output inductor at $V_{IN(MIN)}$.

Following the process of Step 8 we have,

At $V_{IN(MIN)}$,

$$I_{L(PK)} = I_{O(MAX)} + \frac{(V_{OUT} - V_{DSFW}) \times (1 - D_{MAX})}{2 \times L_{OUT(MIN)} \times f_{SW}}$$

And,

$I_{S(PK)} = I_{L(PK)}$

So,

$$I_{S(PK)} = 4A + \frac{(24V - 0.2V) \times (1 - 0.6)}{2 \times 26.4\mu H \times 250kHz} = 4.4A$$

The current at which the secondary rectifying MOSFET Q_R starts to conduct $I_{S(V)}$, corresponds to $I_{L(MIN)}$.

So,

$$I_{S(V)} = 4A - \frac{(24V - 0.2V) \times (1 - 0.6)}{2 \times 26.4\mu H \times 250kHz} = 3.6A$$

We can now calculate the maximum RMS current in the secondary winding as follows:

$$I_{S(RMS)} = \sqrt{(D_{MAX}) \times \frac{I_{S(PK)}^2 + I_{S(PK)} \times I_{S(V)} + I_{S(V)}^2}{3}}$$

So,

$$I_{S(RMS)} = \sqrt{(0.6) \times \frac{4.4A^2 + 2.4A \times 3.6A + 3.6A^2}{3}} = 3.1A$$

Referring to Figure 4, we can calculate the instantaneous current in Q_M at turn-on and turn-off, $I_{QM(t\text{-}on)}$ and $I_{QM(t\text{-}off)}$, respectively.

$$I_{QM(t-on)} = \frac{I_{S(V)}}{n} = \frac{3.6A}{0.44} = 8.18A$$

$$I_{Q(t-off)} = \frac{I_{S(PK)}}{n} + I_{MAG}$$

So,

$$I_{QM(t-off)} = \frac{4.4A}{0.44} + 1.85A = 11.85A$$

The maximum RMS current in QM can now be calculated as follows:

$$I_{QM(RMS)} = \sqrt{(0.6) \times \frac{11.85A^2 + 11.85A \times 8.18A + 8.18A^2}{3}} = 7.8A$$

The transformer primary current I_P in Figure 4 is a more complex waveform that I_{QM}. I_P is a superposition of I_{QM} and I_{QA}, and the resonant currents that flow during the time intervals when both Q_M and Q_A are off. Nevertheless, it is reasonable to use the approximation that

$$I_{P(RMS)} = I_{QM(RMS)}$$

We now have all the critical parameters of the transformer, as detailed in the following table.

PARAMETER	SYMBOL	VALUE
Primary Magnetizing Inductance	L_{MAG}	40µH ±30%
Primary Peak Current	$I_{P(PK)}$	13.85A
Primary RMS Current	$I_{P(RMS)}$	7.8A
Turns Ratio (N_S/N_P)	n	0.44
Primary Turns	N_P	4
Secondary Turns	N_S	9
Secondary Self-Driven Turns	N_{SD}	2
Secondary Peak Current	$I_{S(PK)}$	4.4A
Secondary RMS Current	$I_{S(RMS)}$	3.1A

Using the parameters in the table above, a suitable transformer can be designed.

Step 10: Choose a Suitable MOSFET for Q_M

All the necessary parameters for selecting a suitable QM have already been calculated.

From step 6, $V_{DS(MAX)}$ = 50.7V.

From step 8, $I_{QM(PK)} = I_{P(PK)}$ = 13.85A.

And $I_{QM(RMS)}$ = 7.8A.

Allowing for reasonable design margin, Vishay® part number SIS468DN-T1-GE3 was chosen for this design with the following specifications:

Maximum D-S Voltage	80V
Continuous Drain Current	30A
D-S Resistance at V_{GS} = 4.5V	32mΩ
Total Gate Charge Q_g	8.7nC

Step 11: Choose Suitable Rectifying and Freewheeling MOSFET for Q_R and Q_{FW}, Respectively

Almost all the necessary parameters for selecting a suitable Q_R have already been calculated. In step 8, we calculated $I_{S(PK)}$, the same peak current that flows in Q_R.

So,

$$I_{QR(PK)} = I_{S(PK)} = 4.4A$$

In step 9, we calculated the maximum RMS current in the transformer secondary winding $I_{S(RMS)}$, the same RMS current that flows in Q_R.

So,

$$I_{QR(RMS)} = I_{S(RMS)} = 3.1A$$

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The peak drain-source voltage seen by Q_R is given by

$$V_{QR(R)} = \frac{V_{IN(MIN)} D_{MAX}}{n(1 - D_{MAX})}$$

So,

$$V_{DR(R)} = \frac{18V \times 0.6}{0.44 \times (1 - 0.6)} = 61.36V$$

For the freewheeling MOSFET Q_{FW} we have

$$I_{FW(PK)} = I_{S(PK)} = 4.4A$$

The maximum RMS current in the freewheeling diode occurs at $V_{IN(MAX)}$ and is calculated using

$$I_{FW(RMS)} = \sqrt{(1 - D_{MIN}) \times \frac{I_{FW(PK)}^2 + I_{FW(PK)} \times I_{FW(V)} + I_{FW(V)}^2}{3}}$$

Where,

$$I_{FW(V)} = I_{O(MAX)} - \frac{(V_{OUT} - V_{QFW}) \times (1 - D_{MIN})}{2 \times L_{OUT(MIN)} \times f_{SW}} = 2.72A$$

So,

$$I_{FW(RMS)} = 3.03A$$

Finally, the peak drain-source voltage seen by Q_{FW} is given by

$$V_{DFW(R)} = \frac{\left(V_{IN(MAX)} - V_{QR(F)}\right)}{n} = \frac{(36V - 0.2V)}{0.44} = 81.36V$$

Allowing for a reasonable design margin, a Vishay n-MOSFET, part number SISS40DN-T1-GE3, was selected for both Q_R and Q_{FW}.

Step 12: Choose Suitable P-Channel MOSFET for the Active Clamp Switch Q_A

Only a portion of the primary magnetizing current flows in the drain of the active clamp switch during the interval between t_3 and t_5. If we assume as the worst case that all the magnetizing current flows in Q_A, then we can estimate the RMS current flowing in the drain of Q_A as follows:

$$I_{MAG(RMS)} = \sqrt{D_{MAX} \times \frac{I_{MAG}^2}{3}} = \sqrt{0.6 \times \frac{1.85A^2}{3}} = 827mA$$

At such a low RMS current, conduction losses will be very low, so choosing a MOSFET with a low gate charge should be the primary consideration, with low $R_{DS(ON)}$ being only a secondary concern. In addition to conduction losses being very low, switching losses are also negligible, because the body diode of Q_A is conducting before Q_A turns on. The repetitive peak current in Q_A is the maximum primary magnetizing current:

$$I_{QA(PK)} = I_{MAG} = 1.85A$$

The active clamp switch will experience the same voltage stress as the main power switch;referring to step 6 this is as follows:

$$V_{DS(QA)} = V_{DS(QM)} = \frac{V_{IN}}{1 - D} = 50.7V$$

Allowing for reasonable design margin, Vishay P-Channel MOSFET, Si2337DS, was chosen for this design, with the following specifications:

Maximum D-S Voltage	80V
Peak Repetitive Drain Current	2.2A
D-S Resistance at V_{GS} = 7V	0.215Ω

Step 13: Choose a Suitable Clamp Capacitor C12

The clamp capacitor (C12) helps in resetting the flux in the transformer core as well absorbing leakage inductance energy, and it forms a complex pole-zero pair with the magnetizing inductance (L_{MAG}) of the transformer, at a frequency f_R.

$$f_R = \frac{1 - D_{MAX}}{2\pi \times \sqrt{L_{MAG} \times C_{12}}}$$

The value of the clamp capacitor for a 20% voltage ripple is calculated as:

$$C_{12} = \frac{\Delta I_{MAG} \times (1 - D_{MIN})^2}{1.6 \times V_{IN(MAX)} \times f_{SW}} = \frac{1.85A \times (1 - 0.29)^2}{1.6 \times 36V \times 250000Hz} = 65nF$$

We chose 33nF as the clamp capacitor.

The voltage stress on the clamp capacitor can be calculated as:

$$V_{C12} = \frac{V_{IN}}{1-D} = V_{DS}$$

The C12 should be rated for at least 1.4x the calculated worst-case V_{C12} stress.

Step 14: Calculate and Choose the Output Capacitor C_{OUT}

Output capacitance value can be calculated based on either steady-state voltage ripple or transient voltage ripple. If the design consideration is the transient steady-state voltage ripple, then the output capacitor is usually sized to support a step load of 25% of the rated output current (I_{OUT}) in isolated applications so that the output-voltage deviation is contained to 3% of the rated output voltage. The output capacitance can be calculated as follows:

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

where C_{OUT} is the total capacitance required at the output, I_{STEP} is the load step, $t_{RESPONSE}$ is the response time of the controller, and ΔV_{OUT} is the allowable output voltage deviation during transient.

Response time of the controller $t_{RESPONSE}$ is given as

$$t_{RESPONSE} = \frac{0.33}{f_C} + \frac{1}{f_{SW}}$$

The complex pole-zero pair frequency formed due to clamp capacitor and magnetizing inductance of the converter is given as

$$f_R = \frac{1-D_{MAX}}{2 \times \pi \times \sqrt{L_{MAG} \times C_{12}}} = \frac{1-0.6}{2 \times 3.14 \times \sqrt{40 \times 10^{-6}\mu H \times 22 \times 10^{-9}\mu F}} = 68kHz$$

f_C is the target closed-loop crossover frequency, which is given as

$$f_C = \frac{f_R}{5} = 13.6kHz$$

So, the response time of the controller $t_{RESPONSE}$ is given as

$$t_{RESPONSE} = \frac{0.33}{13.6 \times 10^3 Hz} + \frac{1}{250 \times 10^3 Hz} = 28\mu s$$

Choose I_{STEP} equal to 25% of output current, I_{STEP}, ΔV_{OUT} = 3% of output voltage, which is equal to 720mV.

So, the output capacitance is given as

$$C_{OUT} = \frac{1A \times 28 \times 10^{-6} A}{2 \times 0.72V} = 19.44\mu F$$

In this design, to get smaller output voltage ripple, 4 x 22µF ceramic capacitors are used. Considering 20% derating of the ceramic capacitors, the total ceramic output capacitance would be 4 × 22µF × 0.8 = 70.4µF.

Step 15: Calculate and Choose the Input Capacitor C_{IN}

Capacitor selection is based on switching ripple. The maximum average input current drawn from the input power supply at minimum input voltage can be calculated as

$$I_{IN(AVG)} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} = \frac{24V \times 4A}{0.92 \times 18V} = 5.8A$$

The voltage ripple present on the input capacitor is 2% of the minimum input voltage and is given as

$$\Delta V_{IN(RIPPLE)} = 0.02 \times V_{IN(MIN)} = 0.02 \times 18V = 0.36V$$

The value of the input ceramic capacitor with the above assumed ripple voltage can be calculated as follows:

$$C_{IN} = \frac{I_{IN(AVE)} \times (1-D_{MAX})}{\Delta V_{IN(RIPPLE)} \times f_{SW}} = \frac{5.8A \times (1-0.6)}{0.36V \times 250000Hz} = 26.51\mu F$$

In this design, 3 × 10µF ceramic capacitors are used for the input capacitor.

Step 16: Calculating and Selecting the UVLO and OVI Resistor

Figure 5 illustrates how undervoltage lockout (UVLO) and overvoltage inhibit (OVI) are implemented in this design. The EN/UVLO pin on the MAX17599 serves as an enable/

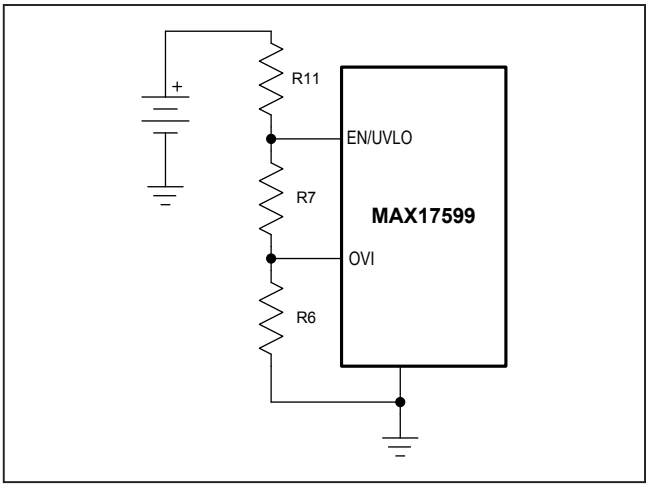

Figure 5. UVLO and OVI.

disable input, as well as an accurate programmable UVLO pin. MAX17599 operation is only guaranteed when the voltage on the EN/UVLO pin exceeds 1.26V. Once operating, the MAX17599 continues to operate, providing the voltage on the EN/UVLO pin exceeds 1.20V.

The OVI pin on the MAX17599 serves as an accurate programmable OVI input. The MAX17599 is guaranteed to shut when the voltage on the OVI pin exceeds 1.26V. Switching is guaranteed to resume only when the voltage on the OCI pin falls below 1.1V. In this instance, the MAX17599 performs the soft-start sequence.

Because R11, R7, and R6 are applied across V_{IN}, the starting point for choosing appropriate values for these resistors is setting a limit for the maximum power P_{IVP} dissipated in the resistors. By choosing a maximum allowable power loss in the resistor divider R11, R7, R6, we can calculate the maximum current in the resistors at $V_{IN(OVI)}$ as follows:

$$I_{OVI} = \frac{P_{IVP}}{V_{IN(OVI)}}$$

At $V_{IN(OVI)}$ the voltage across R4 should be 1.26V to ensure OVI shutdown, so,

$$R6 = \frac{1.26V}{I_{OVI}}$$

At $V_{IN(UVLO)}$ the current in the resistors R11, R7, R6 is

$$I_{UVLO} = \frac{V_{IN(UVLO)}}{V_{IN(OVI)}} \times I_{OVI}$$

At $V_{IN(UVLO)}$ the voltage across (R4+R7) should be 1.26V to ensure start-up of the MAX17599 at the UVLO threshold, so,

$$(R6 + R7) = \frac{1.26V}{I_{UVLO}}$$

Substituting for R4, we have

$$R7 = \frac{1.26V}{I_{UVLO}} - \frac{1.26V}{I_{OVI}}$$

at $V_{IN(UVLO)}$:

$$V_{R11} = V_{IN(UVLO)} - 1.26V$$

and

$$R11 = \frac{V_{R5}}{I_{UVLO}}$$

Substituting for VR5 we have

$$R11 = \frac{\left(V_{IN(UVLO)} - 1.26V\right)}{I_{UVLO}}$$

For this design, we have set P_{IVP} = 2mW, $V_{IN(OVI)}$ = 38V, and $V_{IN(UVLO)}$ = 16V. The closest standard values for R11, R7, and R6 are 680kΩ, 30kΩ, and 24kΩ, respectively.

Step 17: Calculating and Selecting the Peak Current Limit Resistors (R8 and R18)

The current sense resistors R8 and R18 are connected between the source of Q_{MAIN} and P_{GND}. This resistor sets the peak current limit of the power supply. When Q_{MAIN} is on the primary transformer current I_P flows through R8 and R18 and the voltage developed across R8 and R18 is measured at the CS pin of the MAX17599.

The MAX17599 implements 70ns of leading-edge blanking to suppress leading edge-current spikes that might be encountered due to circuit and component parasitic. An additional RC filter (R17, C11) can be placed between the source of Q_{MAIN} and the CS pin of the MAX17599 to increase the amount of leading-edge blanking.

The signal voltage obtained at the CS pin is used for current mode control and peak current limiting purposes. A voltage of 305mV on the CS pin terminates the NDRV and AUXDRV drives to the MOSFETs until the next switching cycle begins.

R18 can be calculated so that when the peak primary current (plus 50% design margin) is flowing in Q_{MAIN}, the voltage across R21 is 305mV, so,

$$R_{21} = \frac{305mV}{1.5 \times I_{P(PK)}} = 15m\Omega$$

A standard 33mΩ current sense resistor is used in the design. Low inductance current sense resistors should be used for R8 and R18.

Step 18: Calculating and Selecting the Dead-Time Resistor (R3)

Placing dead-time between the NDRV and AUXDRV drive edges allows ZVS to occur, minimizing switching losses and improving efficiency. Resistor R8 connected from the DT pin of the MAX17599 to SGND programs the amount of dead-time. This amount of dead time is applied to both leading and trailing edges of the drive signals. A dead-time between 25ns and 250ns can be calculated by:

$$R3 = 0.4 \times t_{DT}$$

Where R3 is in kΩ and t_{DT} is in ns. A value of 100k is chosen to give a dead-time of 250ns. The dead-time can be increased by experiment to ensure ZVS across the widest range of line and load conditions.

Design Resources

Download the complete set of **Design Resources** including schematics, bill of materials, PCB layout, and test files.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/19	Initial release	—

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